A hardware implementation of the Levinson routine in the radio detector of cosmic rays to improve a suppression of non-stationary RFI

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ABSTRACT

The radio detector system for ultra high-energy cosmic rays in the Pierre Auger Observatory operates in the frequency range 10-30 MHz, which is often contaminated by human-made RFI. Several filters were used to suppress RFI: based on the FFT, IIR notch filter and FIR filter based on the linear prediction. The last refreshes the FIR coefficients calculating either in the external ARM processor, internal soft-core NIOS® processor implemented inside the FPGA or hard-core embedded processors (HPS) being a silicon part of the FPGA chip. Refreshment times significantly depend on the type of calculation process. For stationary RFI, the FIR coefficients can be refreshed each minutes or even hours. However, an efficient suppression of non-stationary short-term contaminations requires a much faster response. Calculations of FIR coefficients in an external ARM take 1-2 seconds, by the soft-core virtual NIOS® processor on the level of hundreds milliseconds. The HPS allows a reduction of refreshment time to 560 µs (the 32-stage FIR filter). A symmetry of covariance matrix allows one to use the much faster Levinson procedure instead of typical Gauss routine for solving a set of linear equations. The Levinson procedure calculated even in the HPS takes relatively a lot of time. A hardware implementation of this procedure inside the FPGA fabric as specialized a micro-controller requires only ~53 800 clock cycles. We used 64- or 48-bit floating point numbers to calculate FIR coefficients. Resources occupation is relatively high, as the design was optimized for a maximal register performance. However, the RFI suppression is very efficient. We expect significant suppression of even short-term non-stationary RFI.

CONCLUSIONS

The hardware Levinson procedure implemented into FPGA fabric significantly shortens the refreshment time in the linear predictor approach used for RFI suppression. With Cyclone® IV (FPGA used at present in the Dutch AERA digitizers) and in Cyclone® V (considered as FPGA for the future upgrade) the refreshment time is on a level of 560 µs (with 100 MHz clock for covariances calculation and the Levinson recursion). The 200 MHz speed has been achieved in the Stratix® III FPGAs (speed grade - 2) and allowed a reduction of refreshment time to 275 µs, however, the Stratix® series are too power consuming and too expensive. We plan to use the above algorithm for tests of RFI suppression: a) in Łódź environment using the standard AERA antenna and b) in real radio stations on Argentinean pampas.

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Fig. 1 − The structure of data flow for the hardware implementation of the Levinson algorithm.

Fig. 2 − A structure of 32 fast logic blocks calculating covariances (accu in Fig. 1. All data are the fixed-point representations.

Fig. 3 − C code of the Levinson algorithm.

Fig. 4 − Four first steps in the Levinson algorithm implementation.

Fig. 5 − The structure of the FIR filter.

Fig. 6 − Fourier spectra for the original signal (A) and for a single calculation of FIR coefficients (B) in the beginning of trace cleaning.

Fig. 7 − Multidetectors of Fourier spectra for a single FIR coefficients calculation (A) and for each pixel in (B).

Fig. 8 − “Quantum” simulation of FIR coefficients calculation by the hardware Levinson procedure. Calculation of 3 and 5 covariances takes 12 and 20 µs, respectively. Floating point coefficients takes next ~538 µs. Simulations show sequence of processing in the consecutive A, B, C and D loops.

Fig. 9 − Comparison of 64- and 48-bit input covariances (two left columns), FIR coefficients calculated in the PC (middle column) and in the FPGA 64-bit (4th column) and 48-bit (right column). Some discrepancy on least significant bits for 64-bit calculations are visible. However, the relative accuracy is on a level of 10-13. The accuracy for 48-bit calculations dramatically drops down to a level of 10-4.

Fig. 10 − Quartus® simulation of FIR coefficients calculation by the hardware Levinson procedure. Calculation of r and y covariances takes 12 and 20 µs, respectively. Floating point coefficients takes next ~538 µs. Simulations show sequence of processing in the consecutive A, B, C and D loops.