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Beam Test Performance of the Prototype Trigger-less Data Acquisition for the PANDA Experiment

Tuesday, 7 June 2016 15:00 (1h 30m)

We present the first FPGA-based version of a Prototype Trigger-less Data Acquisition (PTDAQ) for the PANDA experiment. The PANDA experiment will operate in an trigger-less environment of 20 MHz interaction rate, with a peak rate up to 50 MHz, and a design luminosity of 2 x 10^{32} cm^{-1} s^{-1}. The event size will be about a few KB, producing data rates of several hundreds of GB/s. A reduction of up to three orders of magnitude will be accomplished after event filtering based on a full reconstruction of the events in real-time, including tracking and particle identification.

An additional complication arises from overlapping events occurring at high event rates. Thus, event assembly is a highly non-trivial process and is accomplished by combining data packets from the freely streaming subsystems using precision time stamps.

The PTDAQ system consists of xTCA-based FPGA Processor (xFP) cards, equipped with a Xilinx Virtex-5 FPGA and 4 GB DDR2 RAM. The system is scalable. The xFP cards are either hosted by a microTCA shelf or by a AdvancedTCA carrier board. This hardware platform is a development of IHEP Beijing in cooperation with JLU Giessen.
Featuring similar functionality as the final DAQ of PANDA, the PTDAQ receives data from freely streaming front-end electronic devices (FEE) synchronized using the Synchronization of Data Acquisition Network (SODANET). We have implemented data input and output interfaces and basic features like zero suppression and low level event-building in VHDL. For Gigabit Ethernet I/O we use FPGA implementations of the TCP and UDP protocols from collaborating institutes.

A first in beam test at the MAMI facility reading out a PANDA electromagnetic calorimeter prototype as well as the Glasgow Tagged Photon Spectrometer was performed in November 2015. This is the first test of the full DAQ chain including SODANET and the PTDAQ.

In this contribution we present the overall architecture of the PTDAQ system as well as results from the test.

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