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A coprocessor for the Fast Tracker Simulation

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The Fast Tracker (FTK) executes real time tracking for online event selection in the ATLAS experiment. Data processing speed is achieved by exploiting pipelining and parallel processing. Track reconstruction is executed on a 2-level pipelined architecture. The first stage, implemented on custom ASICs called Associative Memory (AM) Chips, performs Track Candidate (road) recognition in low resolution. The second stage, implemented on FPGAs (Field Programmable Gate Arrays), builds on the track candidate recognition, performing Track Fitting in full resolution.

The use of such parallelized architectures for real time event selection opens up a new huge computing problem related to the analysis of the acquired samples. For each type of implemented trigger, millions of events have to be simulated to determine, within a small statistical margin of error, the efficiency and the bias of that trigger. The AM chip emulation is a particularly complicated task.

This paper proposes the use of a hardware co-processor, in place of its simulation, to solve the problem. We report on the implementation and performance of all the functions complementary to the pattern matching in a modern, compact embedded system for track reconstruction. That system is the miniaturization of the complex FTK processing unit, which is also well suited for powering applications outside the realm of High Energy Physics as well.

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