Contribution ID: **129** Type: **Poster presentation**

Upgrade Of The Central Logic Board For The Phase-2 Of The KM3NeT Neutrino Telescope.

Tuesday 7 June 2016 15:00 (1h 30m)

The KM3NeT collaboration aims the construction of a multi-km3 high-energy neutrino telescope in the Mediterranean Sea consisting of thousands of glass spheres, each of them containing 31 photomultiplier of small photocathode area. The main elements of a neutrino telescope are, therefore, the sensitive optical detectors, which on the case of KM3NeT is the small photocathode area photomultipliers (PMT) distributed around the glass sphere of Digital Optical Module (DOM). Each DOM has 31 small PMT which collect the Cherenkov light and convert it onto electronic signals. In order to translate these signals onto the arrival time of the photons, they are processed by Time to Digital Converters (TDC).
The firmware of the DOM is based on two LM32 microprocessors, an open source firmware microprocessor from Lattice. One of them is dedicated to the White Rabbit protocol which directly manages the tunable oscillators and the optical link traffic, in order to achieve a time synchronization of sub-nanosecond level with the Grand Master clock of the on-shore station. The rest of the modules are managed by the second microcontroller, which has access to all the communication interfaces (SPI, UART, GPIO and I2C) needed for the instrumentation devices, the acoustic and optical readout systems and the multiboot module.
31 TDCs are responsible to record the arrival time and the width (with 1 ns of resolution) of the hits incoming from the signals of the PMTs. An acoustic readout is dedicated to the decoding of the incoming AES3 formatted stream. All the data, together with some other slow control monitoring information (as temperature, humidity, tilt meter, compass, currents, etc. .) are put in UDP packets and connected to an IP/UDP packet buffer stream selector (IPMUX). This IPMUX splits the data into separate streams, based on UDP port number and send to the shore station via the endpoint, a normal Ethernet MAC but it has time stamping capabilities allowing sub-nanosecond timing precision, such that it facilitates the Precision Time Protocol (IEEE588).
The multiboot allows the selection of a different image from where to boot the electronic system and the presence of a Golden Image as a fallback solution, will make possible to remotely configure the firmware after the deployment of the DOM.
All these features are implemented effectively on Artix FPGA, reducing resources, costs and power consumption with respect to the phase-1 prototype, based on Kintex-7.
The control of the DOM is achieved through complex and robust embedded software running in the LM32. No operative system is used in order to reduce power consumption. The software allows multiple parties to work on it and extending it without compromising stability and clarity. The software has been layered into three main modules, named Common, which contain the common functions, macros and standard libraries. Platform layer, which includes the start-up code and drivers, and App layer for the application specific code. Each module has its own use and has security restrictions for functions in different levels (with exception of callbacks)

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Session Classification: Poster session 1

Track Classification: Upgrades