A Testbench Based on UVM Research for ABCStar

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Abstract

It is demanding to implement more and more functions and algorithms in front-end Application-Specific Integrated Circuit (ASIC), which, in consequence, makes the logic designs more complicated. It necessitates to develop reliable and robust function verification test benches during ASIC designs. ABCStar is a front-end readout ASIC under development and aims to read out the silicon strip sensor for ATLAS Phase II upgrade. Its digital part would include two levels of buffering, several trigger modes, cluster identification, data formatting, and etc. To simulate and verify its full functions, we have built a well-constructed testbench with the Universal Verification Methodology (UVM), which represents an advance and powerful verification methodology based on SystemVerilog. Features of the testbench include: functional coverage evaluation, result comparison with reference models, and selected SystemVerilog assertions for validating key design features.

Test Results

1 Input Register detection mode test
There are four detection modes for ABCStar Input Register, two for normal data taking (Level and Edge mode), one for alignment (hit mode), and one reserved for special usage.

With corresponding concurrent assertions, we can check whether the Device Under Test (DUT) works correctly in each mode. We also sample the functional coverage output hits of the Input Register in three modes.

2 Maskbits test
ABCStar supports turning off bad or noisy channels through a mask register according to the following logic:

\[
\text{output\_data} (256\ \text{bits}) = \text{input\_data} (256\ \text{bits}) \& \text{maskbits} (256\ \text{bits}).
\]

3 Trigger combination test
We use constraint combination stimulus to produce:

- \(L0\) with a fixed latency;
- \(L0\) intervals = $\text{dist\_posion}(seed, 40)$ (BCs, rate is 1MHz).
- \(LP\) latency = $\text{dist\_poisson}(seed, 480)$ (BCs, mean is 12us).
- \(LP\) intervals = $\text{dist\_poisson}(seed, 40)$ (BCs, rate is 1MHz).
- \(PR\) latency = $\text{dist\_poisson}(seed, 480)$ (BCs, mean is 12us).
- \(PR\) intervals = $\text{dist\_poisson}(seed, 400)$ (BCs, rate is 100KHz).

*Note: BC is Beam Crossing Clock, JBC=25ns

Conclusion

- We have built a well-structured testbench for the ABCStar design based on UVM. It includes functional coverage statistic, a reference for result comparison, and assertions for real time validation.
- We have verified the main features of the ABCStar, by using UVM-constrained and randomized stimulus to simulate the real data input. The coverage and assertions show the design is working correctly.