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A Timing Synchronizer System for Beam Test Setups requiring Galvanic Isolation

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Detector elements operated with preproduction setups of readout chains are analyzed during beam tests. Usually, the readout chain of a beamtime setup is composed of different kinds of processing boards being mainly built from FPGAs, microcontrollers and custom readout ASICs.
Besides high-speed links which are used to transfer the data recorded by the frontend electronics to a post-processing system, it is mandatory to provide adequate means in order to control the readout system. For the overall system control a slow-control system can be used like the IPbus system developed at CERN.
However, in many readout systems it is important that at least the frontend electronics that samples the signals from the detector, runs with a clock of common frequency which has a known phase relation among the frontend ASICs. For that reason, a timing control system is required which distributes a clock from a central master to the slave nodes that connect to the frontend electronics and provide the data path of the readout.
In case of a pre-series beam test setup of the CBM Silicon Tracking System, the detector elements together with the readout ASICs need to be interfaced with DC-coupled connections. Due to their physical characteristics, the detector elements together with the parts of the data acquisition up to the FPGA-based processing nodes need to be operated at a ground potential which is offset by a few hundred volts for the p- and n-side respectively. Thus, all of the control and data links to these processing nodes require a galvanic isolation in order to prevent damage from the connected electronics.
Taking into account all of these requirements, a versatile FPGA-based point-to-multipoint timing synchronizer system was developed which allows to provide a common clock and pulse-per-second signal to the slave processing nodes.
The firmware running on the FPGAs of the timing synchronizer data processing boards (tDPB) is fully controllable through IPbus and offers different features like the operation with internal or external clock or PPS, automatic clock switch-over, second and cycle counters and fine phase shifting of transmitted and received clocks.
The development of the tDPB system did incorporate the design of FPGA Mezzanine Cards (FMC) which offer galvanically isolated constant latency LVDS links for the transmission over twisted-pair cables and can be mounted on Advanced Mezzanine Cards (AMC) to be used in MicroTCA crates.
Using these FMC cards, different system topologies may be composed like a cascaded tDPB system structure with a Grand-Master, Sub-Masters and the Slave processing nodes, e.g. offering 56 Slave links. For future setups the Master tDPB AFCK may be mounted inside a MicroTCA crate, where the Grand-Master clock and PPS is supplied through the backplane of the crate.
The system was implemented and evaluated on AMC FMC Carrier Kintex (AFCK) FPGA boards. Measurements show that the system is capable of operating beamtime setups with twisted-pair cables at the target distance of 10 meters between nodes.

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