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Design of a 10-Gbps Random Number Recorder

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We have design a 10-Gbps true random number generator recently and the quality verification requires an ultra-fast data cache device to acquire very long continuous random bit sequence. The NIST statistical test suite does not require a length of sequences or a quantity of sample data. However, to get a credible result from the test suite, we plan to acquire at least 1 giga continuous random bits for each generator channel at 1-Gbps generate rate. With these target, the commercial instruments such as the oscilloscope or the logic analyzer cannot acquire the random data at the high rate nor the record depth.

With the requirements, we design a data acquisition system to record the 1 giga continuous random bits in real time. The DAQ system has three parts: Acquisition, Cache, and Data up-link. Acquisition is the interface to the high-speed random data, and we use Gigabit Transceiver (GTX) and select IO in FPGA to deserialize the random data. The low-speed parallel data can be handled by the FPGA code and cache the data in an external DDR3 memory. When enough random data is stored, these data is upload to PC via Ethernet.

The first hardware demo is accomplished with a Xilinx Vertex 6 evaluation board. The GTX module in Vertex 6 can work up to 6 Gbps while we use it works at 1 Gbps to deserialize the random data. The parallel data is stored in an onboard 2 GB DDR3 memory stick. We fill the 2 GB DDR3 memory with continuous random bits, and update the random data to PC via Ethernet. The demo meets our requirement of the data acquisition for one channel of the random number generator and proves the DAQ structure.

We customized a DAQ design with the structure and fulfill the ten channel random bits acquisition. The random data from the DAQ also pass the NIST statistical test for random number. Both the 10-Gbps true random number generator and fast digital data DAQ system are succeed. The structure of the DAQ system is also a guidance for the similar instrument.

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