

RT2016

Phase-I Trigger Readout Electronics Upgrade for the ATLAS Liquid-Argon Calorimeters

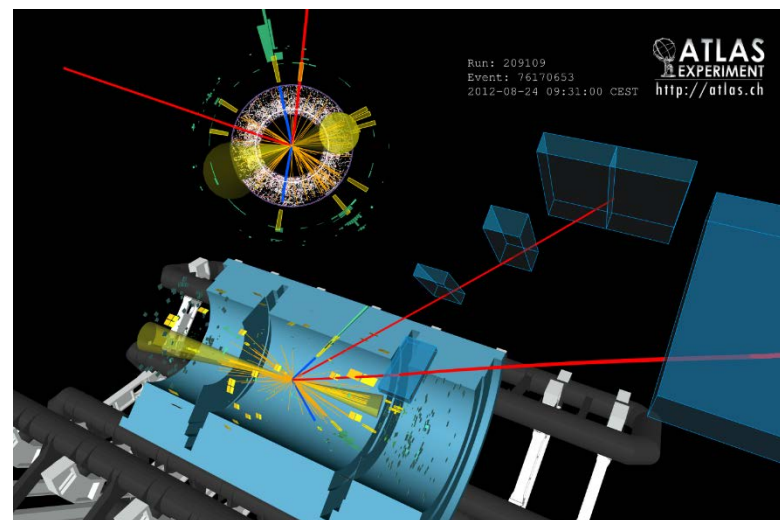
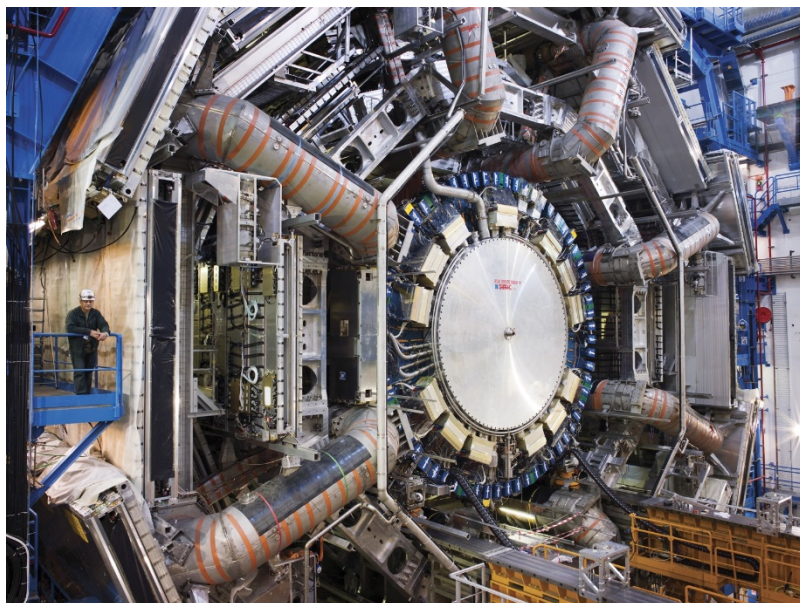
*Nicolas Chevillot (LAPP/CNRS-IN2P3)
on behalf of the ATLAS Liquid Argon Calorimeter Group*

Plan

- Context
- Front-end upgrade
- Back-end upgrade
- Demonstrator
- Conclusions

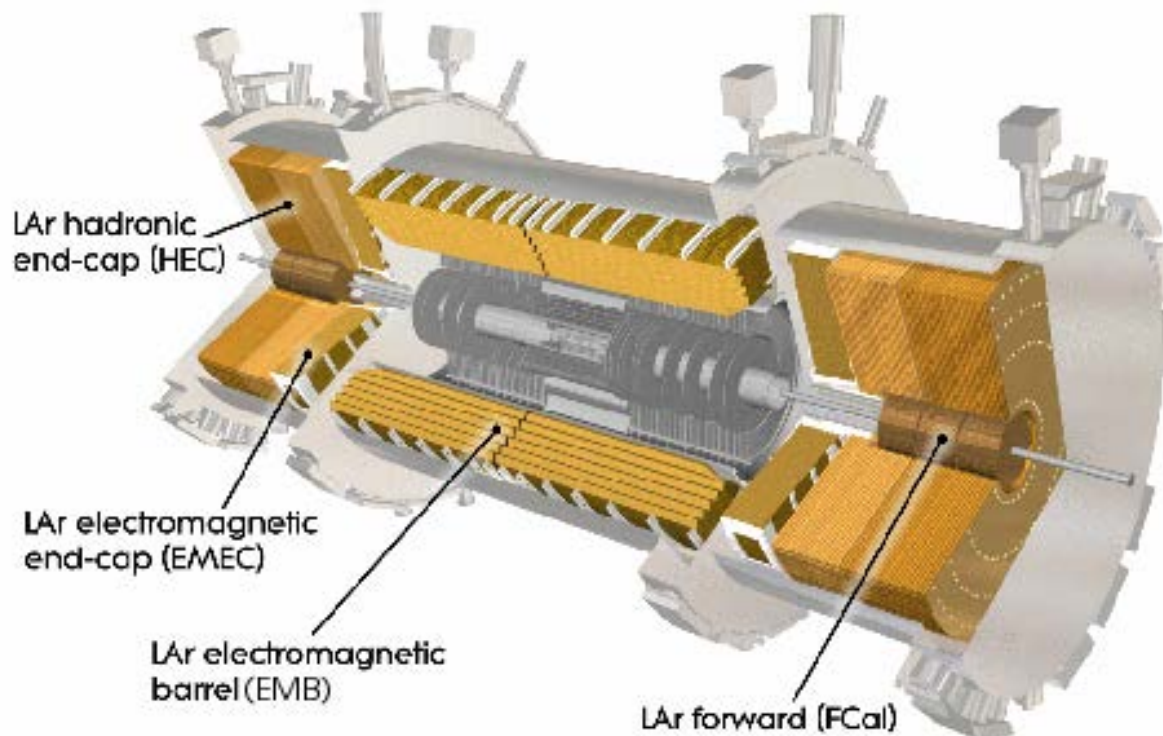
Context - LHC and ATLAS

- Large Hadron Collider (LHC) at CERN, Geneva, Switzerland
 - 27km circumference
 - depth between 50 to 175m
- A Toroidal LHC Apparatus (ATLAS)
 - 46m long, 25m diameter and 7000 tons
- Purpose:
 - Answer fundamental physics questions
 - Standard model

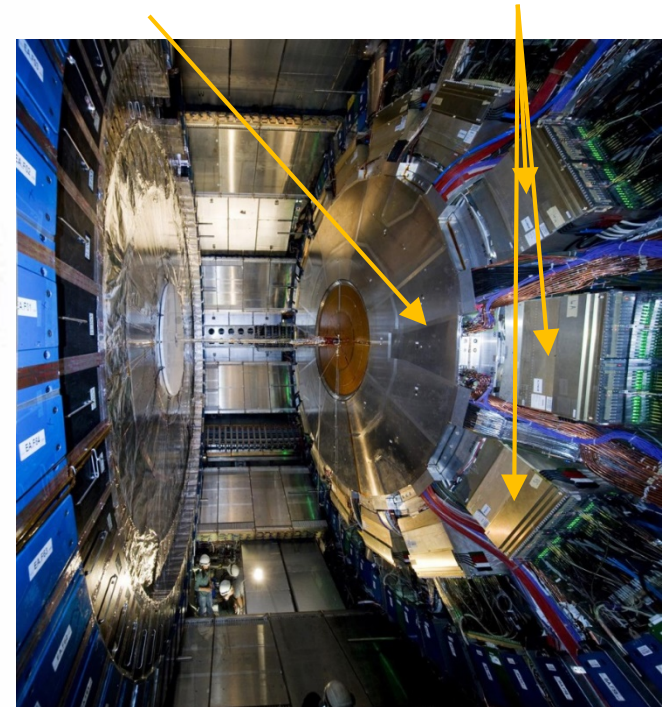


Context - ATLAS LAr calorimeter

- **180K channels** for the full readout of the electromagnetic (**EMB+EMEC**), hadronic (**HEC**) and Forward (**Fcal**) calorimeters
- **3K channels** for **analog Trigger** readout
- Front End crates: \approx **1600 Front End Boards (FEB)**
- Back End crates: **200 Readout Out Driver boards (ROD)**



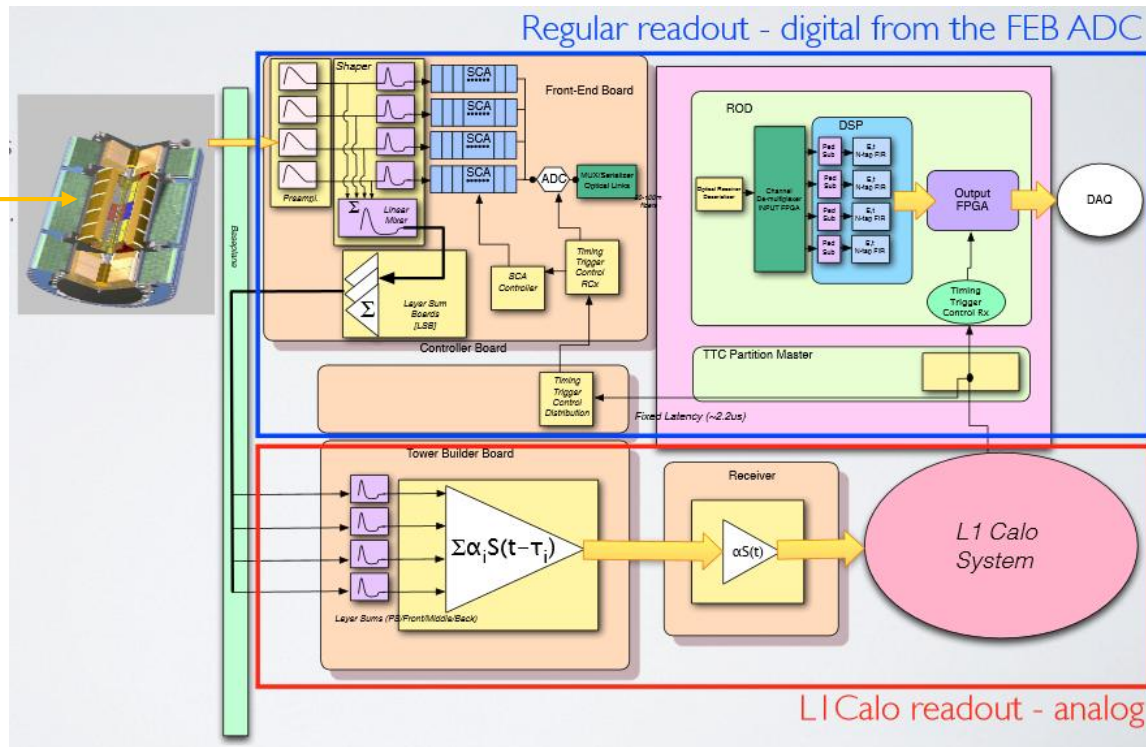
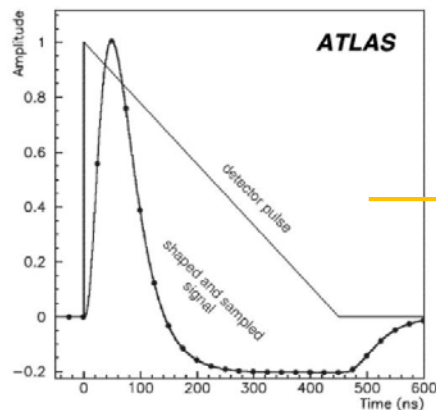
Calorimeter *Front End Crates*



Between Electromagnetic barrel and end-cap

Context - Current electronics

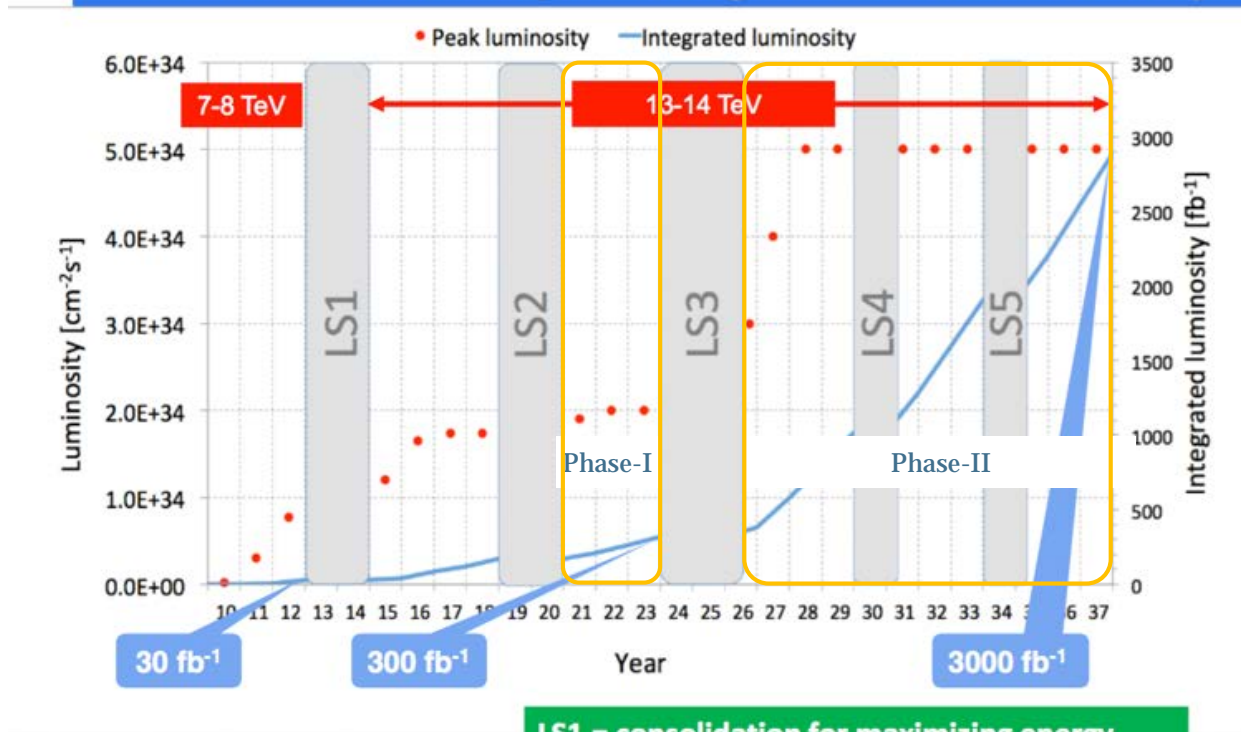
- **Regular readout:**
 - Cells signals are amplified, shaped, sampled at 40MHz, digitized and transmitted at 100kHz upon level-1 trigger
- **Trigger readout:**
 - Summing signals on **Layer Sum Board (LSB)** to form 0.1×0.1 ($\Delta_\eta \times \Delta_\phi$) trigger towers
 - **Tower Builder Board (TBB)** sums analog signals from **LSB** to send to **L1 Calo** system



Context - LHC Schedule

- Two phase upgrade planned for LHC, ATLAS upgrade:
 - Phase-I (2021-2023): upgrade of trigger path, installation in 2019-2020
 - Phase-II (after 2025): upgrade of data path, installation in 2024-2025

LHC roadmap: Integrated luminosity



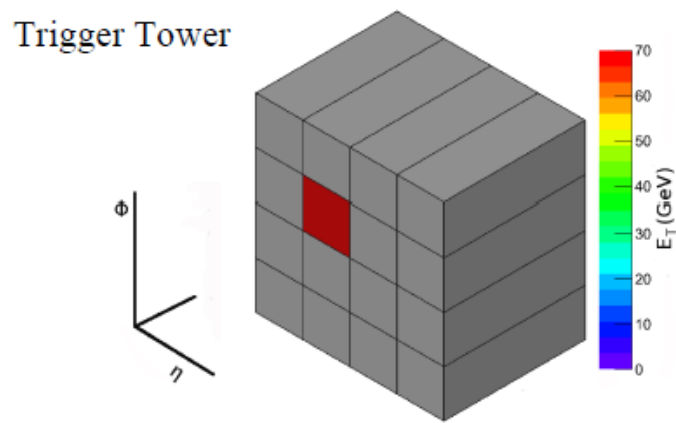
LS1 = consolidation for maximizing energy reach of the LHC (8 to 14 TeV)
 LS2 = LIU for beam intensity upgrade
 LS3 = HL-LHC for luminosity upgrade



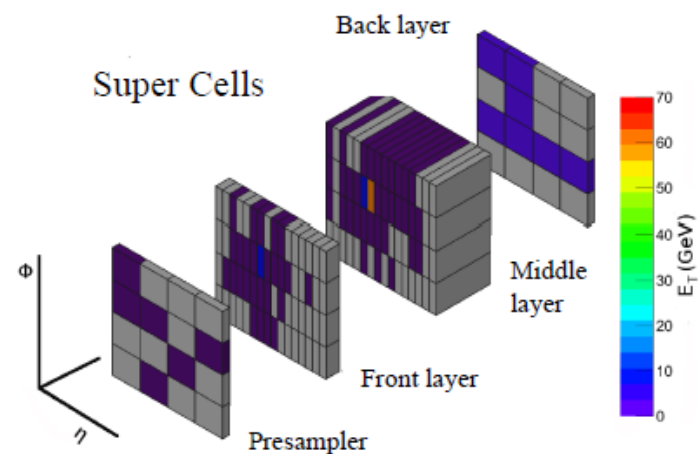
Status of LHC and HL-LHC
 EPS-HEP 2015 conference
 Frédéric Bordry
 27th July 2015

Context - Phase-I Upgrade

- Upgrade in Phase-I is for **trigger path**
- Current concept: **Trigger Tower**
 - Transverse energy (E_T) summed over an area of $\Delta_\eta \times \Delta_\phi = 0.1 \times 0.1$
- New concept: **Super Cell** to improve jet rejection using shower shape variables
 - Finer layer segmentation down to $\Delta_\eta \times \Delta_\phi = 0.025 \times 0.1$
 - Keep layer information
- Typically Trigger Tower corresponds to 60 standard cells and 10 Super Cells
- Super Cells digitized at **40MHz** on the new front-end board: **LAr Trigger Digitizer Board (LTDB)**



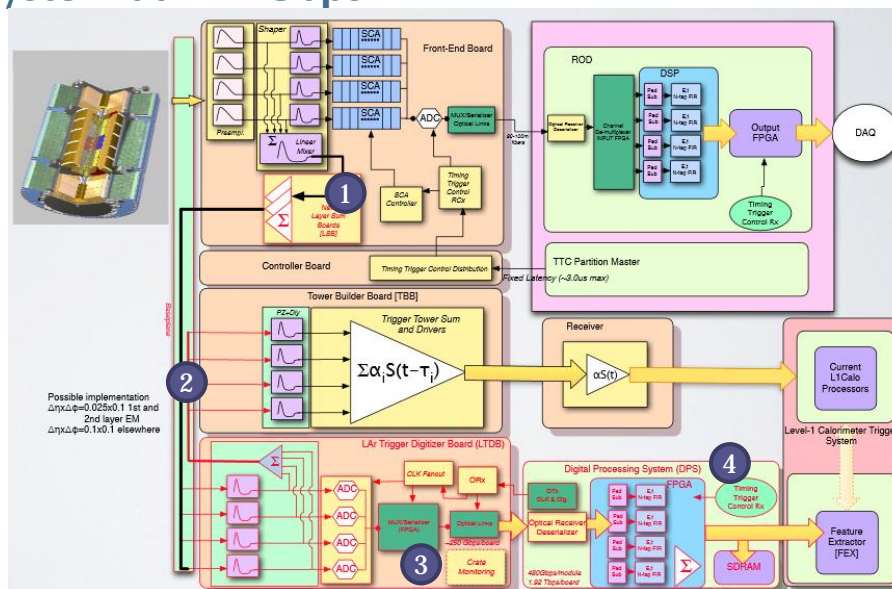
*70GeV electron shower
seen into only one Trigger Tower*



*70GeV electron shower
seen into multiple Super Cells*

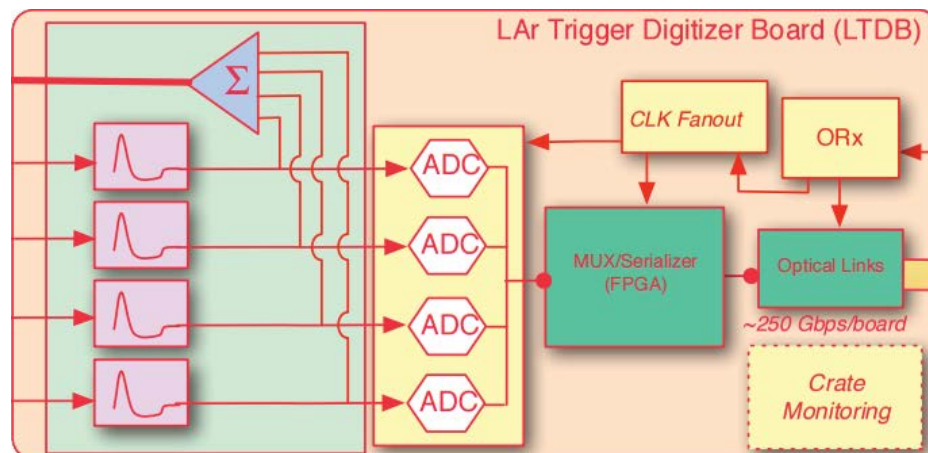
Context - Phase-I electronics upgrade

- Trigger data flow is replaced from analog to digital
- Front-end upgrade:
 1. **Layer Sum Boards (LSB)**: perform **analog sums** for Super Cells (SC)
 2. **Backplane** update: transports additional **analog sums**
 3. **LAr Trigger Digitizer Board (LTDB)**: digitizes **SC** data at **40MHz**, generates analog sums for current trigger system (compatibility), sends data to **LDPB** at **5.12Gbps**
- Back-end upgrade:
 4. **LAr Digital Processing Blade (LDPB)**: reconstructs **SC** transverse energy (E_T) and send to **L1A** Calo system at **11.2Gbps**



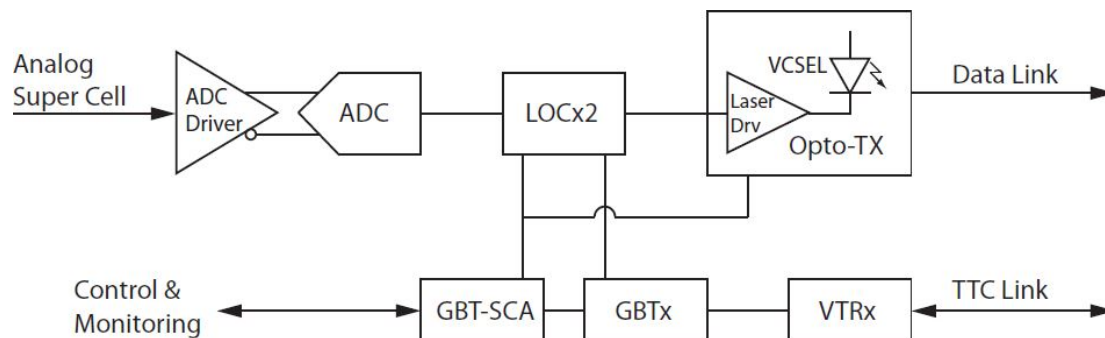
Front-end upgrade

LAr Trigger Digitizer Board (LTDB)



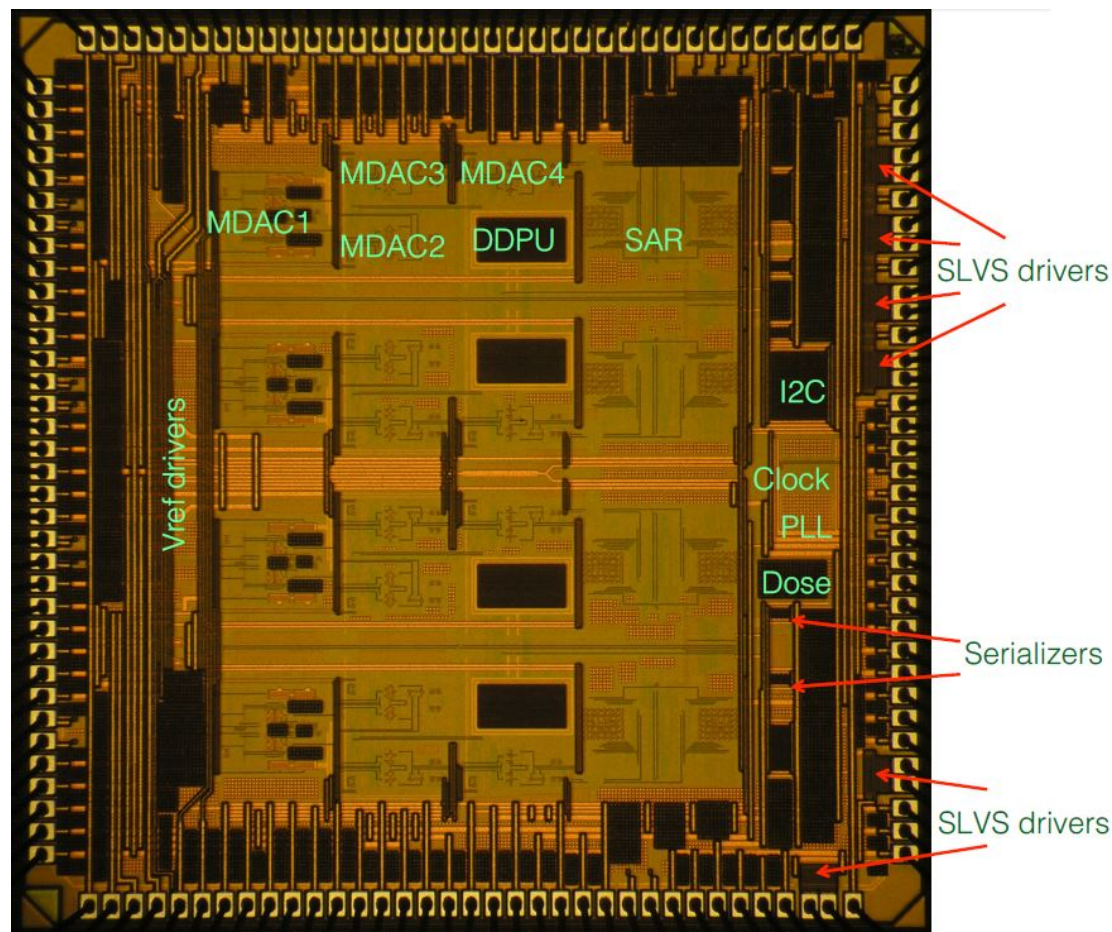
LTDB:

- **124 LTDBs** to readout the **34K Super Cells** of the LAr calorimeter
- 1 LTDB handles **analog input** from **320 Super Cells**
- **Digitizes** all analog signals at **12 bits @ 40MHz** using **80 custom ADC**
- Generate **analog sums** to keep **compatibility** with old system
- **Transmits** digital signals using **40 optical links @ 5.12Gbps** on custom ASIC
- Receives TTC clock and data through 5 GBTx links
- Design is made in collaboration between several groups
- **Phase-II compatible**
- **Key components** in development:
 - **LTDB pre-prototype board**
 - **Nevis ADC**
 - **LOCx2**
 - **LOCId**



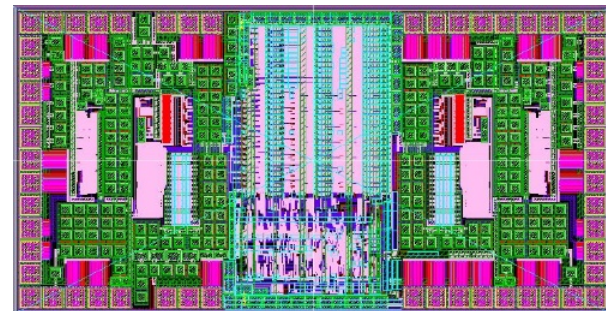
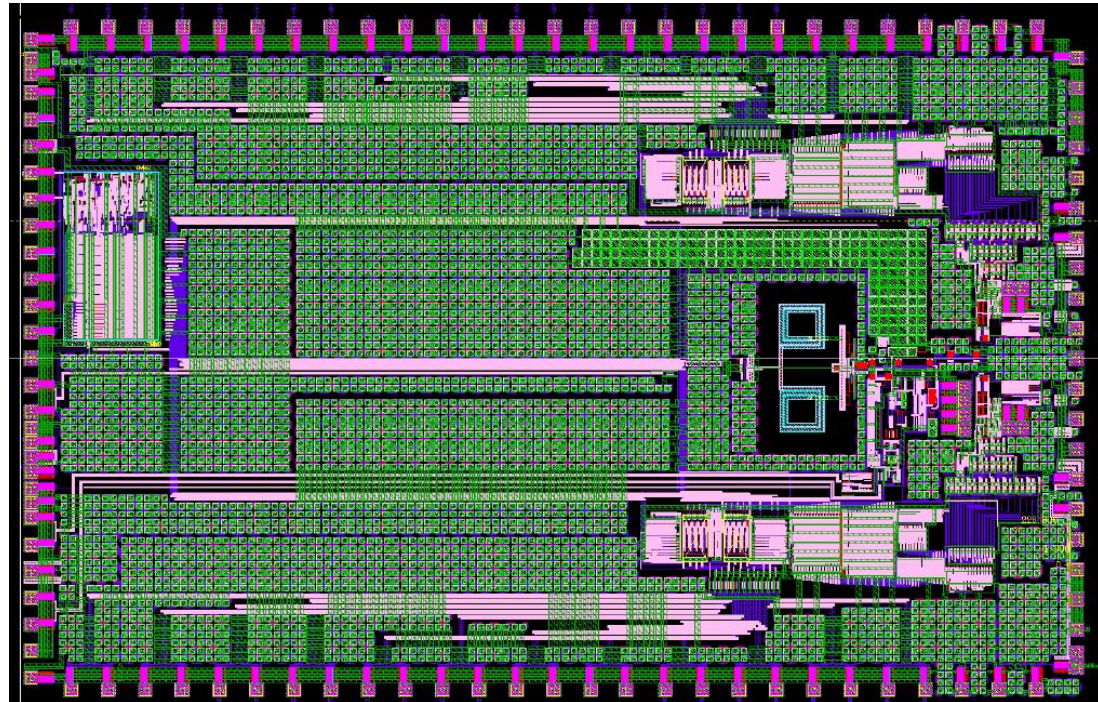
LTDB: Nevis ADC

- Quad 12 bits hybrid pipeline **SAR ADC** (IBM8RF 130nm CMOS)
- 40 MSPS
- $\text{ENOB} \geq 11$
- 45mW/channel
- 87.5ns latency
- **Radiation tolerant**
 - for the whole ATLAS lifetime
- Die:
 - 3.6x3.6mm
 - 72 pins QFN



LTDB: LOCx2/LOCld

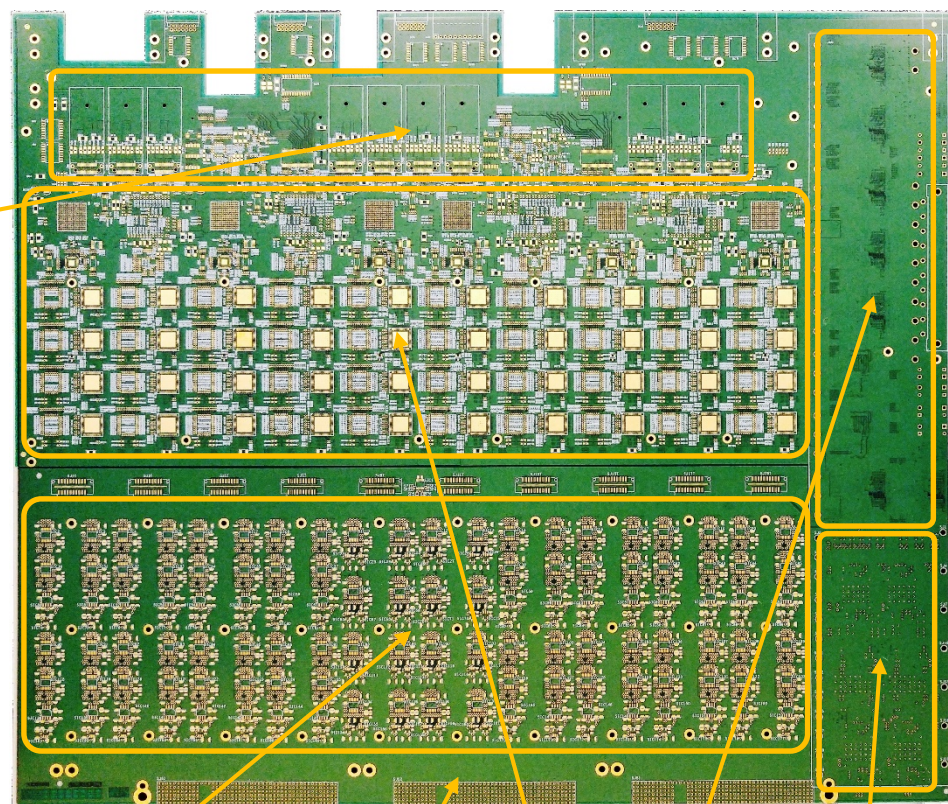
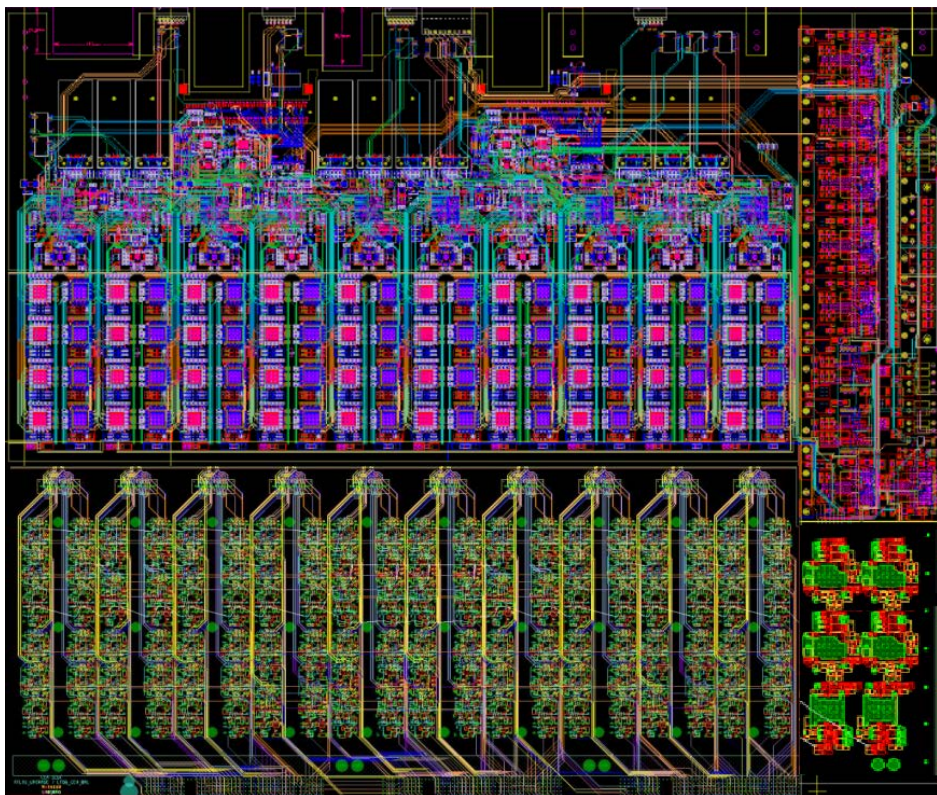
- LOCx2:
 - Dual 8*14 bits channel 5.12Gbps serializer
 - Nevis ADC compatible
 - Radiation tolerant
 - Die:
 - 6.036x3.68mm
 - 100 pins QFN
- LOCld:
 - Dual channel VCSEL driver
 - Radiation tolerant
 - Die:
 - 2.114x1.090mm
 - 40 pins QFN



LTDB:

- Pre-prototype PCB
 - FPGA used to replace LOCx2

10 SFP+ cages



Analog

Digital

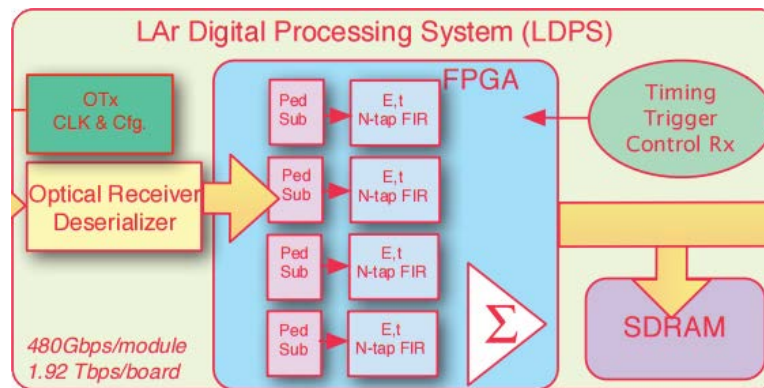
24 layers PCB

Timing and
slow control

Power

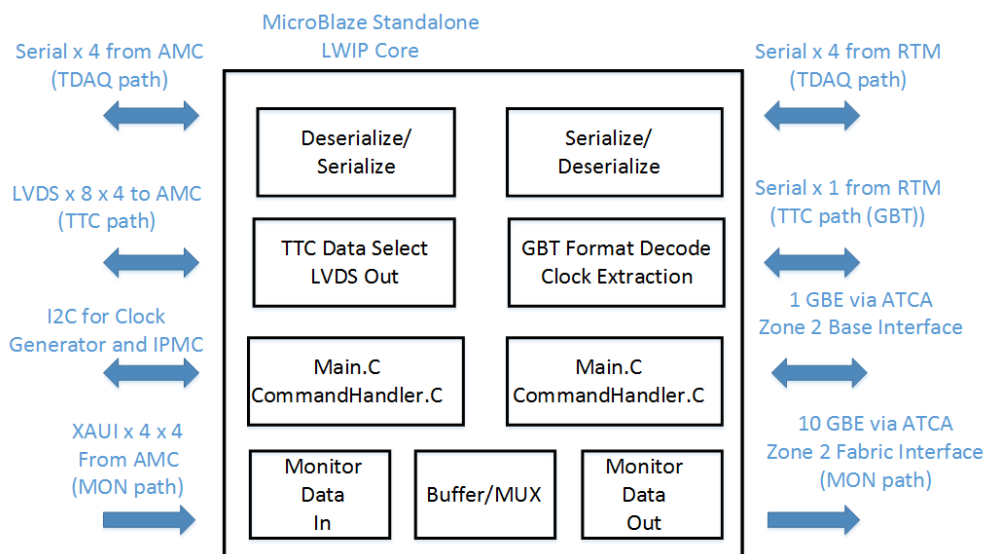
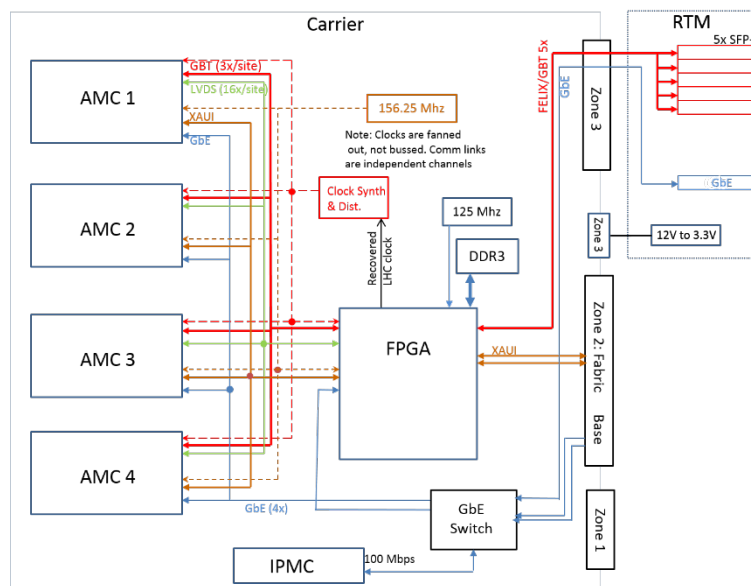
Back-end upgrade

LAr Digital Processing Blade (LDPB)

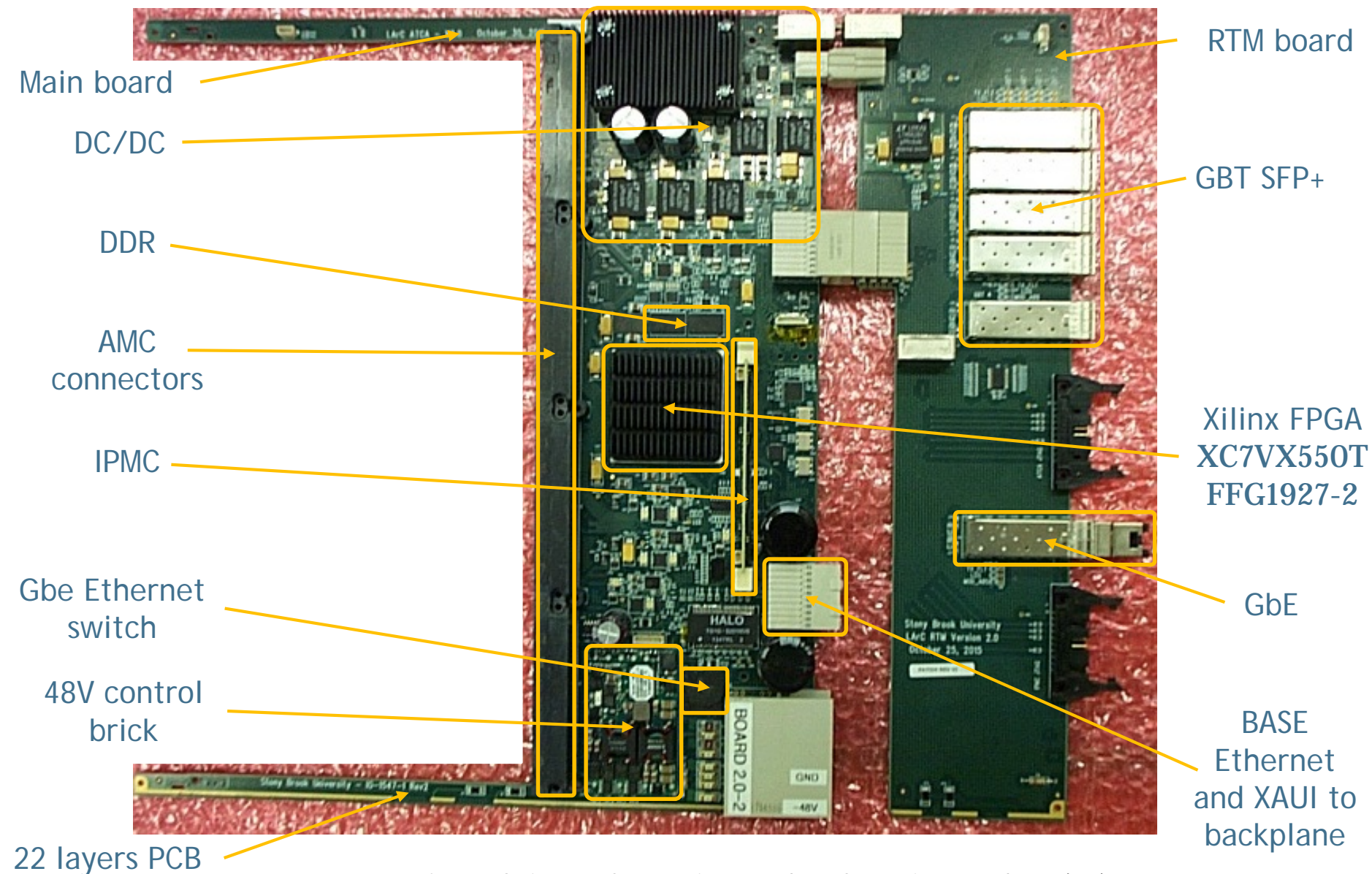


LAr Digital Processing Blade - LDPB

- **ATCA** carrier board for **4 AMC** mezzanines (**LATOME**)
- Brings **power** to **LATOME AMC** through **IPMC**
- Transmits **TTC** recovered **clock** and **data** from **optical links (GBT)** through **LVDS** links to all **4 LATOME AMC** boards
- Routes **GBT** and **XAUI** **monitoring** links from **LATOME** to **SFP+** cages on the backplane
- Connects all LATOME AMC boards to GbE ethernet network through dedicated switch

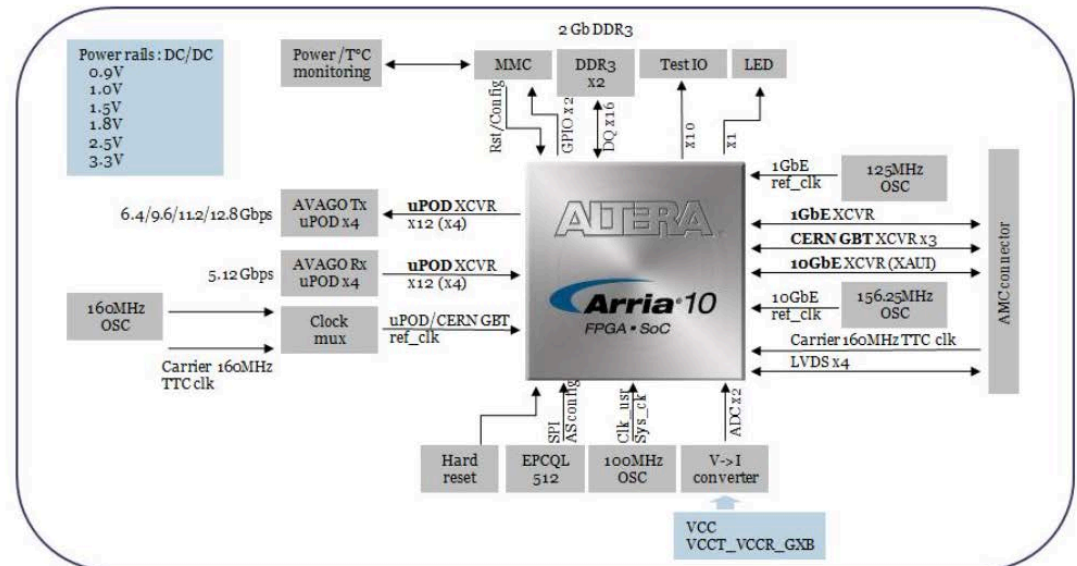


LDPB Carrier board

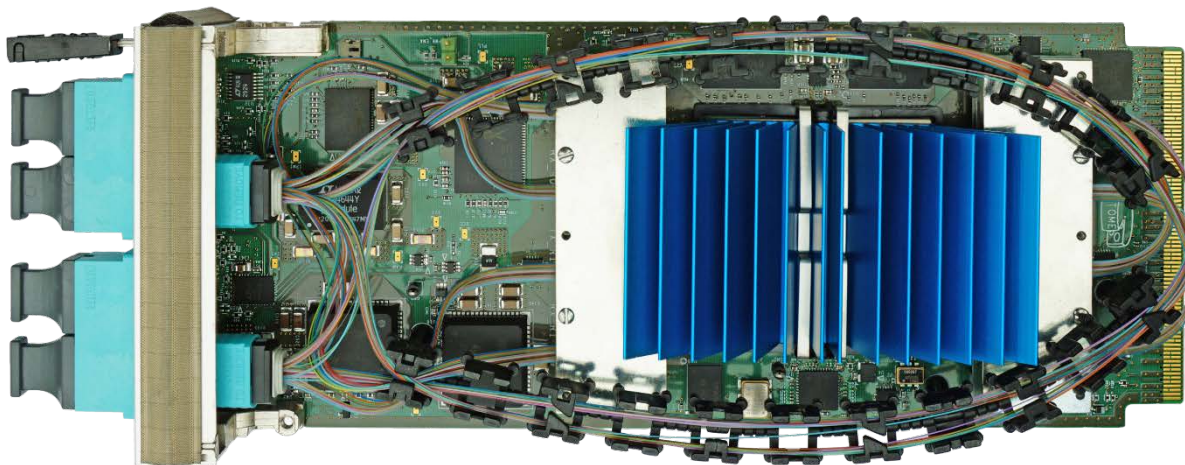
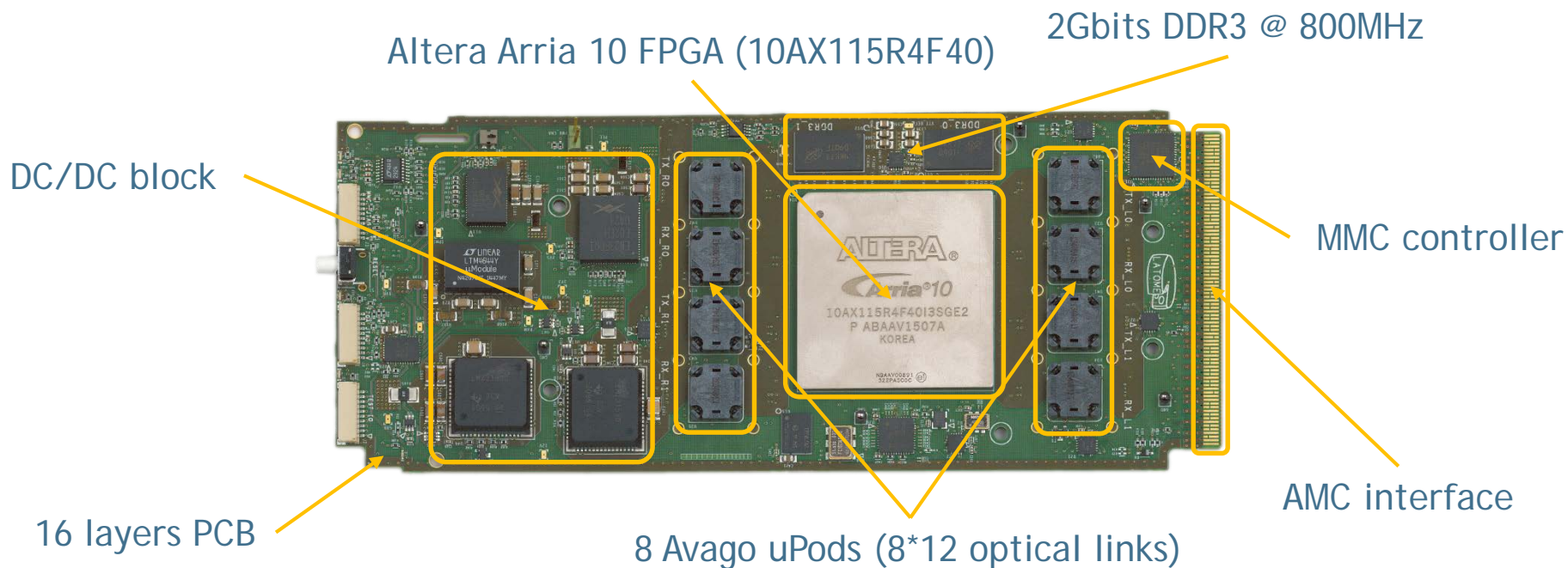


LAr Trigger prOcessing MEzzanine - LATOME

- Main data path:
 - Receives **Super Cell data** from **LTDB @ 5.12Gbps** on up to **48 optical links**
 - Computes **Super Cell transverse energy (E_T)** using **optimal filtering**
 - Builds **trigger tower transverse energy**
 - Sends trigger tower data **@ 11.2Gbps** on up to **48 optical links**
- Receives **TTC** clock and data on **LVDS links**
- **Monitors data** and send to **TDAQ system** upon request on **10GbE network**
- System is **fixed latency** less than **15BC=375ns**
- **80W** power budget

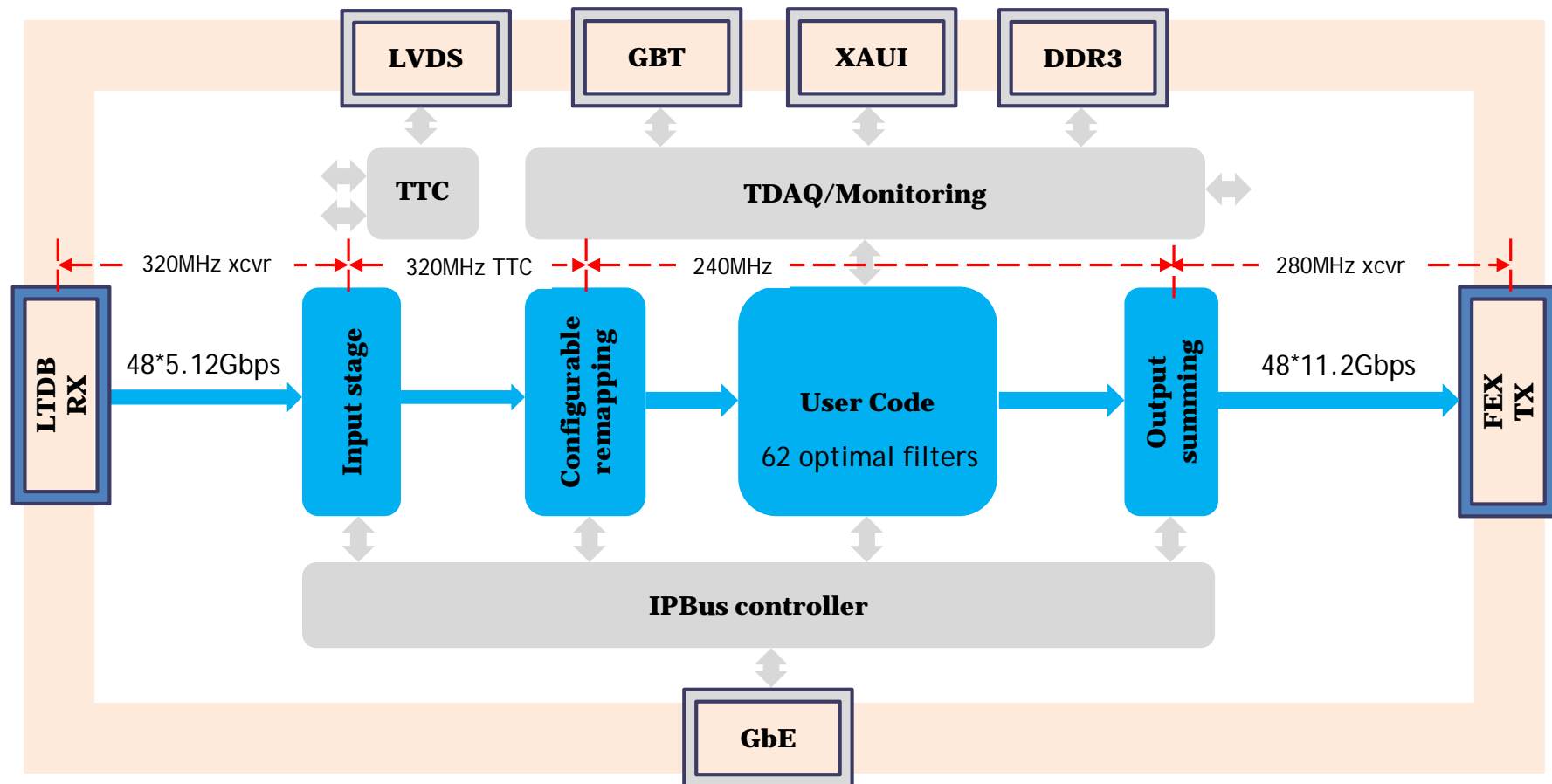


LATOME - Hardware



LATOME - Firmware

- Input stage: align all input fibers together
- Configurable remapping: reorder input data according to detector topology
- User code: computes ET using optimal filtering
- Output summing: builds trigger tower energies



Demonstrator

Demonstrator - Motivation

- Collect data from the Super Cells
- Validate energy reconstruction and bunch crossing identification algorithms in FPGAs
- Measure trigger efficiency and jet background rejection
- Learn about installation and operation of the apparatus in the ATLAS environment

Front-end demonstrator - LTDB

- Handles up to **320 Super Cells** signals
 - **284 Super Cells** in EM Barrel
- **Super Cells** signals are **digitized** with **12bits ADC@ 40MHz**
 - **Commercial ADC COTS** : TI ADS5272 (not radiation tolerant)
- Multiplexing of **8 Super Cells** on one **4.8Gbps optical link**
 - 8B10B encoding, K code sent every Bunch Crossing
 - FPGA (XILINX/ALTERA)
 - **40 optical links**
- Throughput $\approx 200\text{Gbps/LTDB}$
- Status:
 - **2 LTDBs installed** in August 2014
 - **Taking collision data in LHC Run 2**



Digital part

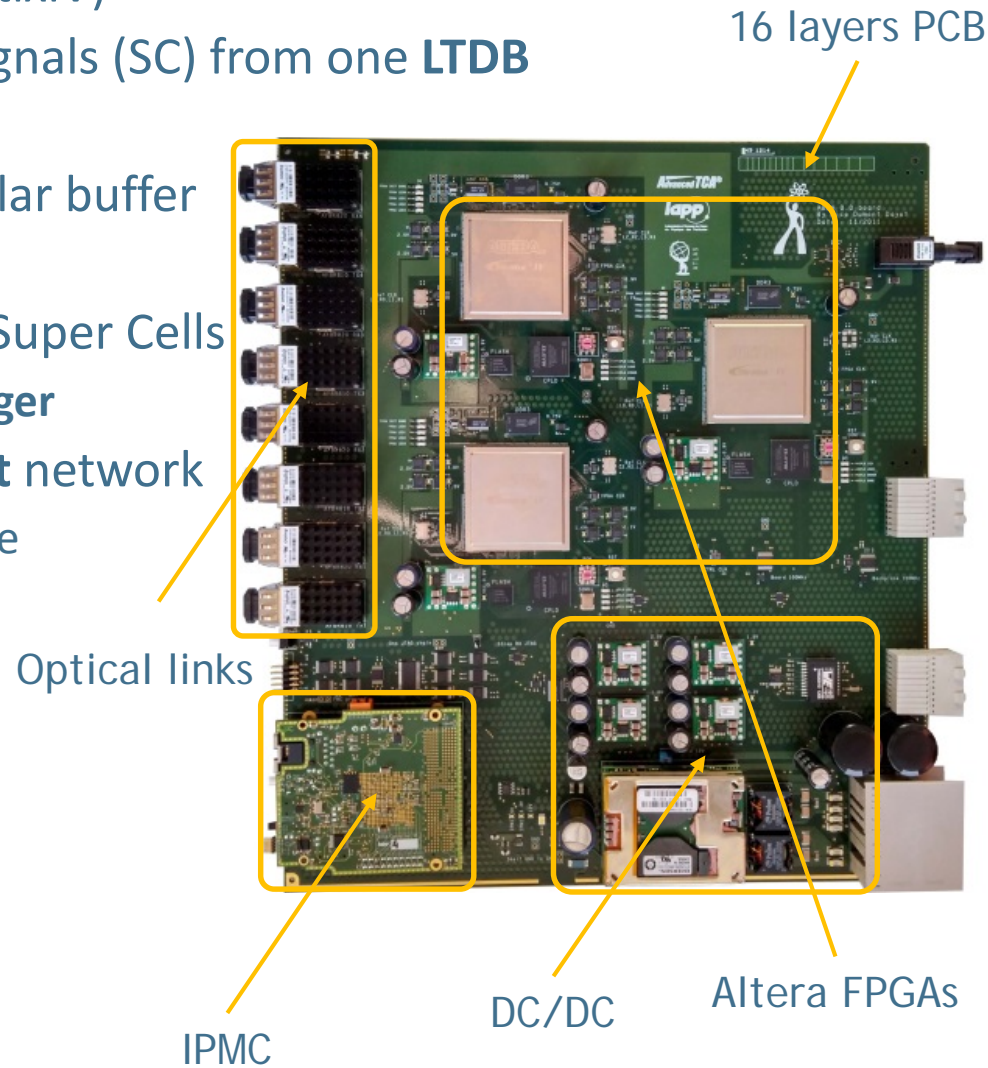


Analog part

LTDB boards (490x410mm)

Back-end demonstrator - LDPB - ABBA

- **ATCA board:** 3 Altera FPGAs (StratixIV)
- Receives up to **320 Super Cells** signals (SC) from one **LTDB**
 - **48 optical links @ 4.8Gbps**
- **Stores Super Cells** data into circular buffer
 - Latency up to 2.5us
- **Waits for TTC trigger** to readout Super Cells
 - Readout with **filtered Level-1 trigger**
- **Readout through 10GbE Ethernet** network
 - Readout with ATCA fabric interface
- **Status:**
 - **2 ABBA boards installed**
 - **Online software** has been set
 - **Taking collision data in LHC Run 2**
 - **Performance as expected**



Demonstrator - Installation in ATLAS

UX15



LTDBs in front-end crate

USA15

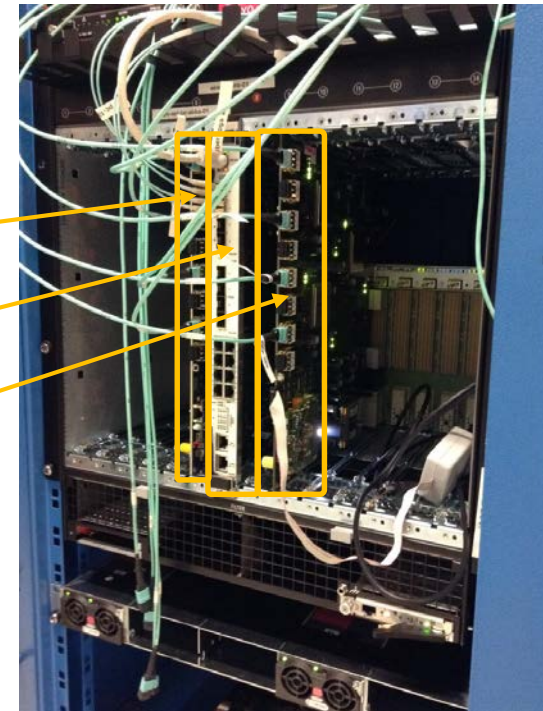


Readout computer (10GbE)

ABBA board n° 1

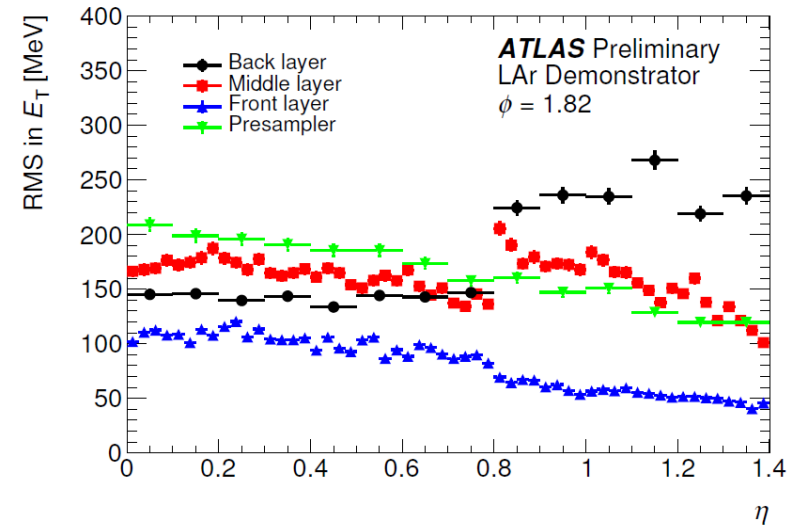
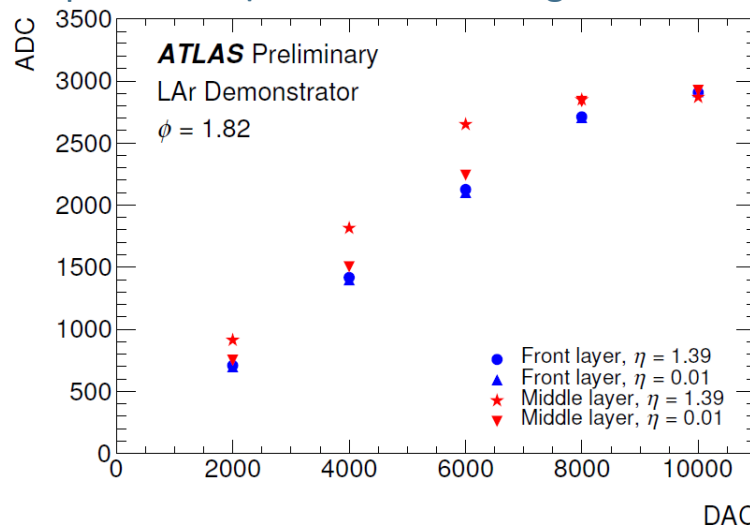
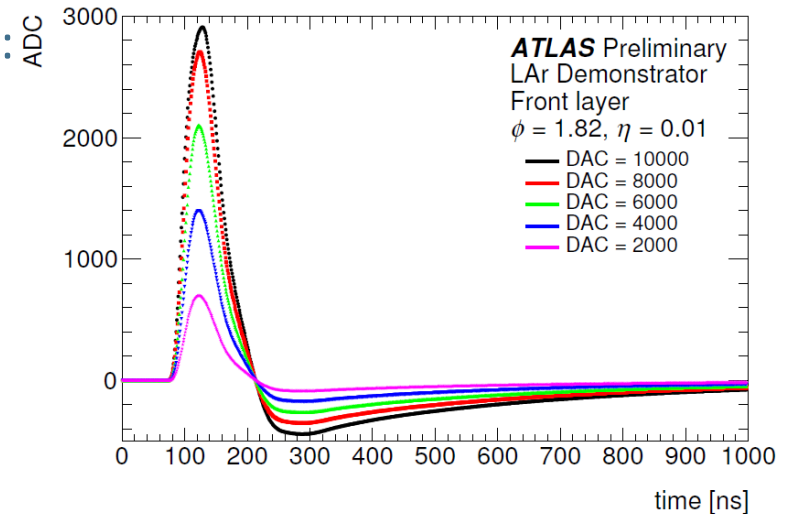
10GbE ethernet switch

ABBA board n° 2



Demonstrator - Results

- Pulse sent through **calibration board**
- Readout through the **complete DAQ chain**:
 - FEB → LTDB → ABBA → TDAQ software
- Results:
 - **Pulse shape** for several signal amplitudes (DAC)
 - **Linearity**:
 - Saturation of analog part ~ 10000
 - **Noise**: (RMS of DAC pedestal)
 - Jump seen at $\eta=0.8$ due to change of material



Conclusion

Conclusion

- A part of the new Trigger scheme (Demonstrator) has been installed
 - Both Front End and Back end electronics have been validated
 - One Front End Crate (1/32) is equipped with the demonstrator
 - Readout through TDAQ software
- Measurements have been done with this new Trigger chain
 - Does not affect the current system : no additional noise
 - Does not disturb the current readout system : works in parallel
 - Pulses shapes have been checked with Calibration runs
- LTDB and LDPB systems are being developed
 - Radiation tolerant ADC and Optical links specifically designed
 - LTDB pre-prototype being assembled
 - LDPB ATCA carrier board and LATOME AMC boards being tested
- Production will start in 2017-2018