



Contribution ID: 197

Type: Oral presentation

A Programmable Read-out chain for Multichannel Analog front-end ASICs

Tuesday, June 7, 2016 10:00 AM (20 minutes)

In this contribution we introduce an innovative multiplexed ASICs read-out system based on 32 analog channels sampling at 40 MHz with 12 bits resolution and 96 digital I/O with selectable voltage standard ranging from differential signaling and 1.8 or 3.3 V CMOS. The ADCs and ASICs read-out is managed by a Kintex-7 FPGA and the communication with the host computer relies on the fast USB 3 communication protocol. The main feature of this system is the new idea of FPGA firmware development based on an easy to use graphical interface, which is able to carry out all the requested functions for an ASIC read-out system (for instance state machines, triggers, counters, time delays, and so on..), without the need to write any Hardware Description code. Furthermore, we also introduce a cloud compiling service, which allows the user to avoid to install the FPGA development environment to create a measurement setup based on this read-out system.

Primary authors: Mr CUSIMANO, Alberto (Nuclear Instruments); Mr ABBA, Andrea (Nuclear Instruments); Mr CAPONIO, Francesco (Nuclear Instruments)

Presenter: Mr CAPONIO, Francesco (Nuclear Instruments)

Session Classification: DAQ 1 / Front End Electronics

Track Classification: Front End Electronics and Fast Digitizers