Contribution ID: **141** Type: **Poster presentation**

FPGA baseline restorer based on high-speed ADC in particle emission rate measurement system

Friday, June 10, 2016 10:30 AM (1h 35m)

A baseline restorer has been implemented with FPGA in 2πα and 2πβ particle emission rate measurement system. The signal of the detector was digitalized by 100MHz ADCs before transferred into the FPGA. The data was transformed into first-order differential and second-order differential data flow in the FPGA for the discrimination of the baseline voltage. The original data and restored data were uploaded to the PC in real-time with only dozens of cycles' delay. Comparison was made by the plots of signal wave for both original data and restored data. And the influence to the emission rate was also discussed. Results indicated that the FPGA baseline restorer was successfully achieved with little distortion of signal wave and it made help to reduce the error counts.

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Session Classification: Poster Session 2

Track Classification: Data Acquisition