



Contribution ID: 3

Type: **Poster presentation**

Design of ultra-low noise power system for high-precision detectors

Friday, 10 June 2016 10:30 (1h 35m)

In most nuclear physics and particle detection experiment, the detection precision usually needs to be very high, especially for detection of weak signal. To meet the requirement of high-precision and low-noise signal readout, the detector system need very high signal to noise ratio (SNR). For this reason, the background noise of the system need to be very low, hence an ultra-low noise power supply system is important and necessary. As an example, in the scientific CCD detector system, the readout noise of CCD is about as low as $5e^{-}$ /pixel. So it is important for the system to be provided with high-precision and low-noise power.

Scientific CCD detector systems are widely used in many areas as high-energy physics, nuclear physics and astronomy for its high quantum efficiency and low readout noise. For example, soft-x-ray CCD imaging, dark matter search based on CCD, astronomical optical band CCD imaging, infrared CCD camera, and especially for some experiments of high-energy physics and nuclear physics, could gain benefits from ultra-low noise readout of scientific CCD systems. Commonly for achieving the ultra-low noise readout, the driving signals for the CCD chip must be very clean as the noise of the bias signals need to be under $40\mu V_{rms}$.

In this paper, we introduce an ultra-low noise power system designed for the scientific CCD detector. Our power system uses power adapter or linear power of 24V as a power input, then generates low noise power outputs for the front-end electronics (FEE) of the detector system. The FEE mainly includes three parts, one is the clocks and biases circuit for driving the CCD, the second is the CCD signal processing circuit and ADC circuit for sampling the CCD outputs. The SNR of this two parts must be very high. Commonly the power noise of the biases circuit and the CCD signal processing circuit need to be under $40\mu V_{rms}$, the power noise of the clocks circuit could be a little higher as about $1mV_{rms}$. The third part is the digital controlling circuit including FPGA, clock chip and USB interface chip etc., the power noise requirement of which is just about $1mV_{rms}$.

Besides, some experiments as astronomical optical band observation or measurement of infrared sky background are hoped to done in some special geographical environments as in Antarctica where there is polar day and night, the air is thin and dry, but the temperature is as low as 193K. However, the general commercial electronic equipment rarely give careful consideration to the work performance and stability with operating temperature of 213K-193K. So when our power system is designed, the influence of low temperature environment is full considered. The system could satisfy the need of long time working in the low temperature condition as in Antarctica.. With fully tests, the system shows stable and continuous work in the simulation environment as low as 193K.

Primary author: WANG, Jian (Univ. of Sci. & Tech. of China)

Co-authors: Mr YANG, Dong-xu (Univ. of Sci. & Tech. of China); Dr ZHANG, Hong-fei (Univ. of Sci. & Tech. of China); Mr WANG, Jian-min (Univ. of Sci. & Tech. of China); Mr LIN, Sheng-zhao (Univ. of Sci. & Tech. of China); Mr FENG, Yi (Univ. of Sci. & Tech. of China)

Presenter: WANG, Jian (Univ. of Sci. & Tech. of China)

Session Classification: Poster Session 2

Track Classification: Front End Electronics and Fast Digitizers