Design of the Readout Electronics Prototype for LHAASO WCDA

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***Abstract*-In the Large High Altitude Air Shower Observatory (LHAASO), the Water Cherenkov Detector Array (WCDA) is one of the major detectors. The WCDA electronics are responsible for the readout of 3600 Photomultiplier Tubes (PMTs), and a total of 400 Front End Electronics (FEE) modules are required. The main challenges in the WCDA readout electronics design include: precise time and charge measurement over a large dynamic input amplitude range (1 Photo Electron (P.E.) ~ 4000 P.E.), high quality of clock distribution and automatic clock phase compensation, and high speed data transfer due to the requirement of "triggerless" architecture. In this paper, we present the prototype design of the readout electronics for the LHAASO WCDA. We also conducted tests on the prototype electronics to evaluate the performance. The results indicate that a charge resolution better than 15%@ 1 P.E. and 2%@ 4000 P.E., and a time resolution better than 0.3 ns RMS are successfully achieved over the whole dynamic range, beyond the application requirement.**

I. Introduction

WATER Cherenkov Detector Array (WCDA) [1]is one of the key parts in the Large High Altitude Air Shower Observatory (LHAASO), in which 3600 Photomultiplier Tubes (PMTs) are scattered in an area of 90000 m^2. [2] The main challenges in the WCDA readout electronics design include: [3]
1) precise time and charge measurement over a large dynamic range from 1 to 4000 Photo Electrons (P.E.);
2) mixed transmission over the same fiber for data, commands, and the clock signal, in order to simplify the system architecture considering the large scale of detector node distribution;
3) high quality clock distribution and automatic compensation with varying ambient temperature.

To address the above issues, several versions of circuit design and tests were conducted, and finally a prototype of the readout electronics was finished, which is presented in the following sections.

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II. System Design

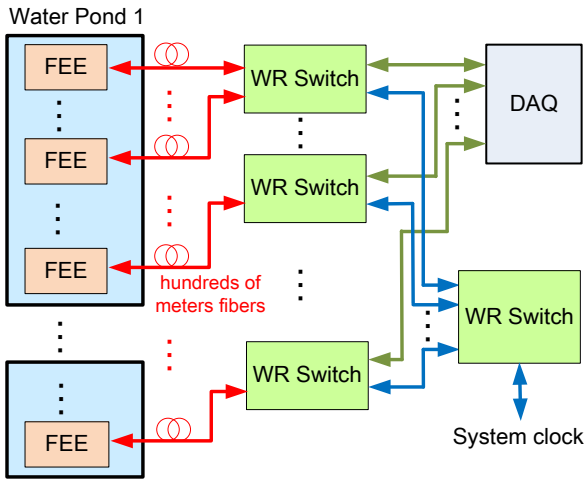

Fig. 1. Architecture of the readout electronics for WCDA.

The structure of the readout electronics for WCDA is shown in Fig. 1. The clock signal from the clock system of LHAASO is distributed by fibers to Front End Electronics (FEE) nodes through White Rabbit (WR) switches. Based on the WR principle [4-7], we proposed an enhanced clock phased compensation method to automatically align the clocks received at different FEEs [8]. The data from FEEs are transferred via the same fiber paths to DAQ based on TCP/IP protocol due to "triggerless" requirement.

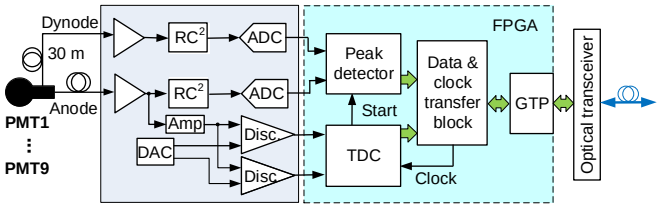

Fig. 2. Block diagram of the FEE.

Fig. 2 shows the block diagram of one FEE. Each FEE is responsible for the readout of 9 PMTs. The signals from the anode and dynode from each PMT are processed by the FEE to cover a large dynamic range from 1 to 4000 P.E. As for charge measurement, the input signal is amplified and then converted to a quasi-Gaussian signal by an RC^2 filter with a time constant of 40 ns. The output of shaper is digitized by Analog-to-Digital

Converters (ADCs) with a sampling frequency of 62.5 MHz; combined with the digital peak detection algorithms in the Field Programmable Gate Array (FPGA) device, the charge information can be obtained. The key parameters such as filter order, time constant, and sampling rate are optimized through analysis and simulation based on pspice and MATLAB. As for time measurement, the anode signal is also fed to discriminators and digitized by FPGA-based Time-to-Digital Converters (TDCs). Discriminators with two thresholds are employed to avoid deterioration of time measurement resolution which would be caused by noise or interference in the baseline of the large input signal from the PMT. The input of the TDC is also used as the "start" flag for the digital peak detector block. The PMT signals are transmitted to the FEE through 30-meter cables, so high precision impedance matching is also necessary due to the large dynamic range.

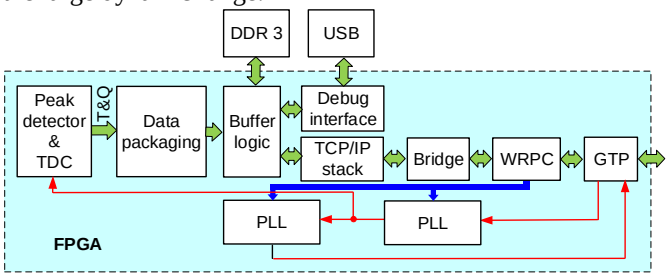

Fig. 3. Block diagram of the data & clock transfer block.

Fig. 3 shows the block diagram of the data and clock transfer block. Due to the requirement of "triggerless" architecture, all the data need to be read out to the DAQ, and data transfer based on 1000 M Ethernet and TCP/IP protocol is required. Meanwhile, since the 3600 PMTs are scattered in a 90000 m^2 area, the long distance of signal transmission would cause clock phase alignment mismatch between different FEEs. Besides, the temperature variation at high altitude should also be considered. In the design of the readout electronics, we proposed an enhanced automatic clock phase compensation technique based on the original WR principle. The basic idea is to measure the delay fluctuation in real time, and adjust the clock phase at FEEs based on a new method to decide the delay increment of the upwards (from FEE to WR switch) and downwards (from WR switch to FEE) directions. To simplify the hardware and guarantee a good symmetry between the upwards and downwards paths, the PLL inside the Artix-7 FPGA is employed, and a delay adjust step size of 15 ps can be achieved. We use the SiTCP core for TCP/IP data packaging, and White Rabbit PTP Core (WPRC) is employed to be compatible with the standard WR switches. A data interface is designed to bridge between these two cores.

To simplify the system structure, clock, data, and commands are mixed together, and transmitted through the same fiber (300~ 400 meter).

III. System Performance Test

We have finished the design of the readout electronics prototype, and conducted tests to evaluate the system performance.

A. Charge and Time Measurement Performance Test

In this test, we used a signal source (Tektronix AFG3252) to generate the input signal according to the signal waveform of the PMT, and this signal is transmitted to the FEE through a 30-meter cable. By changing the input amplitude with an attenuator (WAVETEK 5080.1), the performance can be obtained in the input amplitude range from 1 to 4000 P.E.

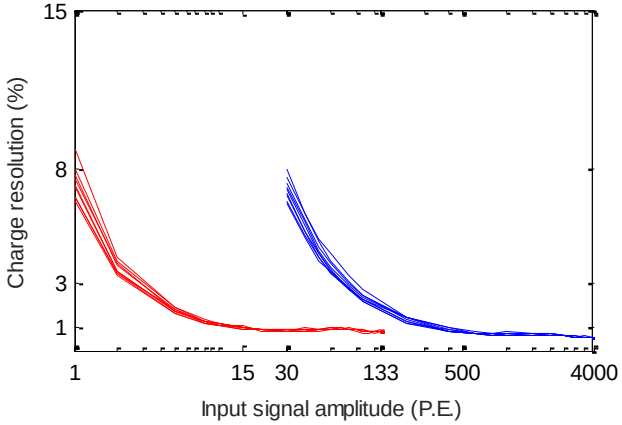

Fig. 5. Charge resolution test results.

Fig. 5 shows the charge resolution test results, which indicate that the charge resolution is better than 15% @ 1 P.E. and better than 2%@ 4000 P.E., well beyond the application requirement (30%@ 1 P.E. and 3%@ 4000 P.E.).

Time resolution test results are shown in Fig. 6, and a time resolution better than 0.3 ns RMS is achieved in the whole range from 1 to 4000 P.E., also beyond the required 0.5 ns RMS.

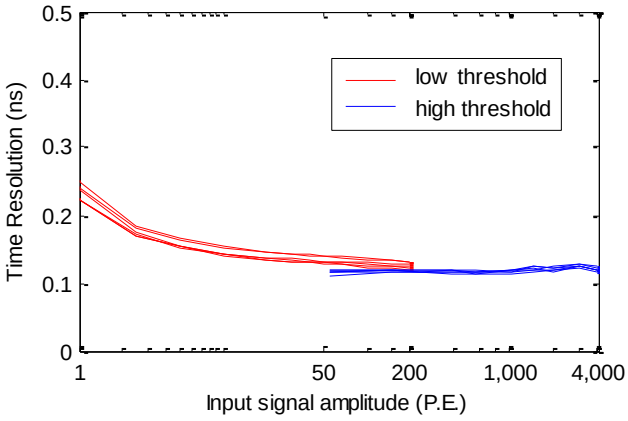

Fig. 6. Time resolution test results.

B. Clock Compensation Test

We also conducted tests to evaluate the clock compensation performance. In this test, we placed one FEE and the 400-meter fiber between the FEE and WR switch in a climate chamber to vary the ambient temperature, and another FEE was in a stable room temperature. By observing the difference of the time measurement results of these two FEEs, the clock compensation

performance can be obtained. As shown in Fig. 7, the compensation precision is better than 100 ps in the temperature range of 70 ºC.

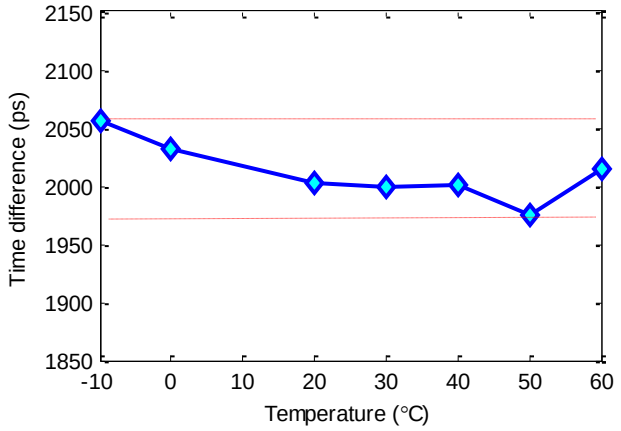

Fig. 7. Clock phase compensation performance in the temperature range from -10 ºC to 60 ºC.

IV. CONCLUSION

A prototype of the WCDA readout electronics was designed, which features a large input dynamic range, high precision automatic clock phase compensation, mixed transmission of clock, data, and commands, etc. Tests were also conducted to evaluate its performance, and the results indicate that this prototype has successfully achieved a charge resolution better than 15@ 1 P.E. and 2%@ 4000 P.E., a time resolution better than 0.3 ns RMS in the whole range, as well as a clock compensation precision better than 100 ps in a 70 ºC temperature range, beyond the application requirement.

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