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Low Phase Noise Local Oscillator and Clock Generation for Cavity Field Detection

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When designing Low-Level RF (LLRF) system for the new generation of Free-Electron Laser (FEL) machines there are many considerations. First is superior performance of the front-end electronics focused on ultra-low phase noise which contributes to the quality of the electromagnetic field of superconducting RF cavities in accelerating modules, stability of accelerated electron bunches arrival time and finally to the output laser light of FEL. Other important goals for LLRF system are drift minimization, remote control and diagnostics, high reliability and serviceability. This can be achieved introducing to all subsystems highly integrated PCB modules that can accommodate all the system requirements. One of the crucial subsystems of the LLRF front-end is Local Oscillator (LO) generation and Clock (CLK) generation which are a subject of this article. The cavity probe signal of frequency 1300 MHz is mixed with ultra-low phase noise LO signal 1354 MHz and downconverted to an intermediate frequency (IF) of 54 MHz. This lower frequency IF signal holds the original amplitude and phase information of the field inside the cavity. The IF signal is sampled by analog-to-digital converter (ADC) with 81 MHz low jitter CLK and processed by digital part of the LLRF. The cavity field detection critically influences the regulation of the acceleration field. That is why phase noise performance of the LO and CLK signals is of our interest here. This is even more critical when vector sum of probe signals from multiple cavities is calculated and used for field regulation. In this paper different LO and CLK generation schemes have been presented and discussed. Performance and small form factor for PCB integration were of our interest. Phase-lock loop (PLL) based technique and mixing technique were considered the most promising for LO generation. Technologies limits where performance and the size of VCO's and LO filters are in tradeoff have been met. Low jitter CLK generation circuit optimization has been described. 2 DUT phase detector test methodology has been used to measure residual phase noise of different LO and CLK generation circuits. Circuit of the best performance has been chosen for the final realization. Results at the level of single femtoseconds of the residual integrated RMS time jitter have been achieved. Based on that a family of LO and CLK generation modules has been developed.

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