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A VXS [VITA41] Trigger Processor for the 12GEV Experimental Programs at Jefferson Lab

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Now that the 12GeV experimental program at Jefferson Lab is successfully underway in Hall D (GlueX experiment) a new version of the trigger processor has been designed and will be commissioned in the CLAS12 experiments starting in the fall of 2016. The new trigger processor is a second generation development and combines the functions of two current modules, the Crate_Trigger_Processor[CTP] and Global_Trigger_Processor[GTP]. The new board, called the VXS_Trigger_Processor[VTP], will be used in front end and global trigger VXS crates. In front-end crates it can receive and process trigger information from a variety of existing Jefferson Lab modules over the VXS backplane (64 full duplex lanes at up to 8.5Gbps each): up to 256 channels of flash ADC, up to 1536 channels of discriminated drift chamber hits, and up to 16384 channels of silicon vertex tracker hits. Cluster and track reconstruction is performed on the Virtex 7 FPGA and the results are sent to the Sub_System_Processor[SSP] in the global trigger crate using up to 4 of the QSFP transceivers (up to 34Gbps each). In the global-trigger the VTP will perform final high level trigger decisions (detector coincidence/geometry matching) based on the trigger information it receives from up to 16 Sub_System_Processor[SSP] modules that each receive up to 8 VXS crates each for a total capacity of 128 front-end VXS crates. Additionally, the VTP uses a 1GHz Zynq SoC processor to provide a configuration, control, and diagnostic Ethernet interface. The Zynq contains a 40Gbps Ethernet interface that will be combined with a hardware accelerated TCP/IP stack residing in the programmable logic section of the chip. In the future the 40Gbps interface will be used for front-end module readout, eliminating the use of the VME64x/2eSST interface which operates at a much lower rate of 200MB/s. This readout upgrade is intended to provide flexibility for future data hungry experiments or level 3 CPU/GPU farm triggers. This paper details the hardware performance, implementation and some of various trigger algorithm requirements and implementations for the CLAS12 experiment.

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