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# Operational Experience with the Readout System of the MINOS Vertex Tracker

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The MINOS vertex tracker is a compact instrument built for in-beam spectroscopy of exotic nuclei. Its main component is a ˜30 cm long hollow cylinder shape time projection chamber (TPC) surrounding a liquid hydrogen target. The anode of the TPC is read out by a Micromegas detector segmented in 18 concentric rings of 2 mm x 2 mm pads totaling 3604 channels. Space constraints near this detector necessitated the development of an advanced cabling solution based on sub-millimeter pitch micro-coaxial cables to connect all pads to the preamplifiers placed one meter away. Using this technology, tests in experimental conditions show that channel noise remains low, typically ˜1500 electrons rms. A new readout system was designed for MINOS. Its built-in versatility allows exploiting a legacy readout chip, the AFTER designed for the T2K neutrino oscillation experiment, and its evolution, the AGET, made for active target TPCs. Both of these multi-channel ASICs (72 channels in AFTER and 64 in AGET) rely on a 512 cell switched capacitor array (SCA) to support a high sampling rate, up to 100 MHz, during a short time capture window (5.12 µs at 100 MHz sampling rate), with a typical power consumption as low as ˜20 mW/channel. Besides its four ASICs, the front-end card used in MINOS houses an inexpensive commercial FPGA module based on a Xilinx Spartan 6 FPGA. This "System-On-Module"approach led to an extremely fast development time while the full performance of the AFTER and AGET was preserved by a careful partition of tasks between those implemented in the FPGA fabric and those handled by the embedded MicroBlaze processor. One of the major improvements of the AGET compared to its predecessor, and other comparable devices, is that it includes a discriminator for each channel. The resulting information can be used to elaborate a self-trigger signal, and it is also exploited by the chip itself during the readout phase to time multiplex towards the external ADC only the cells corresponding to hit channels. This selective digitization brings a first level of data reduction and substantially cuts dead-time when occupancy is low, because only a small fraction of the SCA matrix is read out. Two other techniques are used to further reduce dead-time: 1) The mapping of detector channels to front-end electronics is made so that expected track hits are spread on different readout cards and chips; 2) A mechanism implemented in FPGA logic determines on the fly which chips have to be readout and which are skipped, depending on the hit occupancy of each AGET. Further data reduction and pre-processing are performed by the FPGA module that controls the front-end chips and handles communication over Gigabit Ethernet with the data acquisition PC. Over the last three years, five experimental campaigns with MINOS were conducted, all successfully. We describe the prominent aspects of the readout system of this instrument, present performance measurements, and report on lessons learned during exploitation.

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