A High Frame Rate Test System for the HEPS-BPIX based on NI-sbRIO Board

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***Abstract*—HEPS-BPIX is a pixel detector designed for the High Energy Photon Source (HEPS) in China. As a hybrid pixel detector, it consists of a silicon sensor and a readout chip which is bump-bonded to the sensor with Indium. The detector contains an array of 104×72 pixels while each pixel measures $150\mu m \times 150\mu m$. Each pixel of the readout chip comprises a preamplifier, a discriminator and a counter. Aiming at X-ray imaging, HEPS-BPIX works in the single photon counting mode. The counting depth of every pixel is 20 bits. The test system of the detector which implements all the control, calibration, readout and real-time imaging has been developed based on the National Instruments (NI) single-board RIO 9626 (sbRIO-9626). The field programmable gate array (FPGA) of the NI-sbRIO board deserializes the data from the pixel array and translates the clock as well as the serial configuration data to the detector. The FPGA firmware and the simple data acquisition (DAQ) system have been designed with LabVIEW environment in order to decrease the time of the development. Through the use of the LabVIEW programmed DAQ software, the test system can control the signal generator by Ethernet to calibrate the detector automatically. Meanwhile, it can monitor the real-time image and change the configuration data to make the debugging much easier. The test system has been utilized for the X-ray test and the beam line test of the detector. A series of X-ray images have been taken and a high frame rate of 1.2KHz has been realized. This paper will give the details of the test system and present results of the performance of the HEPS-BPIX.**

I. Introduction

PIXEL detector has been widely used in the high energy physics experiments due to the features of good spatial resolution, high readout speed and so on [1]. The High Energy Photon Source (HEPS) which will also use the pixel detector as the X-ray detector is now being built in China. HEPS-BPIX is a hybrid silicon pixel detector designed for the HEPS. It contains an array of 104×72 pixels while each pixel is of $150\mu m \times 150\mu m$ size. HEPS-BPIX works in the single-photon-counting mode, and every pixel has a counter of 20 bits. The frame rate of the detector can be as high as 1.2 KHz. Aiming to calibrate and test HEPS-BPIX, we need to design a test system which can handle the high frame rate. Meanwhile, in order to make the detector available in the market as soon as possible, developing the prototype for testing quickly is very important. This paper gives the details of the HEPS-BPIX design and reports the results of the experiments based on the test system. The results show that both the detector and the test system can meet the performance requirements of 1.2 KHz frame rate.

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II. Test system design

In order to develop a test prototype quickly and make it flexible to use, the test system is designed based on the National Instruments (NI) single-board RIO 9626(sbRIO)[2]. The board has a 400 MHz processor, a 512 MB nonvolatile storage, a 256 MB DRAM and a Spartan-6 LX45 FPGA for custom timing, inline processing and control. NI has developed the related LabVIEW modules to make the re-configuration convenient and slash the development time.

The test system consists of a pixel detector, a daughter board, a sbRIO-9626 board and a host computer. The architecture is shown in the Fig. 1. The silicon detector is bonded on the daughter board through golden wires which connect the pads of the readout ASICs to the daughter board. The daughter board is linked to the sbRIO-9626 by the RMC connector. The connector provides a direct link to the FPGA so that the FPGA can deal with the data from the daughter board and deliver them to the real-time (RT) processor. The RT processor translates the data and then sends them to the host computer by 100M Ethernet. The whole design includes the hardware design of the daughter board, the firmware of the FPGA and the software which runs on the RT CPU.

The daughter board provides the mechanical support and the electrical connection for the HEPS-BPIX detector. NI has provided some reference design templates for the sbRIO daughter board, whereas the daughter board of the test system is a little different from the normal sbRIO daughter board because of the unique application of the silicon pixel detector. As shown in Fig. 2, the main part of the daughter board is outside the boundary of the sbRIO mother board so that the sbRIO mother board can be shield by metal when the detector is exposed to X-ray. This design avoids the problems which may occur when the digital circuit works in the radiant environment. In order to reduce the impact from the noise of the mother board, the daughter board separates the power supply from which of the mother board. In addition, the daughter board provides the high voltage port for the detector

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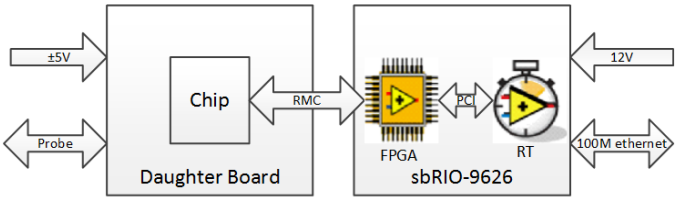

Fig. 1. Test system architecture. The pixel detector is wire bonded to the daughter board and directly connected to the FPGA through the RMC connector. The FPGA communicates with the real-time (RT) processor by the PCI bus. The RT processor can process and translate the data from FPGA to the computer through Ethernet.

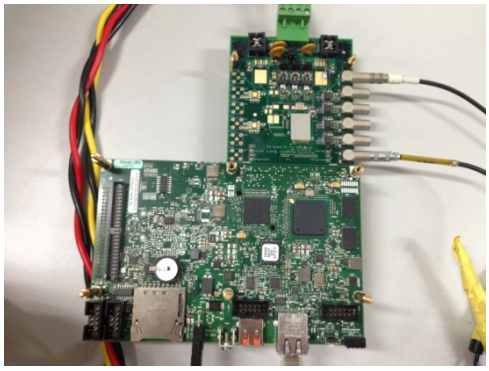

Fig. 2. The architecture of the sbRIO daughter board and mother board. The daughter board is beyond the boundary of the mother board to make the detector exposed to X-ray while the mother board is protected by the metal shield.

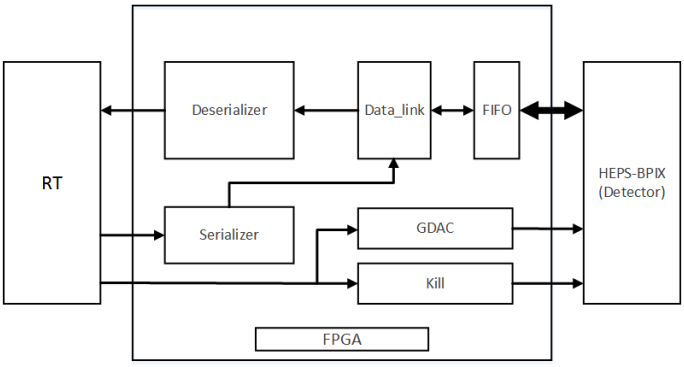

Fig. 3. Simple block diagram of the FPGA firmware. The FPGA deserializes the data from the detector and sends them to the RT processor for further processing. Moreover, the configuration data for the pixel array from the RT processor are serialized by the FPGA. GDAC and Kill are modules dealing with the other configuration data for the detector. The FPGA also provides the clock for HEPS-BPIX.

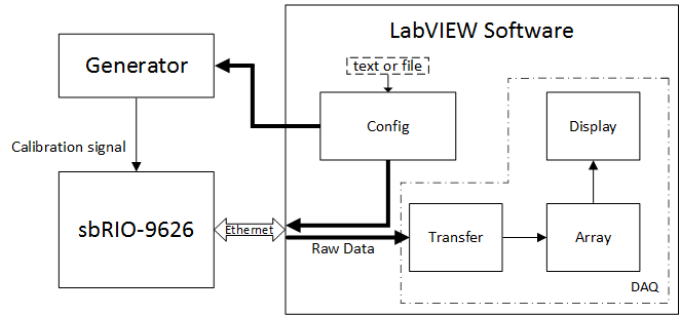

Fig. 4. The structure of the upper-computer LabVIEW software. The raw data from the sbRIO mother board are transformed to single-frame files by the Transfer module. The Array module processes the single-frame file and make it a 104×72 array which can be displayed by the Display module to implement the real-time imaging. The Config module can configure the test system as well as control the signal generator for S-curves collection.

and some input/output (I/O) ports for the monitoring and calibration signals to make the test and calibrate of the test system more convenient.

The design of the sbRIO mother board mainly includes the development of the FPGA firmware as well as the RT processor software. With the FPGA and RT processor LabVIEW modules provided by NI, all the designs can be realized by the graphical programming language in the LabVIEW programming environment and the development becomes quick and convenient. The architecture of the FPGA firmware is shown in Fig. 3. The counters of all the HEPS-BPIX detector pixels are readout serially and deserialized by the Deserializer module. Then the data will be delivered to the RT processor for further processing. The pixel array configuration information from the upper-computer is passed on to the Serializer module by the RT processor and serialized in the module before it sent to the front-end detector. First-in-first-out (FIFO) module acts as the buffer of the data when they are transferred in and out of the detector, and ensures the signals follow the timing requirements. The Data link module provides the data links between the Deserializer module, the Serializer module, and the FIFO module. The GDAC module deals with the configuration of the global threshold and the Kill module loads the kill chain information. Furthermore, the FPGA firmware provides the reset signal and the clock for the detector to make it work properly. The frame rate of the HEPS-BPIX detector will be 1.2 KHz and the total data rate will be 172Mbps when the clock frequency is 20MHz. The data can get through the PCI bus without cache but cannot be delivered to the upper-computer by 100M Ethernet in real time. Therefore, the RT processor have to utilize the DRAM on the sbRIO mother board as data cache as well as transfer the data between the PCI bus and the Ethernet to realize the frame rate of 1.2KHz. The sbRIO mother board can store more than 12000 frames, which is enough for the practical application.

The upper-computer software which is developed with the LabVIEW programming environment has the functions of configuration, data acquisition, and real-time imaging. All the functions are combined together to make a uniform user interface which can meet the requirements for the debugging and testing of the system. Fig. 4 gives the structure of the upper-computer. The raw data sent to the computer by Ethernet are stored as a packet of multiple frames. The packet is transformed to single-frame files in the Transfer module. Then, the Array module arrange the counters to make it a 104×72 matrix according to the pixel location of the detector. The Display module uses the matrix to realize the real-time imaging. The Config module sends the configuration information to the detector, and controls the signal generator to generate calibration signals. With the cooperation of the generator control and the data acquisition, the test system can get the S-curves of the HEPS-BPIX detector chip.

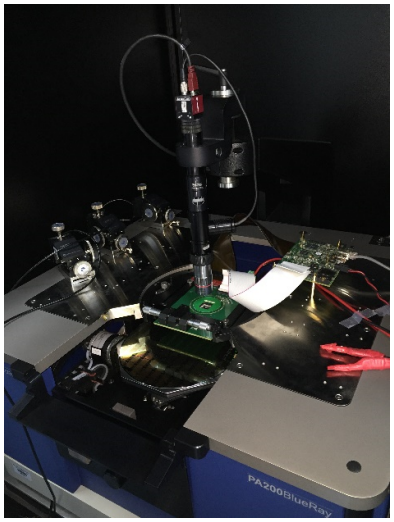

Fig. 5. The probe daughter board. The mother board, the FPGA firmware, and the LabVIEW software are reusable.

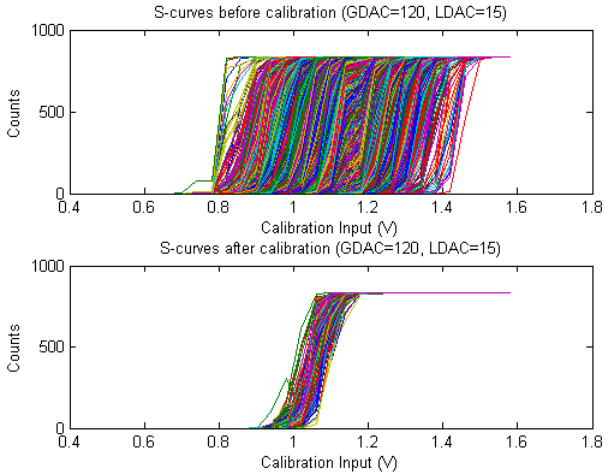

Fig. 6. S-curve before and after calibration. The equivalent noise extracted from the data is $115.8e^-$, and the threshold nonuniformity is $55.1e^-$.

Because the test system adopts the structure that the daughter board combined with the mother board, it has good reusability. At present, the probe daughter board has been developed to test the detector module before wire bonding as is shown in Fig. 5. Since the new system just changes the daughter board, there is no need to reconfigure the FPGA firmware and upper-computer LabVIEW software.

III. Test Results

According to the test results of the laboratory, X-ray source, and Beijing Synchrotron Radiation Facility (BSRF) 1W2B beam line experiments, the test system has been verified to be usable, and the frame rate of 1.2KHz has been realized. The laboratory tests mainly verify the functions of the detector chip, and calibrate the nonuniformity of the pixel thresholds. The calibration takes the method of S-curve [3] which means extracting the calibrated configuration information from the gathered S-curves to make the discrepancy of the thresholds as small as possible. Fig. 6 gives the S-curves before and after

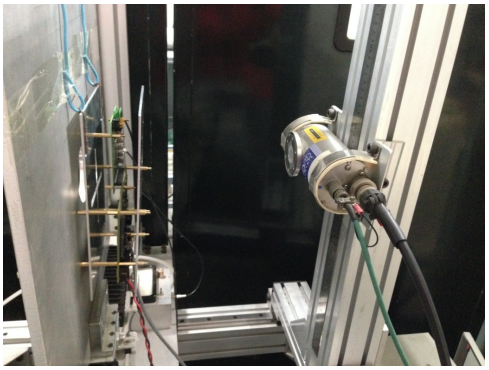

Fig. 7. The X-ray experiment environment.

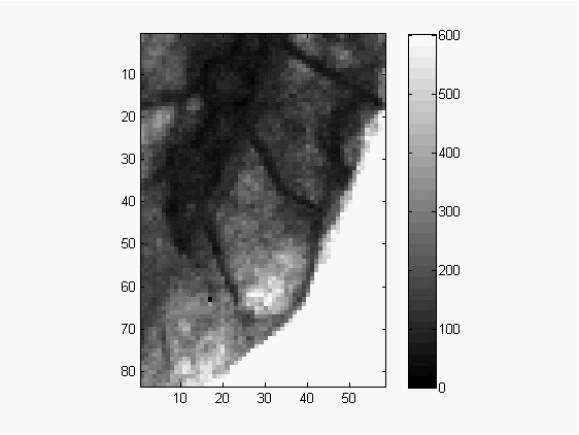

Fig. 8. A fishtail: image taken by a Fe55 X-ray source.

the calibration, the threshold dispersion after calibration is $55.1e^-$, and the equivalent noise calculated from the S-curves is $115.8e^-$. The experiments done with the X-ray source are imaging tests. The testing environment is shown in Fig. 7, and Fig. 8 gives the X-ray photography of a fishtail. Aiming at the synchrotron radiation application, tests have been carried out on the BSRF 1W2B beam line. One important test is an imaging experiment of a four-blades-fan which is rolling at the frequency of 50Hz while the frame rate of the detector is 1.2KHz. The metal blades stop the beam to make the image of the facula change. The images got from the test are periodical and repeat every 6 frames, which proves the frame rate to be 1.2KHz. Fig. 9 shows the frame 1, frame 3, and frame 5 of one period.

The test results show that the test system can implement the debugging and calibration of the detector. Also, it has the functions of data acquisition and real-time imaging. Furthermore, it reaches the target frame rate of 1.2KHz. Compared with the traditional developing method which designs the FPGA firmware with hardware description language (HDL) and writes upper-computer software with general programming language [4], [5], the development based on the sbRIO mother board makes the whole working completed in the LabVIEW programming environment, which is suitable for quick debugging and reconfiguration as well as reducing the prototype development time. There are real-time processors and FPGA on the sbRIO mother board, so the test system

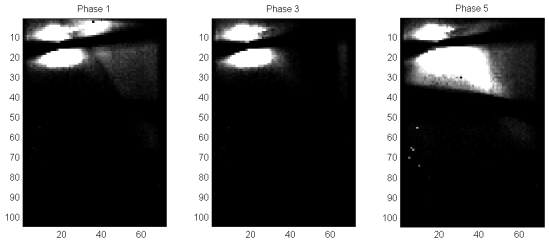

Fig. 9. Images taken by the beam light. A rolling fan with four blades was placed before the test system to stop the beam light. The rotation frequency of the fan is 50Hz and the period of every blade is 6 frames, which proves the frame rate of the system to be 1.2kHz. Phase 1, 3 and 5 of the 6 frames in a period are shown in the figure.

introduced in this paper is more flexible in use than the developments based on the PXI related boards [6], [7]. The test system can setup without PXI backplane and can link to the computer with commonly used Ethernet port.

IV. Conclusion

This article introduces a high frame rate test system designed for the HEPS-BPIX silicon detector and the experiments made to check the system and the detector. The functions of the detector have been verified and the design of the detector prototype with 6 detector modules is going smoothly thanks to the test results. In addition, the probe daughter board which is designed based on the test system has been utilized to testing the detector module before and after bump-bonding. The probe daughter board plays an important role in verifying the reliable of the bump-bonding technique and picking up suitable modules for the 6-modules detector prototype.

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