



Development of ATLAS Liquid Argon Calorimeters Readout Electronics for HL-LHC

Kai Chen

on behalf of the ATLAS Liquid Argon Calorimeter Group

BROOKHAVEN
NATIONAL LABORATORY

Brookhaven National Laboratory
Upton, NY, USA

The Phase-II Upgrade of Liquid Argon Calorimeters Readout

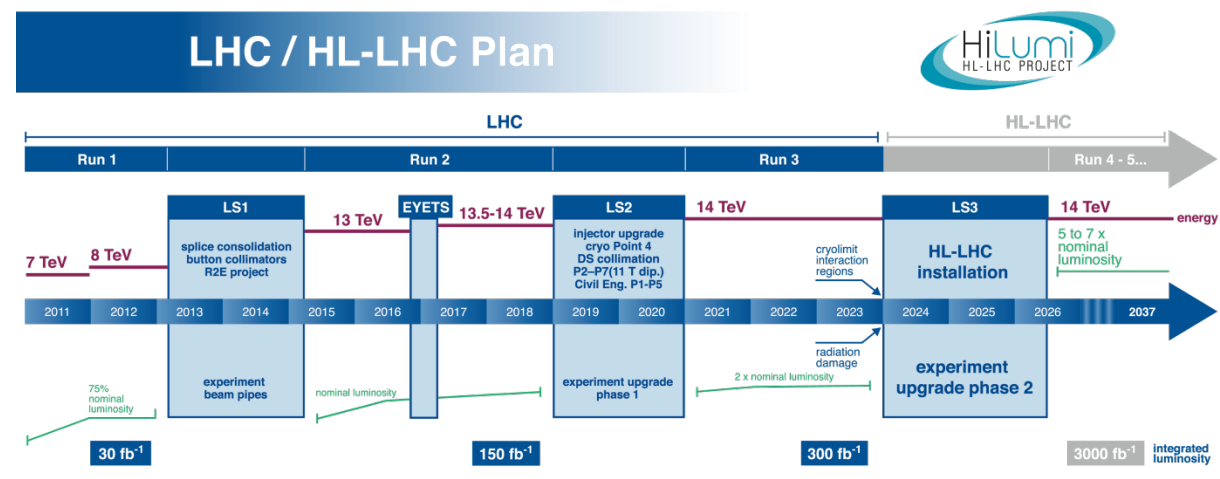


Fig.1 The LHC/HL-LHC Plan

The Large Hadron Collider (LHC) will be upgraded to HL-LHC (High Luminosity LHC) after Run 3. HL-LHC will have an instantaneous luminosity of $5-7 \times 10^{34} \text{ cm}^{-2}\text{s}^{-1}$, it can provide an integrated luminosity of $3-4.2 \text{ ab}^{-1}$ after 12 years of running. The Liquid Argon (LAr) calorimeters are used in the electromagnetic barrel, electromagnetic endcap, hadronic endcap and forward calorimeters of ATLAS detector. There is a total of 182,468 calorimeter cells.

The Phase-II upgrade of the readout electronics for the LAr calorimeters will be installed on the ATLAS detector during the third long shutdown in 2024 to 2026.

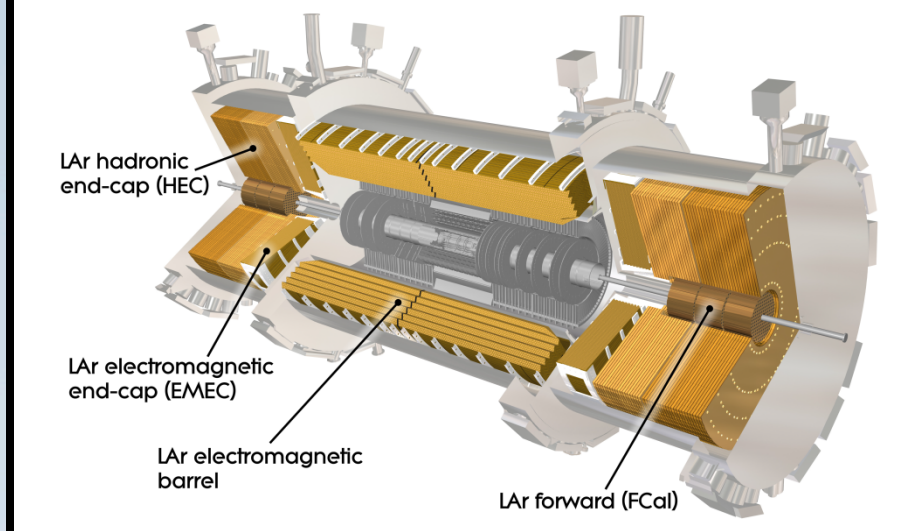


Fig.2 The LAr electromagnetic barrel, endcap, hadronic endcap, and forward calorimeters

Architecture of the Upgraded Read-out Electronics

The readout of all of the calorimeter cells will be performed at 40/80 MHz sampling rate and 14 bit resolution to cover 16 bit calorimeter signal, without trigger selection. To mitigate the pile-up effects in energy reconstruction, the second trigger level can get calibrated energies of all cells at a rate of 1 MHz.

Figure 3 shows the upgraded readout architecture. In front-end, the grayed “legacy” trigger electronics will be decommissioned. The LAr Trigger Digitizer Board (LTDB) and LAr Digital Processing System (LDPS) installed in Phase-I upgrade will be kept for the fast trigger. The main readout electronics with new FEB-2 (front-end boards) will amplify and shape the calorimeter cell signals, and digitize them with ADC running at 40/80 MHz frequency. The digitized data will be sent over high-speed optical links to the new back-end board LAr Pre-Processor Boards (LPPR). Totally there will be 60-120 LPPRs in ATCA crates. The LPPR will use the Phase-I LAr Digital Processing Blades (LDPB) board as the prototype. High performance extended optimal linear filter coefficient method (LOF) will be implemented in the FPGAs. The amplitude and timing of a signal pulse can be obtained. The front-end electronics need to be radiation tolerant and low power consumption. Some ASICs are currently being developed, like the pre-amplifier, shaper, ADC and the serializer in 65 and 130 nm CMOS technologies.

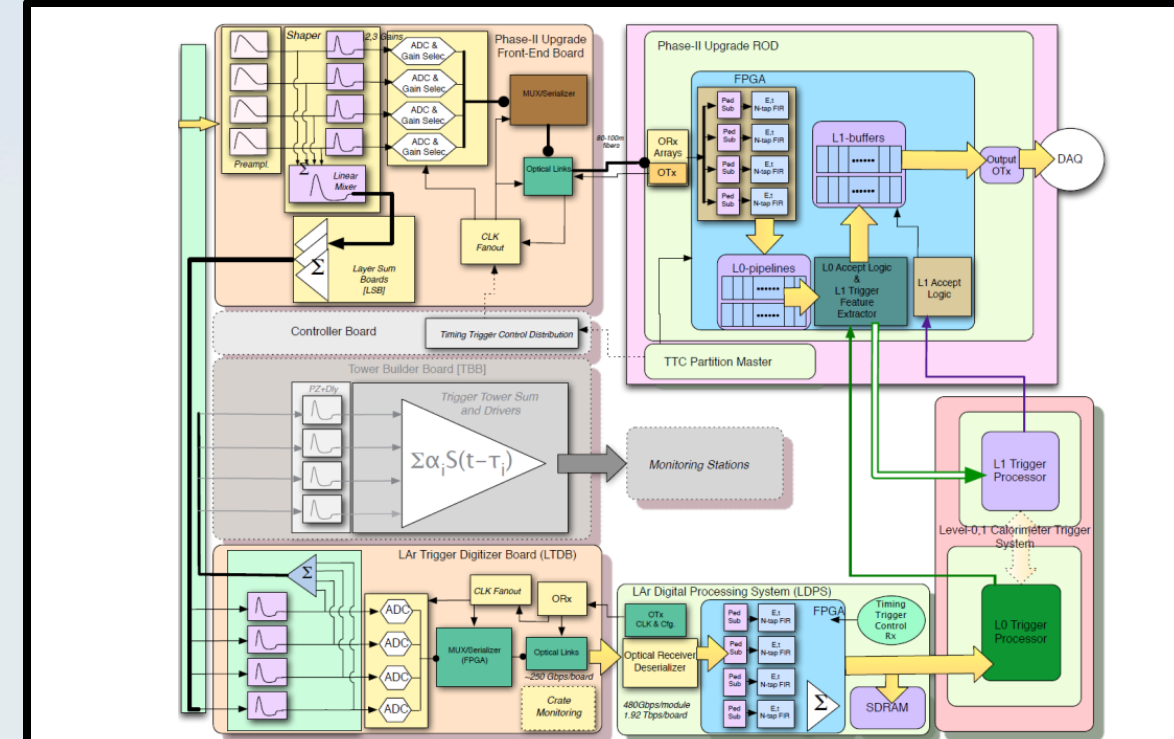


Fig.3 Phase-II upgrade of Liquid Argon Calorimeter readout architecture.

Analog Front-End

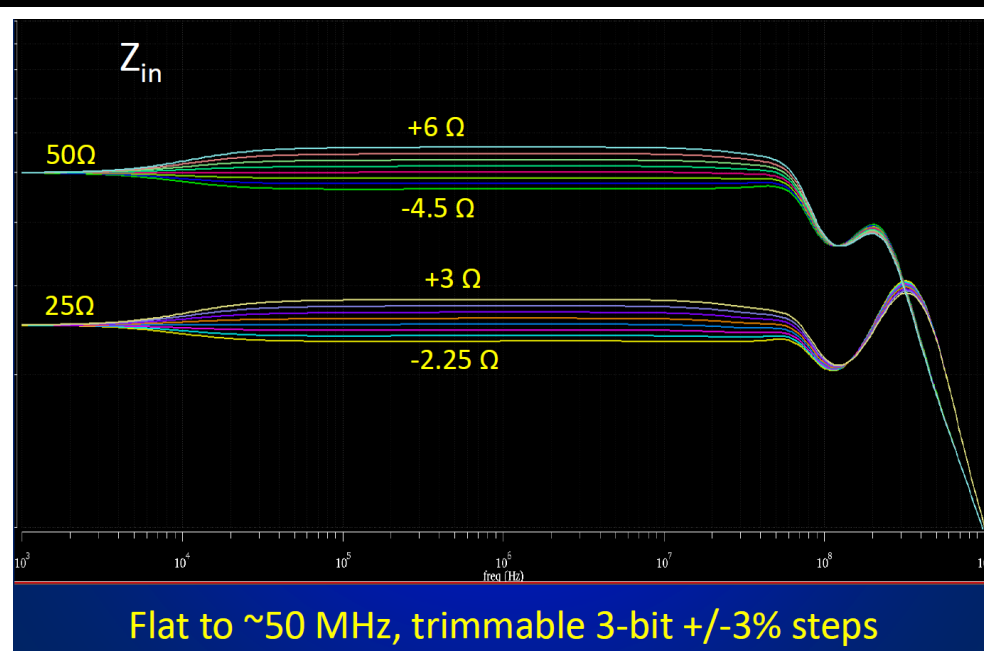
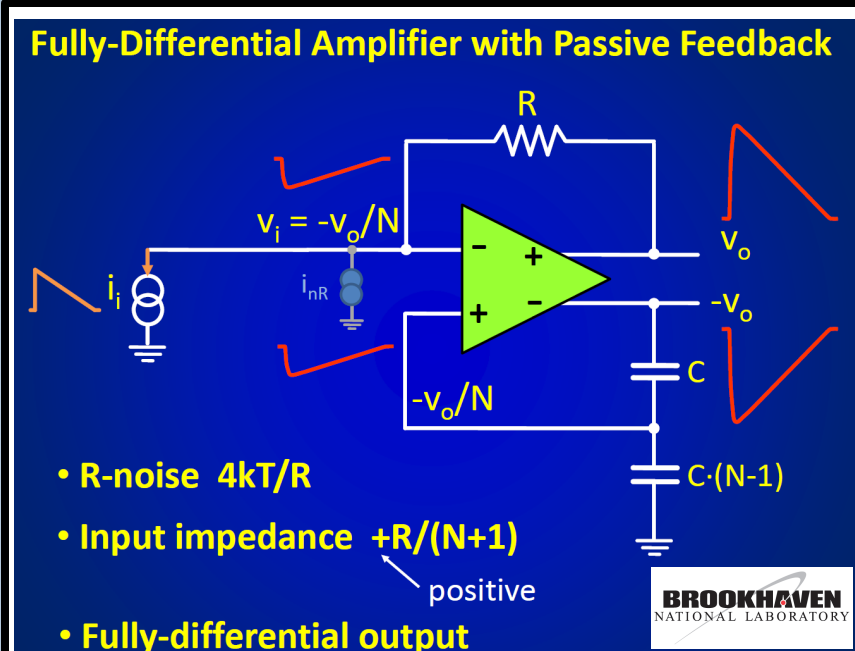
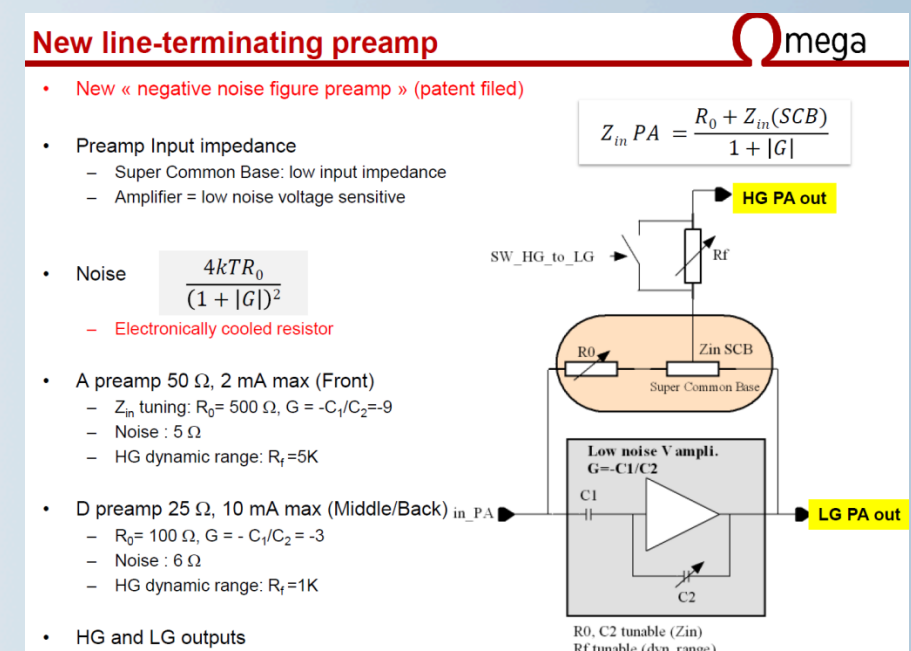
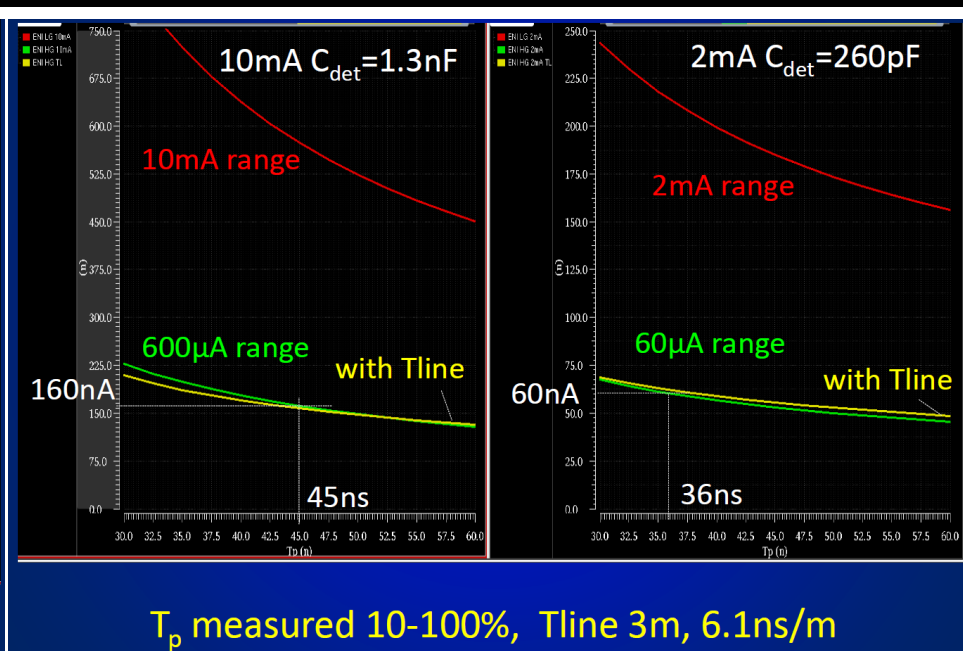


Fig.4 Architecture of the fully-differential amplifier (65 nm), and preliminary simulation results.



ADC Design

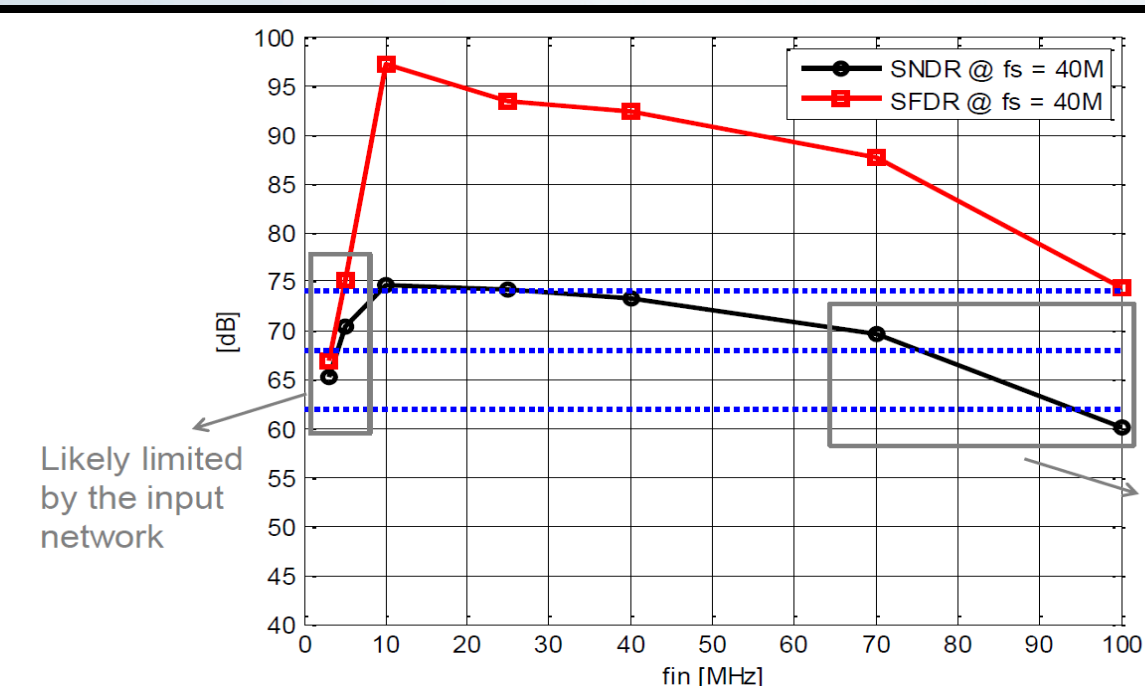
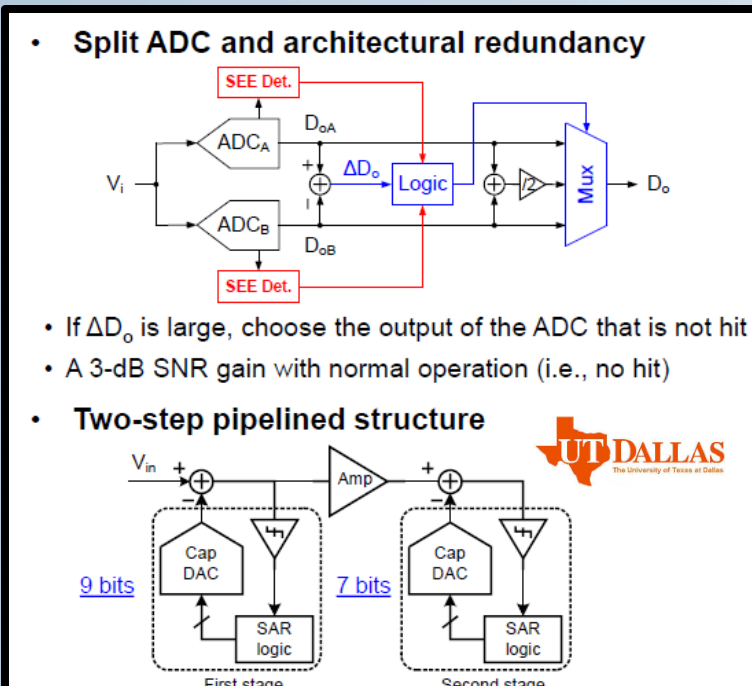


Fig. 6 Preliminary test results of the 14 bit Split-SAR ADC prototype (65 nm).

Conclusions

For the front-end analog part, a design with preamplifier and shaper using 65 nm CMOS technology with a 1.2 V supply, and a preamplifier with 130 nm CMOS technology with 2.5 V supply are being developed. The termination and dynamic range are programmable, they can be 25 ohm termination with 10 mA dynamic range, or 50 ohm termination with 2 mA dynamic range. There will be a low gain output and a high gain output in both cases. A common test bench is being developed for both ASICs, aim to get a preliminary test result in 2016. A split-SAR (successive approximation) ADC prototype with 65 nm CMOS technology has been designed and tested. Large DAC mismatch is observed due to some area is not filled with dummy around the SAR. The preliminary result shows a 12.1 bits ENOB measured at 10 MHz input for a 40M sampling rate. A new design based on the 40 MHz, 12 bit NEVIS ADC (130 nm CMOS) for Phase-I upgrade is expected to start soon. About the optical transmitter, the VLAD (VCSEL Array Driver) and its low power version lpVLAD have been submitted to IMEC in Feb. 2016. The test is expected in summer of 2016. The power is 35 mW/ch for VLAD, and 20 mW/ch for lpVLAD.

Based on the testing results of these ASIC chips, the basic requirement is to integrate the preamplifier and shaper. The desirable result will be to integrate the ADC. The best result is to also integrate serializer, and form an Front-End System On Chip (FESOC) for LAr readout on HL-LHC.

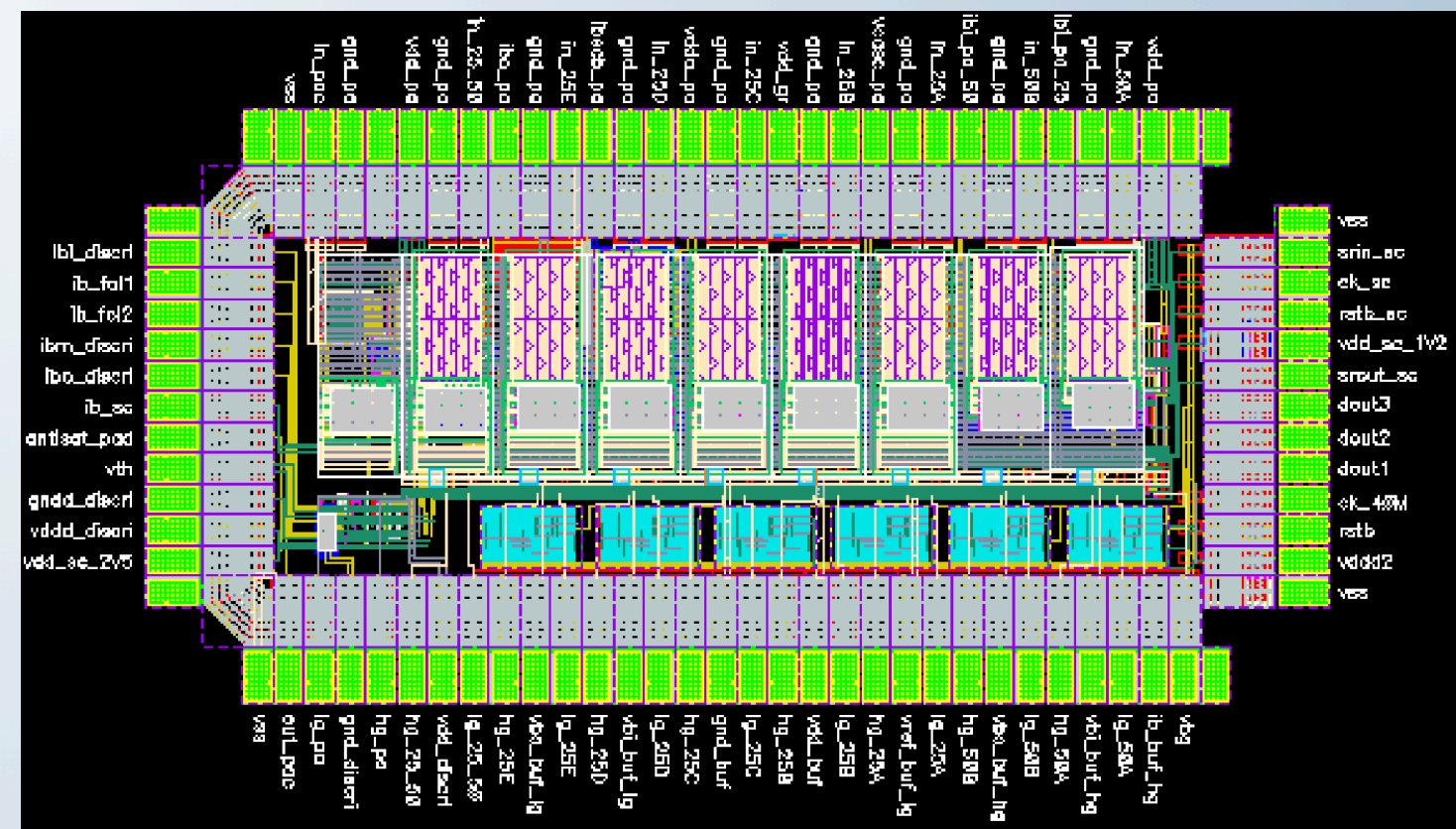


Fig.5 Layout of the preamplifier in 130 nm CMOS (OMEGA/LAL).

Optical Transmitter and Serializer

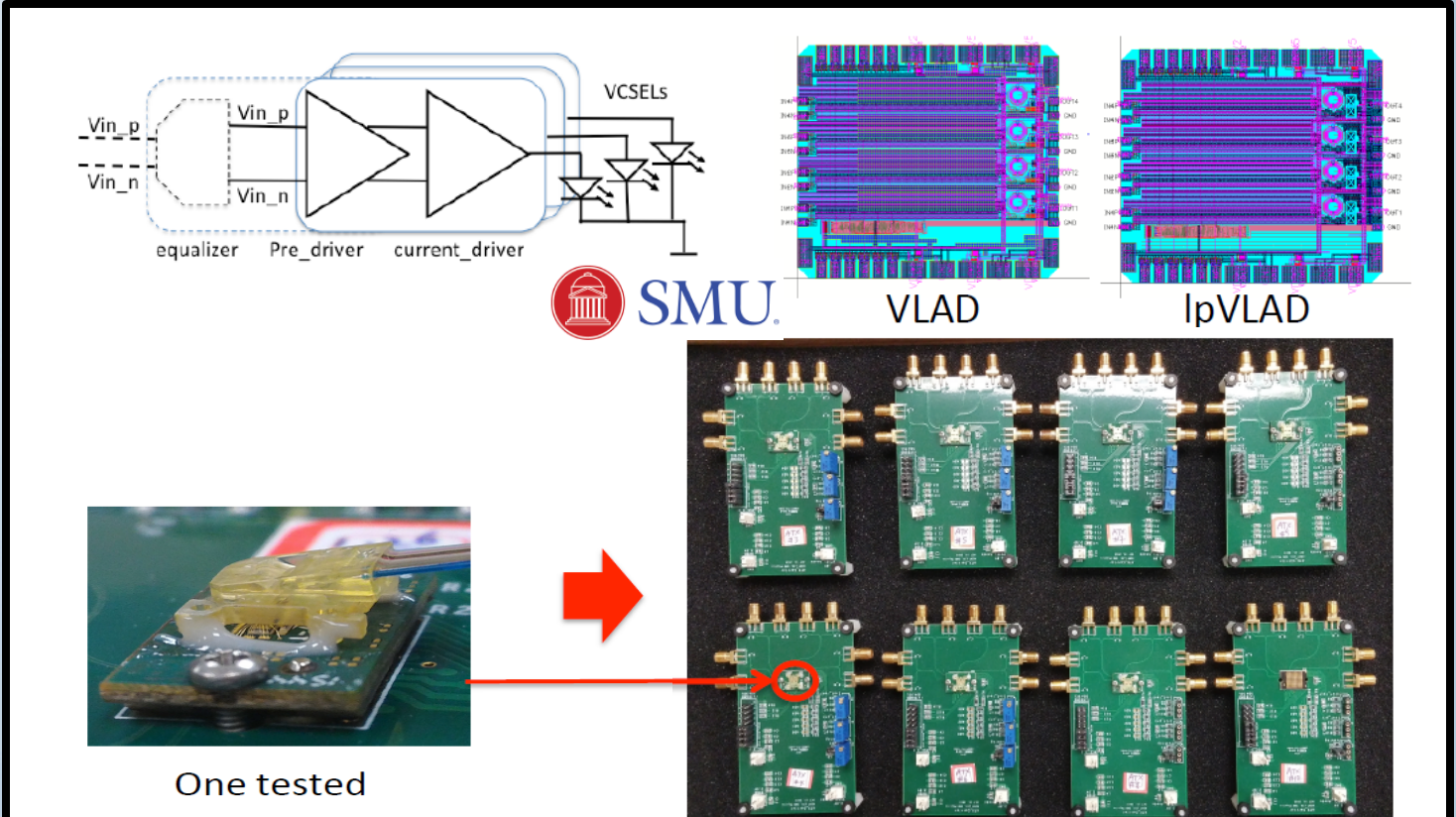


Fig.7 Design and layout of VLAD/LpVLAD (65 nm).