New updates on the ATLAS ROD board implementation for Pixel Layer 1 and Layer 2

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\textbf{Abstract}

This work intends to briefly overview the new technological updates on the LHC ATLAS acquisition system of the Pixel Detector.

The herein presented Read-Out Driver (ROD) is a VME board devoted to data processing, configuration and control. It is designed to provide data formatting, front-end-specific error handling, and calibration.

This board was initially designed to interface the data sensed by IBL with the ATLAS TDAQ system. The Insertable B-Layer (IBL) is the innermost sensing layer of the ATLAS Pixel Detector, added during the 2013/2014 LHC long shutdown, to withstand higher luminosity and feature higher throughput performance. To read out the new layer of pixels, with a smaller pixel size with respect to the other outer layers, a front end ASIC (FE-I4) was designed. Because of its optimal performance, it was decided to adopt the IBL ROD also for Pixel Layer 1 and Layer 2. Among the several advantages, one of the most important is the reduction of link occupancy due to the increased bandwidth (80 Mbit/s, two times the previous one). 40 ROD boards, fabricated and tested in 2015, were installed in the Layer 2 acquisition system while 45 RODs for Layer 1 are still under test and will be installed by the end of 2016.

\textbf{ROD Firmware for IBL and for Pixel Layer 1 and 2 are slightly different:}

- FHM and Master FPGAs have the same firmware
- Slaves FPGAs are different in some ways:
  1) Front-end chips providing data are different;
  2) Data are decoded in different ways;
  3) IBL BOC has 2 SLink per Slave FPGA, while Pixel Layer 1 / 2 BOC has only 1 SLink per FPGA, so the router outputs have to be merged in a unique bistream;
  4) If Eo size and configuration parameters are different

\textbf{Comparison between old SiROD and new ROD}

- 12 FPGAs
- 12 external FIFOs
- 5 DSPs
- Max bandwidth = 40 Mbit/s for Layer 2 and 80 Mbit/s for Layer 1
- Communication with Software programs through VME
- 4 FPGAs
- 8 external FIFOs (only inside FPGAs)
- 6 DSPs
- Max bandwidth = 80 Mbit/s for Layer 2 and 160 Mbit/s for Layer 1
- Communication with Software programs through PPC (ethernet) and VME

\textbf{Summary}

- 64 RODs have already been delivered to CERN.
- 14 RODs for the 14 staves of IBL are currently running in USA15.
- 26 RODs for Pixel Layer 2 are currently running in USA15.
- 6 RODs (out of 40) for Pixel Layer 1 are currently running in USA15.
- 45 RODs (Layer 1 + spare) are under test right now and will be delivered by the end of the year.
- ROD Firmware for IBL and Layer Pixel 2 / 1 is done, data taking and calibration also work. The entire software-firmware system debug is ongoing so that the ROD code is continuously under development for a fine-tuning.
- ROD data bandwidth 100 Mbit/s for Layer 1 still under development, time plan is to have it working before the end of the 2016.
- Due to optimal performances obtained, Pixel B-Layer ROD upgrade is considered right now.