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A DAQ Prototype for the ATLAS small-strip Thin Gap Chamber Phase-I Trigger Upgrade

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ATLAS is one of four experiments that is located at the Large Hadron Collider (LHC) now being constructed at CERN, Geneva, Switzerland. The ATLAS detector accepts the events from the proton–proton collision at a rate of 40 MHz. The Tracks containing events of interest are selected via a series of trigger decisions. However, the low energy protons, generated in the magnet materials between the small wheel (SW) and the end-cap muon detector (EM), hits the end-cap trigger chambers, thus producing fake triggers. As the already existing Muon Trigger is not capable of determining the direction of the muon before the magnetic field, muon not emerging from the Interaction Point (IP) can be misidentified as primary trigger candidates. In order to cope with these problems, the ATALS detector will be upgraded in 2018. we will present a DAQ prototype designed for the ATLAS small-strip Thin Gap Chamber (sTGC) Phase-I trigger upgrade. The prototype includes two VMM chips developed to read out the signals of the sTGC, a Xilinx Kintex-7 FPGA used for the VMM2 configuration and the events storage, and a Gigabit Ethernet Transceiver (GET) working at the physical layer. The VMM2 chip is composed of 64 linear front-end channels. Each channel integrates a Charge Sensitive Amplifier (CSA), a shaper, a stable band-gap referenced baseline, several ADCs and other functions. For large data transmission, a large data transfer rate is needed. The test result shows that the transfer rate of the GET can reach up to 900Mb/s without missing code. In order to test the performance of the developing sTGC detector in the future, an event identity is added behind each event, which is implemented via a counter. The GUI panel mainly achieves several functions: the global reset and parameter set, the VMM configuration, VMM data acquisition and some Test modes.

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