

A cosmic ray readout system for qualifications of small-strip Thin Gap Chambers of the ATLAS Muon Spectrometer Phase-I upgrade

Xu Wang, Kun Hu, Houbin Lu, Feng Li, Hang Yang, Xinxin Wang, Tianru Geng, Liang Han and Ge Jin

Abstract—The Atlas detector, which is one of the Large Hadron Collider (LHC) at CERN, will be upgraded in order to extend the frontiers of particle physics. Bunches of up to 10^{11} protons will collide at the rate of 40MHz to provide 14TeV proton-proton collisions at a designed luminosity of $10^{34}\text{cm}^{-2}\text{s}^{-1}$. Currently ATLAS is under Phase-I upgrade, which focus mainly on the Level-1 trigger system to maintain the full acceptance of muon tracking while discriminate against background and keep the Level-1 rate at an acceptable level. The New Small Wheel(NSW), which consists of 16 detector planes in two multi-layers comprising of four small-strip Thin Gap Chamber(sTGC) and four MicroMagas(MM) detector planes, is to replace the current muon Small Wheel in order to achieve the upgrade goals. The sTGC Level-1 pad trigger logic is implemented first single wedge pad trigger which is based on coincident hits in three out of four layers of a multiplet in each wedge independently and then pad trigger which is based on geometrical matching between the two wedge triggers in order to identify the interaction point (IP). We designed the pads Front End Board (pFEB) to gather and analyses pads trigger which is the most important issue for Atlas Phase-I upgrade.

I. INTRODUCTION

The ATLAS experiment at the CERN Large Hadron Collider (LHC) will be upgrading its Muon Spectrometer during LHC phase-I upgrade in around 2019 to benefit from high luminosity and high energy runs at the LHC[1], [2]. The upgrade will replace the innermost station (namely Small Wheel) of the Muon Spectrometer in the forward region with the so-called New Small Wheel (NSW)[3], in order to improve its Level-1 trigger in the high background rate environment. The NSW employs two types of high rate capable gaseous detectors, namely MicroMesh Gaseous Structure (Micromegas)[4] and small-strip Thin Gap Chamber

(sTGC)[5], for on-line reconstruction of muon segments with pointing accuracies of 1 mrad. sTGCs, primary trigger detectors similar to those Thin Gap Chambers instrumented in the present ATLAS Muon Spectrometer but with fine-pitch readout strips, will utilize about 400k readout channels to discriminate bunch crossing in 25 ns and determine hit positions with a precision of about 100 μm per detector layer. Stringent requirements on the timing and spatial measurement precisions, large number of readout channels all impose significant challenges to both the detector construction as well as readout electronics system design. The readout front-end boards under development for the sTGC detector will carry four to eight 64-channel sophisticated amplifier and digitization ASICs(namely VMM)[6][7], four trigger data processing ASICs(namely TDS)[8] as well as readout and slow control chips. These boards are expected to carry hundreds of channels of sensitive analog signals as well as high speed serial lines with speeds up to 4.8 Gbps to shift out trigger data off detectors. Large amount of data to be processed on detector and moved out in both trigger and precision readout paths with low latency requirement are of big concern. We will present the development of the first prototype of the front-end board for the sTGC detector, readout scheme and firmware for the mini data acquisition system that has been used to characterize the amplifier and digitation ASIC as well as for integration test with a prototype detector. Results from the front-end board and the prototype detector integration as well as plans to develop a full data rate acquisition system to verify the front-end electronics design will be discussed.

II. SYSTEM ARCHITECTURE

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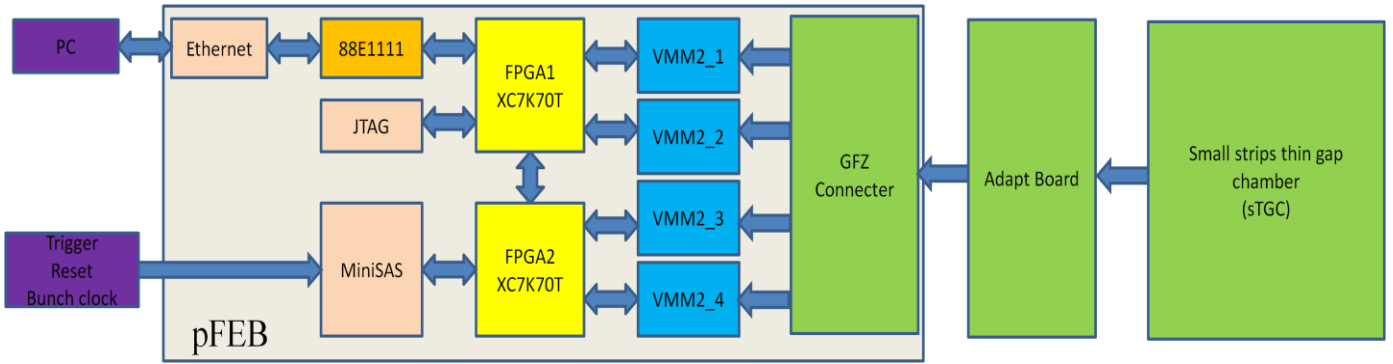


Fig. 1. The block diagram of the cosmic ray readout system.

Fig.1 is a simplified block diagram of the cosmic ray readout system. The signals of the sTGC prototype detector (pads, strips and wires) are gathered by an adapt board and then come through the GFZ connector to the pFEB. The GFZ connector has 10*30 pins and 256 channels will be used as signal channels and others will be used as ground connections. The 256 signal channels will be sent into the VMM2 chip, which is an application-specific integrated circuit (ASIC) chip designed specifically to amplify, shape and digitize the signals from the chamber. Information of amplitude and timing of each hit will be recorded. Kintex-7 FPGA is used for the configuration and data readout of VMM2 chips. External trigger, reset and bunch clock will also be sent to FPGA via twinax cables for system synchronization and event pickup. Trigger ID and Bunch clock ID are assigned in FPGA for event grouping with different systems. Ethernet will be used for communication with PC, including receiving commands and configuration bits and sending data picked from VMM.

III. SYSTEM DESIGN

A. Pads Front-end Board(pFEB)



Fig. 2. The photo of the pFEB(bottom) and the former FEB(top).

Fig.2 is a photo of our pFEB(bottom) and the former FEB(top). As you can see, the pFEB is designed with a size of 6.5cm*16.5cm in order to be installed on the limited space on the detector, which is about the same size of the former front-end board. However, there are 256 input channels on the pFEB instead of 16 on the former FEB. In addition, pFEB can achieve much more functions like analog and digital output, Ethernet communication, data storage and analyze with FPGAs and external trigger while the former FEB have only time over threshold pulse output. We can benefit from these additional functions to study the performance of the chamber and get much more information. High density, high event rate and anti-radiation requirement are great challenges for the design, solder and debug of the pFEB board. A variety of tests have been performed with internal test pulse, external test pulse and chamber. The digital output is consisted with flag, threshold, channel number, peak amplitude ADC count, TDC count and bunch clock count. All the ADCs are calibrated with an external signal source so that the ADC count can be converted to input charge or time for further analysis. Our test results prove that the pFEB is able to achieve the functions required.

B. FPGA data readout

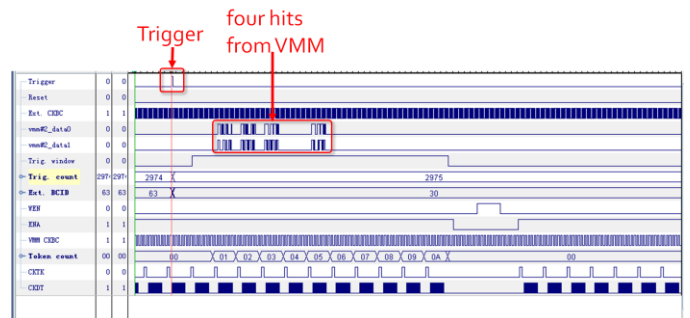


Fig. 3. Time diagram of FPGA.

A trigger window is opened when an external trigger is received by FPGA. The external trigger is the coincidence of several layers of scintillators and has been fan-out to different FEBs. All the data will be saved in FPGA when the trigger window is opened. Raw data from VMM2 is consisted of flag bit, threshold bit, channel number, amplitude ADC count, TDC count and Bunch Clock ID, chip ID, trigger ID and extended BCID are added to the data for event

synchronization. The reorganized data are sent to PC through Ethernet.

A. Graphical User Interface on PC

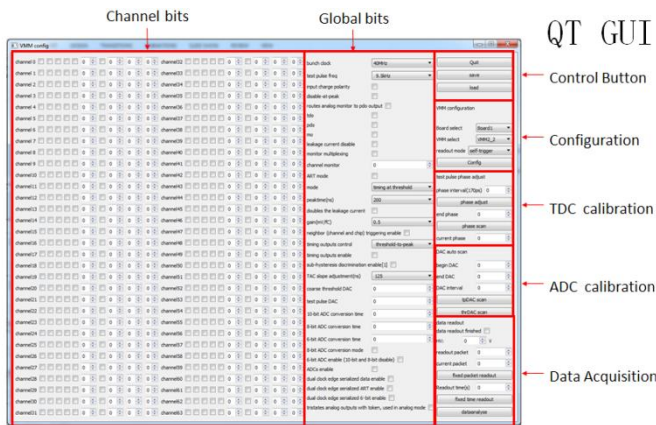


Fig. 4. The picture of QT GUI.

A graphical user interface(GUI)(shown on Fig.4) based on QT is developed for the configuration and data readout. The GUI sends commands and receive data from pFEB through Ethernet. Pcap library is used to get access to Ethernet. Each VMM2 chip require 1616 configuration bits containing mode, polarity, gain, peaking time, threshold and other settings which can be set and sent to FPGA with the GUI, then the FPGA will config the VMM2 chips. The output signals are delivered to FPGA which will store the data and sent to via Ethernet, then the GUI will capture the Ethernet packets and save the data to a binary file. Some simple analyze with the data can be done with the GUI and channel histogram will be displayed in order to monitor the readout system.

IV. TEST RESULT

A. Electronic Test

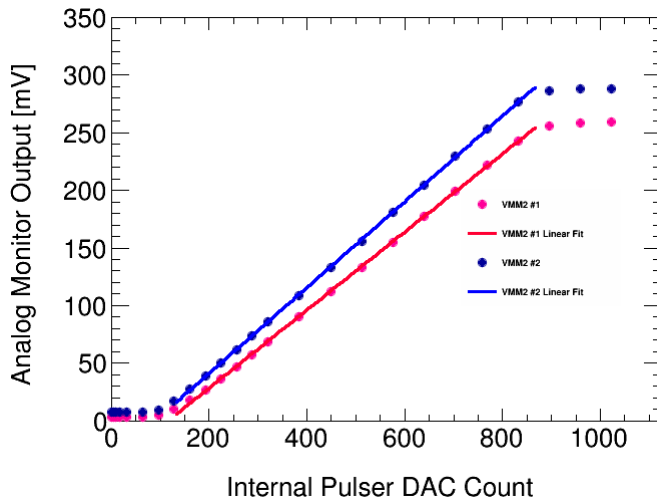


Fig. 5. The linearity test of the VMM internal pulser DAC.

Internal test pulse is provided by VMM2 chip and dominated by a pulser DAC which is controlled by the configuration bits. We have tested the linearity of the pulser

DAC by stepping up the pulser DAC and measure the analog output of VMM2. The internal test pulse will be used for the calibration of the amplitude ADC and TDC in VMM2.

B. Noise Test

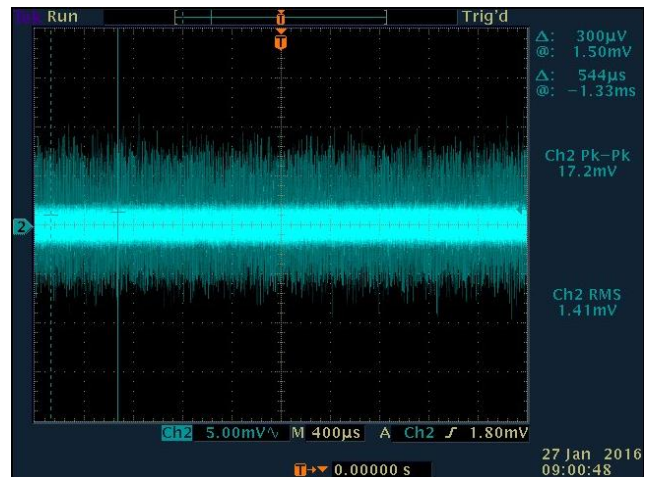


Fig. 6. The typical analog signal of sTGC pads.

Fig.6 shows the typical noise of the pads of the sTGC prototype. The pad size is $75\text{cm}^2(8.7\text{cm}*8.7\text{cm})$ and the gain we use for the test is $1\text{mV}/\text{fC}$. There is a variation between different channels, and the RMS value of the noise is between 1mV to 1.6mV .

C. Chamber Test

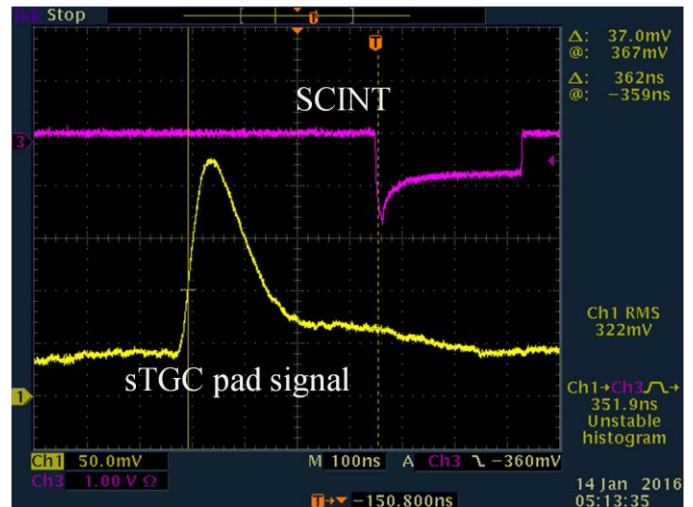


Fig. 7. The typical analog signal of sTGC pads

Fig. 7 is a typical analog signal observed with oscilloscope. The signal is triggered by scintillators. The amplitude and timing information are digitized and sent to FPGA.

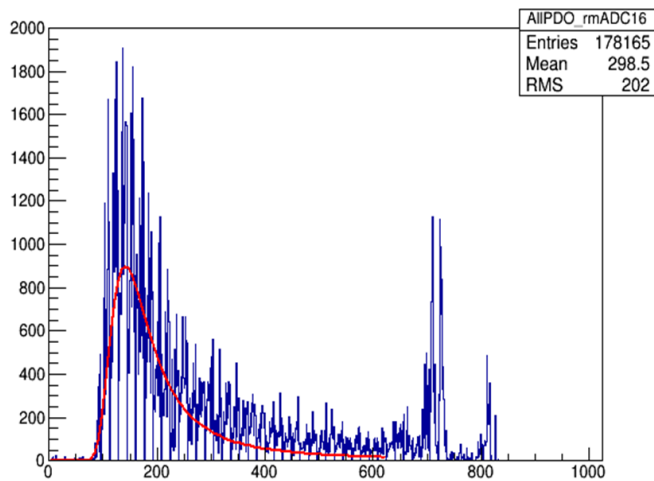


Fig. 8. The amplitude distribution of sTGC pads

Fig.8 shows the amplitude distribution of over 178k sTGC prototype pad cosmic ray hits picked up by external under the high voltage of 2800V. The gain we use is 1 mV/fC. The distribution is reasonable and the readout system can meet the design purpose for sTGC qualification.

V. CONCLUSION

In this paper, a cosmic ray readout system has been built for small-strip Thin Gap Chamber (sTGC) qualification. We

designed the pads front-end board and a DAQ prototype based on FPGA with Ethernet communication to PC and external trigger acceptance. Test results show that the system is able to measure the noise rate, efficiency, amplitude and timing which are important for sTGC qualification.

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