uSOP: a microprocessor-based Service-Oriented Platform for Control and Monitoring

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Overview

• uSOP: a Service-Oriented Platform for embedded applications
• Hardware
• Software
• uSOP at work: monitoring @ KEK Laboratory
  – Belle2, Beast
• Future plans
• Conclusions ...
• ... and one for aficionados of manga 漫画 ...
uSOP

- **uP-based, Service-Oriented Platform** for embedded applications
- Designed for slow-controls the Belle2 experiment (KEK-Tsukuba, J)
- Strongly oriented to SPI, I2C, JTAG, UART, with isolated power for peripherals and sensors
- Fully managed remotely
- Running Linux OS (Debian)
- 3U Eurocard native form factor, expandable
- Derived-from and compatible-with BeagleBone Black open-source project
LET’S SPEAK
uSOP – uP and utilities

- 512 MB DDR3 RAM
- 4 GB Flash eMMC
- USB device
- 10/100 Ethernet
- USB host
- uSD
- 10/100 Ethernet (controls and management only. See next slide)

A. Aloisio
20th IEEE Real Time 2016 - Padua, Italy
Remote Management

- Remote control over IP for:
  - uP RST
  - Boot mode
  - Power on/off

UART over IP:
- Console
- Bootloader

- More tasks can be implemented (watchdog, controls, ...)

- Based on the latest version of Lantronix Xport-Pro
- μP Freescale MCF5208, MMU-less architecture, 8MB RAM, 16MB Flash
- SoC running uCLinux with a full cross-compiled SDK
uSOP – Peripherals/Intf

- 16 x GPIO
- 2 x RS232 (*)
- 2 x SPI (*)
- 2 x I2C (*)
- 4 x 12 bit AIN (**)
- + 2 on-board power monitoring

• = fully isolated, 5V-12V supply
** = buffered

Pace Scientific

Timers
PWM
Event Capture
PRU

FPGA firmware download
SOFTWARE
Linux porting

• Linux distribution: Debian - armv7l
  – image-builder script to generate a Linux Debian rootfs image for operating system installation on eMMC or network booting
• Full support for compilers and applications (packages management via APT repository)
• Kernels: major releases available
  – 3.x (up to 3.8.13 with Xenomai - Real-Time Linux support)
  – 4.x (up to 4.5.0)
• bootloader: U-Boot
  – some patching done on official TI bootloader in order to enable network booting and boot media selection (eMMC, uSD, network)
• first stage boot available:
  – eMMC
  – uSD
  – UART (XModem/YModem protocol)
  – Ethernet (DHCP + TFTP)
• Linux boot available
  – eMMC
  – uSD
  – Ethernet (TFTP)
• Devices for root filesystem (rootfs) mounting:
  – eMMC
  – uSD
  – Ethernet (NFS)
EPICS

Experimental Physics and Industrial Control System

• EPICS ([http://www.aps.anl.gov/epics/](http://www.aps.anl.gov/epics/)) is a set of Open Source software tools, libraries and applications developed collaboratively and used worldwide to create distributed soft real-time control systems for scientific instruments such as particle accelerators, telescopes and other large scientific experiments.

• On uSOP:
  – Straightforward compilation on ARM
  – Variety of EPICS extensions available on board:
    • ALH (ALarm Handler)
    • PV gateway
    • Asyn
    • StreamDevice
    • Autosave
  – IOCs for:
    • Linear LTC2499 (I2C)
    • Linear LTC2983 (SPI)
    • Sitara ADC (parallel)

• On XportPRO
  – uCLinux customization, to enable additional software packages and security reinforcement of network services (SSH vs telnet)
  – Custom, low-footprint EPICS implementation, cross-compiled for uCLinux
  – IOCs for:
    • I2C protocol software emulation
    • SITARA power control
    • SITARA first stage boot setting (eMMC, Ethernet, uSD, UART)
    • LED activity
Beebotte as EPICS IOC consumer

- Beebotte ([https://beebotte.com/](https://beebotte.com/)) is an open cloud platform for network connected objects.
- In our system, EPICS IOCs are interfaced with Beebotte using the bbt-Python library. Data is pushed to Beebotte every few minutes.
- A Publish/Subscribe model offers bidirectional data communication. Users decide which data to retain by using persistent and/or transient messages.
- Beebotte has REST API to let backend (server) applications read, write and publish data.

Traffic from SPI, I2C, UART, JTAG, ADC

EPICS IOCs <-> bbt_python

Pub/Sub

REST API

Source: Beebotte.com

Websockets

Pub/Sub

Traffic from

Web Traffic
Auth. requests

Server (backend)

Clients (Browsers)

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System Metrics Dasboard

- In the same fashion, Beebotte is also used to monitor the uSOP main system metrics:
  - CPU load
  - RAM/FLASH usage
  - Network activity
  - peripheral power supplies
SLOWDOWN...
$\Delta\Sigma$ ADC – LTC2499 noise floor

- uSOP bench test with LTC2499:
  - $\Delta\Sigma$ ADC, 24 bit
  - I$^2$C, powered by uSOP isolated supply
  - $V_{in} = 0$V, Input shorted to local ground
  - ~5 Hz sampling rate
  - x1 mode
  - 50 Hz filter
  - $V_{ref}$: 5V
  - Read-out by EPICS IOC
  - GUI by CSS/BOY

Source: linear.com
BEAST is a detector presently taking data at SuperKEKB Interaction Point, to study beam background.

uSOP is monitoring T and Rh of the 18 BEAST crystals (LYSO, CsI, CsI(Tl)). Data available via EPICS and Beebotte.
The EndCap ECL monitoring system 1/2

- Minimal, stand-alone monitoring system at the EndCap ECL test station
- 4 sectors over 32 monitored to control the conditioning system (T, Rh)
- Up-time > 1 year
- Data available via both EPICS and cloud

uSOP box
EndCap Sectors 7F and 8F
Cable Adapters

EndCap Test Station at Fuji Exp. Hall, KEK
The ECL EndCap monitoring system 2/2

• The final monitoring system will be installed at KEK during 2016
• Forward and Backward ECL:
  – 2112 CsI(Tl) crystals, 32 sectors
  – T and Rh monitor, 128 analog channels (96 thermistors + 32 Rh probes)
• Features:
  – 3-wire read-out to cancel the 40m cable stray resistance
  – Stray thermocouple effects cancellation
  – 8 uSOP boards, 16 ADCs (24 bit)
  – 6U, 12HP form factor, shielded
  – Selective ground scheme to avoid loops
  – Read-out and controls via network
IS UNDER DEVELOPMENT...
Texas Instruments has released recently the 1.5 GHz dual-core Cortex A15 Sitara AM5728.

On this uP, we have started the design of a new platform with FPGA and dual high-speed ADC: uSOP+.

Not just monitoring: DSP, hardware processing, high-speed links, ...
Conclusions

• uSOP has been intensively tested at KEK, starting from Apr. 2015
• Stable and reliable LINUX platform, with uptime > 1 year
• Access to SITARA Event Capture peripherals
• Hardware controllers for all most common field busses
• Fully (re)configurable and managed remotely (from brick to fully functional)
• Designed to work as a stand-alone unit, yet easy to deploy in complex control infrastructures
• EPICS and NSMv2 compliant, IOCs developed for all the needed DAQ units

• A last thing for the Manga lovers...
Just for fun ...

• Japanese colleagues told us Usop (ウソップ) is one of the One Piece characters by the manga writer Eiichiro Oda

• ... More about Usop on wikipedia:
  – https://it.wikipedia.org/wiki/Usop
The End
BACKUP
# Cortex A Cores (32bit)

<table>
<thead>
<tr>
<th>Cortex-A</th>
<th>ARMv7-A</th>
<th>ARMv8-A</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cortex-A5[^23]</td>
<td>Application profile, ARM / Thumb / Thumb-2 / DSP / SIMD / Optional VFPv4-D / FPU / Optional NEON / Jazelle RCT and DBX, 1-4 cores / optional MPICore, snooping control unit (SCU), generic interrupt controller (GIC), accelerator coherence port (ACP)</td>
<td>4.84 KB / 4.84 KB L1, MMU + TrustZone</td>
</tr>
<tr>
<td>Cortex-A7[^24]</td>
<td>Application profile, ARM / Thumb / Thumb-2 / DSP / VFPv4-D / FPU / NEON / Jazelle RCT and DBX / Hardware virtualization, in-order execution, superscalar, 1-4 SMP cores, MPICore, Large Physical Address Extensions (LPAE), snooping control unit (SCU), generic interrupt controller (GIC), ACP, architecture and feature set are identical to A15, 8-10 stage pipeline, low-power design[^25]</td>
<td>0-64 KB / 0-64 KB L1, 0-1 MB L2, MMU + TrustZone</td>
</tr>
<tr>
<td>Cortex-A8[^26]</td>
<td>Application profile, ARM / Thumb / Thumb-2 / VFPv3 FPU / NEON / Jazelle RCT and DAC, 13-stage superscalar pipeline</td>
<td>16-32 KB / 16-32 KB L1, 0-1 MB L2 opt ECC, MMU + TrustZone</td>
</tr>
<tr>
<td>Cortex-A9[^27]</td>
<td>Application profile, ARM / Thumb / Thumb-2 / DSP / Optional VFPv3 FPU / Optional NEON / Jazelle RCT and DBX, out-of-order speculative issue superscalar, 1-4 SMP cores, MPICore, snooping control unit (SCU), generic interrupt controller (GIC), accelerator coherence port (ACP)</td>
<td>16-64 KB / 16-64 KB L1, 0-3 MB L2 opt parity, MMU + TrustZone</td>
</tr>
<tr>
<td>Cortex-A12[^28]</td>
<td>Application profile, ARM / Thumb-2 / DSP / VFPv4 FPU / NEON / Hardware virtualization, out-of-order speculative issue superscalar, 1-4 SMP cores, Large Physical Address Extensions (LPAE), snooping control unit (SCU), generic interrupt controller (GIC), accelerator coherence port (ACP)</td>
<td>32-64 KB / 32 KB L1, 256 KB-8 MB L2</td>
</tr>
<tr>
<td>Cortex-A15[^29]</td>
<td>Application profile, ARM / Thumb-2 / DSP / VFPv4 FPU / NEON / Integer divide / fused MAC / Jazelle RCT / hardware virtualization, out-of-order speculative issue superscalar, 1-4 SMP cores, MPICore, Large Physical Address Extensions (LPAE), snooping control unit (SCU), generic interrupt controller (GIC), ACP, 15-24 stage pipeline[^25]</td>
<td>32 KB w/parity / 32 KB w/ECC L1, 0-4 MB L2, L2 has ECC, MMU + TrustZone</td>
</tr>
<tr>
<td>Cortex-A17</td>
<td>Application profile, ARM / Thumb-2 / DSP / VFPv4 FPU / NEON / Integer divide / fused MAC / Jazelle RCT / hardware virtualization, out-of-order speculative issue superscalar, 1-4 SMP cores, MPICore, Large Physical Address Extensions (LPAE), snooping control unit (SCU), generic interrupt controller (GIC), ACP</td>
<td>8-64 KB w/optional parity / 8-64 KB w/optional ECC L1 per core, 120 KB-1 MB L2 w/optional ECC shared</td>
</tr>
</tbody>
</table>

[^23]: A. Aloisio
[^24]: 20th IEEE Real Time 2016 - Padua, Italy
[^25]: Cortex-A Cores (32-bit)
[^26]: ARMv7-A
[^27]: Cortex-A8[^26]
[^28]: ARMv8-A
[^29]: Cortex-A12[^28]
[^30]: Cortex-A15[^29]
Beaglebone Black

BeagleBone Black Development Board
(ACTIVE) BEAGLEBK

Key Document
- BeagleBone Black Quick-Start Guide (external link)
  - BeagleBone Black System Reference Manual (external link)
  - View All Technical Documents (8)

Description
BeagleBone Black is a low-cost, open source, community-supported development platform for ARM® Cortex™-A8 processor developers and hobbyists. Boot Linux in under 10 seconds and get started on Stars™ ARM Cortex-A8 processor development in less than 5 minutes with just a single USB cable.

BeagleBone Black ships with the Debian GNU/Linux™ In onboard FLASH to start evaluation and development. Many other Linux distributions and operating systems are also supported on BeagleBone Black including:
- Ubuntu
- Android
- Fedora

BeagleBone Black's capabilities can be extended using plug-in boards called "capses" that can be plugged into BeagleBone Black's two 40-pin dual-row expansion headers. Capses are available for VGA, LCD, motor control, prototyping, battery power and other functionality. More information.

Visit the BeagleBone Black Support Community
AM572x Sitara™ Processors
Silicon Revision 2.0

1 Device Overview

1.1 Features

- For Silicon Revision 1.1 information, see SPR815
- ARM® Dual Cortex®-A15 Microprocessor Subsystem
- Up to 2 C66x™ Floating-Point VLIW DSP
  - Fully Object-Code Compatible With C67x™ and C94x-x™
  - Up to Thirty-two 16 x 16-Bit Fixed-Point Multiplies per Cycle
- Up to 2.5MB of On-Chip L3 RAM
- Two DDR3/DDR3L Memory Interface (EMIF) Modules
  - Supports up to DDR3-1066
  - Up to 2GB Supported per EMIF
- Dual ARM® Cortex®-M4 co-processor
- IVA-HD Subsystem
- Display Subsystem
  - Full-HD Video (1920 x 1080p, 60 fps)
  - Multiple Video Input and Video Output
  - 2D and 3D Graphics
  - Display Controller With DMA Engine and up to Three Pipelines
  - HDMI™ Encoder: HDMI 1.4a and DVI 1.0 Compliant
- 2x Dual-Core Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS)
- 2D-Graphics Accelerator (B32D) Subsystem
  - Vivante™ GC320 Core
  - Video Processing Engine (VPE)
- Dual-Core PowerVR® SGX544™ 3D GPU
- Crypto Hardware Accelerators
  - AES, SHA, RNG, DES and 3DES
- Three Video Input Port (VIP) Modules
- General-Purpose Memory Controller (GPMC)
- Enhanced Direct Memory Access (EDMA) Controller
- 2-Port Gigabit Ethernet (GMAC)
- Sixteen 32-Bit General-Purpose Timers
- 32-Bit MPU Watchdog Timer
- Five Inter-Integrated Circuit (I²C) Ports
- HDQ™/1-Wire® Interface
- Ten Configurable UART/IRDA/CIR Modules
- Four Multichannel Serial Peripheral Interfaces (MCSPIS)
- Quad SPI Interface (OSPI)
- SATA Gen2 Interface
- Multichannel Audio Serial Port (MCASP)
- SuperSpeed USB 3.0 Dual-Role Device
- High-Speed USB 2.0 Dual-Role Device
- PCI-Express® 2.0 Subsystems With Two 5-Gbps Lanes
  - One 2-lane Gen2-Compliant Port
  - or Two 1-lane Gen2-Compliant Ports
- Dual Controller Area Network (DCAN) Modules
  - CAN 2.0B Protocol
- Up to 247 General-Purpose I/O (GPIO) Pins
- Power, Reset, and Clock Management
- On-Chip Debug With CTools Technology
- 28-nm CMOS Technology
- 23 mm x 23 mm, 0.8-mm Pitch, 760-Pin BGA (ABC)
Beagleboard X15

What is BeagleBoard-X15?

BeagleBoard-X15 is the top performing, mainline Linux enabled, power-users’ dream board with a core tailored for every computing task and a high speed interface for every connectivity need. Give your algorithms room to stretch!

**Processor:** TI AM5728 2×1.5-GHz ARM® Cortex-A15

- 2GB DDR3 RAM
- 4GB 8-bit eMMC on-board flash storage
- 2D/3D graphics and video accelerators (GPU)
- 2×700-MHz C66 digital signal processors (DSPs)
- 2×ARM Cortex-M4 microcontrollers (MCUs)
- 4×32-bit programmable real-time units (PRUs)

**Connectivity**

- 2×Gigabit Ethernet
- 3×SuperSpeed USB 3.0 host
- HighSpeed USB 2.0 client
- eSATA (500mA)
- full-size HDMI video output
- microSD card slot
- Stereo audio in and out
- 4×80-pin headers with PCIe, LCD, mSATA
- and much more...

**Software Compatibility**

- Debian
- Android
- Ubuntu
- Cloud9 IDE or Node.js
- plus much more

Register your interest
BEAST dashboard