A Time-to-Digital Converter Based on a Digitally Controlled Oscillator

S. Cadeddu[1], A. Aloisio[2,3], F. Ameli[4], P. Bifulco[2], V. Bocci[4], L. Casu[1], R. Giordano[2,3], V. Izzo[2], A. Lai[1], A. Loi[1], S. Mastroianni[2]

[1]INFN Cagliari, [2]I.N.F.N. Napoli, [3]Università di Napoli, [4]I.N.F.N. Roma

Introduction

Time measurements play a crucial role in trigger and data acquisition systems (TDAQ) of High Energy Physics (HEP) experiments, where calibration, synchronization between signals and phase-measurements accuracy are often required. Although the various elements of a time measurement system are typically designed using a classical mixed-signal approach, state-of-art research is also focusing on all-digital architectures.

We presents a fully-digital TDC application, based on a synthesizable DCO. The TDC has the fundamental task of measuring the phase difference between the 40 MHz LHC machine clock and a digital signal coming from the muon detector with a programmable resolution.
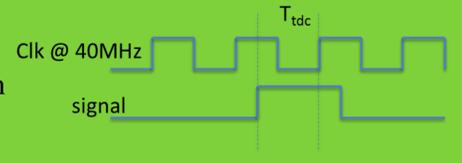
Fundaments and Architecture

The TDC will be used in the new readout chip that is under development for the Muon detector electronic upgrade in LHCb experiment at CERN.

The use of TDC is required to associate the signal observed by the revelator to the bunch collision that generates it. Therefore, TDCs performing the time measures needed to align properly the system in order to reach the required trigger efficiency of 95% in muon identification, which reflects to a requirement of 99% detection efficiency per station, it is crucial to tag each event with the correct Bunch Crossing identifier (BXid).

A simplified block scheme of the TDC architecture is pictured below: during calibration phase, the synthesizable DCO is controlled by a digital Control Logic through a 6-bit encoder. The encoder sets the DCO output frequency clock, which is then used to drive a fast counter performing the phase measurement between the 40 MHz reference clock and the input signal.
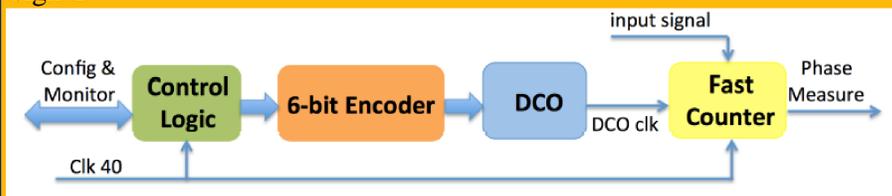

TDC main feature:
- Automatic calibration tool that can be activated on request
- Dithering system to minimize the systematic errors due to discrete delay unit
- TDC measurement is done with a fast counter running with the clock DCO generated
- TDC is active only when a signal arrives, to minimize the switching power consumption.
- The TDC have the possibility to set the resolution in a range from 8 to 32 slices.
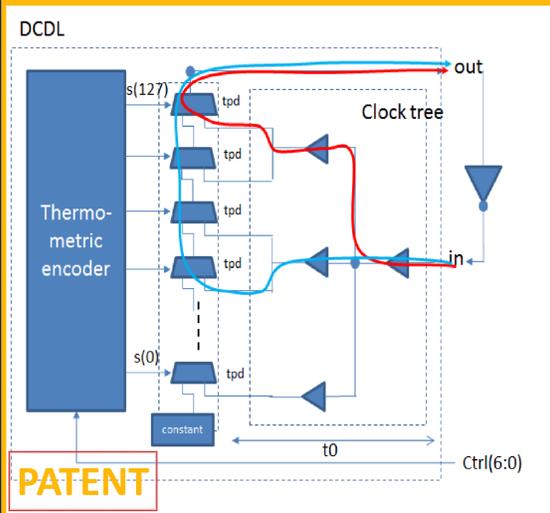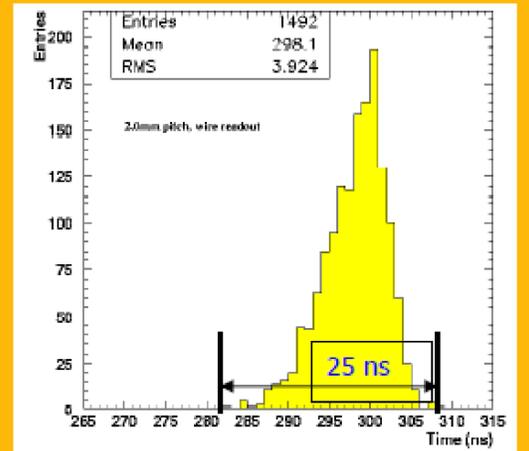
The main part of TDC is a DCO (Digital Controlled Oscillator) based on a high-fan-out network (HFN) feeding a multi-input delay chain. Due to the use of clock tree, a standard element of any digital ASIC, we can guarantee uniform delay between the signal *in* and the input of each delay (t_0). Thermometric encoder determines the number of delay units crossed from *in* to *out* => the total delay $D_t = n \cdot t_{pd} + t_0$, where t_{pd} is the propagation delay of each unit of chain.

The DCO design is technology-independent, it is described by means of a hardware description language and it can be placed and routed with automatic tools.

In the picture aside is showed the layout of a prototype chip ADV2 containing 2 TDCs and 2 DCOs developed to prove the performance of the system.
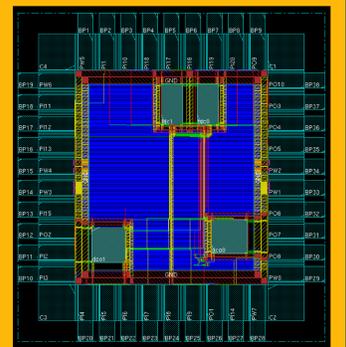
Results and Conclusion
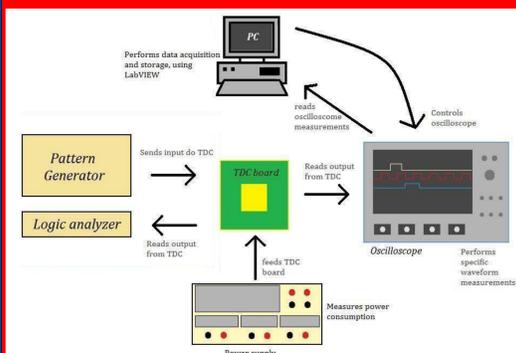
The characterization of TDC and DCO is performed with a setup which consists of a pattern generator with a logic analyzer, a PC to manage acquisition and data storage, the ADV2 test board, a power supply system and an 10GS/s mixed signal oscilloscope.

Main performed measurements for different resolutions are:
- Phase between Signal and Clock
- Current consumption

Quantities obtained from measurements:
- TDC measured time
- Difference between oscilloscope and TDC measured time
- Sigma at different resolutions
- Power consumption Vs signal rate curve
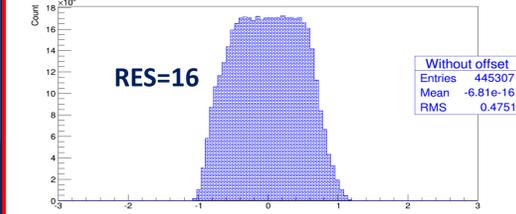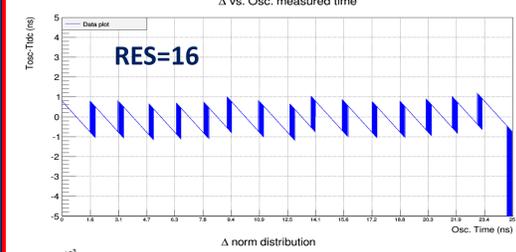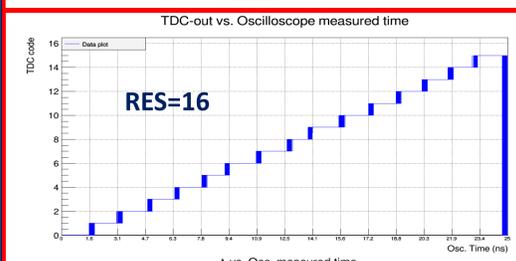
Results show the trend of sigma, when resolution changes, compared with theoretical RMS. It is clear how the curves look very similar, especially for the LHCb resolution, that is 16.

The power consumption graph shows the behavior of TDC: when it is quiet the current consumptions is around 20uA, while when the signal rate increases the average consume can be seen as the value (300uA) at the maximum signal rate the TDC can sustain. This is in accord with the simulation results, where it was achieved a consume of some hundreds of uA.