

Design and Testing of the bunch-by-bunch Beam Transverse Feedback Electronics for SSRF

Jinxin Liu, Lei Zhao, *Member, IEEE*, Linsong Zhan, Shubin Liu, *Member, IEEE*, and Qi An, *Member, IEEE*

Abstract—Shanghai Synchrotron Radiation Facility (SSRF), is one of the third-generation high-beam current (3.5GeV) synchrotron light sources. In the storage ring of SSRF, multi-bunch instabilities would increase beam emittance and energy spread, which degrade beam quality and even cause beam loss. To address the above issues, a Transverse Feedback System is indispensable for SSRF, in which the key component is the bunch-by-bunch transverse feedback electronics. The whole feedback system consists of five main parts: BPM, RF front-end, signal processor, RF amplifier, and vertical/horizontal transverse kickers. The dissertation focuses on the signal processor we design, which is the main part of the feedback electronics. We conducted initial testing on the signal processor to evaluate its performance and function. The typical frequency spectrums analysis (with input frequency of around 100 MHz) of the ADC output signals indicates that the SINAD (Signal-to-Noise and Distortion Ratio) is 63.69 dB and the ENOB (Effective Number of Bit) is 10.3 bit. The test results of ENOB with different input frequency indicate that it is better than 9.5 bit in the input frequency range up to 300 MHz, which is good enough for the application. Besides, the test results of the hardware and the results of the MATLAB model concord well with each other, which means that we have achieved the functionality as expected.

I. INTRODUCTION

SHANGHAI Synchrotron Radiation Facility (SSRF) is one of the third-generation high-beam current (3.5GeV) synchrotron light sources. In the storage ring of SSRF, multi-bunch instabilities would increase beam emittance and energy spread, which degrade beam quality and even cause beam loss. To address the above issues, a Transverse Feedback System is indispensable for SSRF, in which the key component is the bunch-by-bunch transverse feedback electronics [1].

The whole feedback system consists of five main parts: BPM, RF front-end, signal processor, RF amplifier, and vertical/horizontal transverse kickers, as shown in Fig. 1.

The RF front-end imports the signals from the BPM, and then filters them. The signals are input to the signal processor to

calculate the feedback coefficients that are converted to controlling voltages through high-speed DACs (Digital to Analogue Converter). These voltages are then amplified and used as the input of the kickers to tune the beam into the optimum orbit [2] [3]. The main part in the feedback electronics is the signal processor, which is discussed in the following sections.

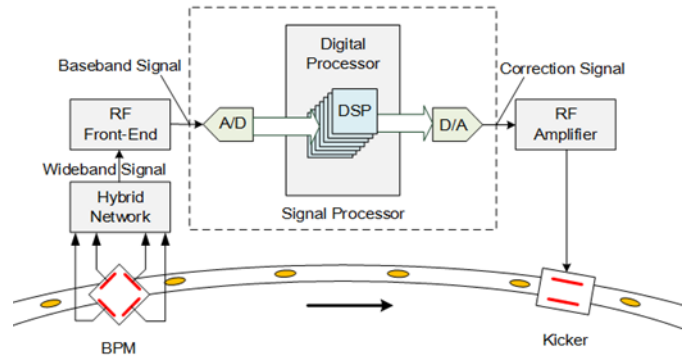


Fig. 1. The overview over the transverse feedback system.

II. SYSTEM DESIGN

Fig. 2 shows the structure of the signal processor.

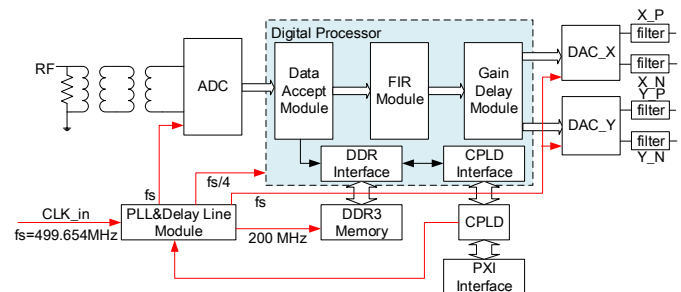


Fig. 2. Block diagram of the signal processor.

The signals from the BPM are pulses with a repetition frequency of 499.654 MHz, and each pulse corresponds to one beam bunch. The sampling frequency of the ADC (Analogue to Digital Converter) is also set to 499.654 MHz to digitize the bunch-by-bunch signal. PLL based clock generation circuits are designed to synchronize the sampling clock with the system of the accelerator, as shown in Fig. 2. The input signals of the signal processor are the outputs of the RF front-end which filters the signals from BPM to a bandwidth below 250 MHz. A 12 bit 500 Msp/s ADC chip AD9434 is employed in this design. The

Manuscript received June 3, 2016. This work was supported by Knowledge Innovation Program of the Chinese Academy of Sciences (KJCX2-YW-N27), National Natural Science Foundation of China (11205153) and CAS Center for Excellence in Particle Physics (CCEPP).

The authors are with the State Key Laboratory of Particle Detection and Electronics, University of Science and Technology of China, Hefei, 230026; and Modern Physics Department, University of Science and Technology of China, Hefei, 230026, China (telephone: 086-0551-63607746, corresponding author: Lei Zhao, e-mail: zlei@ustc.edu.cn).

output of the ADC are then fed to an FPGA (Field Programmable Gate Array) to calculate the feedback coefficients based on FIR (finite impulse response) filters in it [4] [5].

The block diagram of the Digital Signal Processing (DSP) algorithms in the FPGA is shown in Fig. 3. The data from the ADC are first deserialized to four 125 Msps data streams. The information of each bunch is extracted from the data stream using shift registers and then processed by FIR filters to obtain the feedback coefficient. This coefficient can also be adjusted with different gains that can be controlled via remote PC. To make sure that the kicker takes effect on the correct bunch, the algorithm also contains the delay function with a step size of 4 ns. Combined with the external delay line chips, a fine delay step size of 10 ps and a range of 2 μ s can be achieved. The output of the FPGA are then converted to analog voltages by 500 Msps DAC chip AD9436.

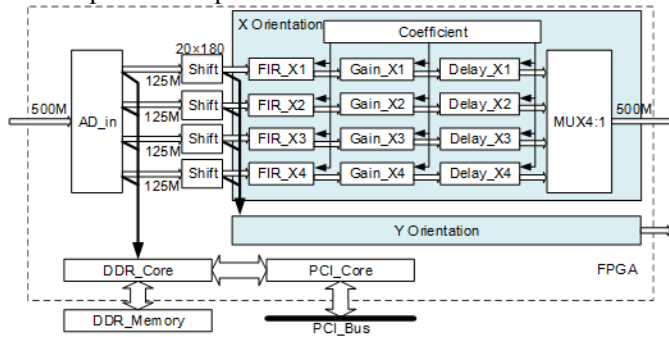


Fig. 3. Block diagram of the digital signal processor algorithm.

III. SYSTEM PERFORMANCE TEST

We also conducted initial testing on the signal processor to evaluate its performance and function.

A. ADC Performance Test

The high-speed high-resolution A/D conversion is a crucial part in the system. We performed the ADC dynamic analysis based on the IEEE Std.1241-2010 [6] to assess the circuit performance. SMA 100A, a high performance signal source, is used to generate input sine wave signals from 10 MHz to 800 MHz. Then the signal is filtered by a coaxial Band Pass Filter (BPF) and imported to the signal processor for digitization.

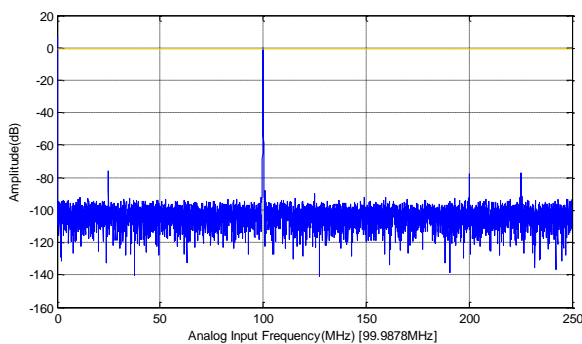


Fig. 4. Typical frequency spectrums of the ADC output.

Fig. 4 shows the typical frequency spectrums (with input frequency of around 100 MHz) of the ADC output signals. The SINAD (Signal-to-Noise and Distortion Ratio) is 63.69 dB and the ENOB (Effective Number of Bit) is 10.3 bit.

We also changed the input signal frequency and obtained a series of test results, as shown in Fig. 5. The results indicate that an ENOB better than 9.5 bit in the input frequency range up to 300 MHz is successfully achieved, which is good enough for the application.

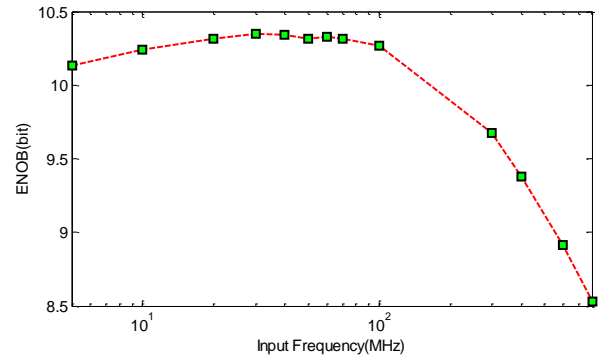
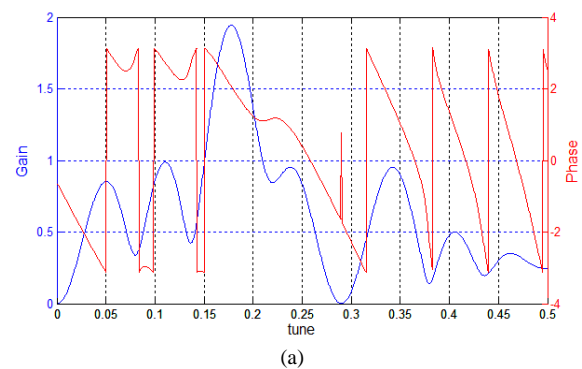


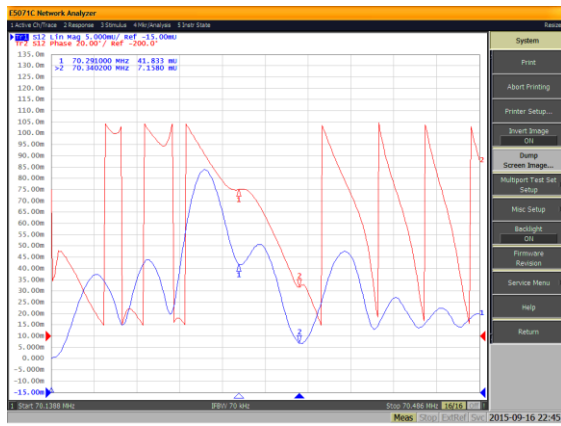
Fig. 5. ENOB curve along with input frequency changing.

B. Functionality Test

We also conducted tests to assess the function of the signal processor. We established a model according to the requirement of the signal processor on the platform of MATLAB, and then we obtained the frequency response of the expected feedback function. Then we used the network analyzer Agilent E5071C to obtain the actual frequency response of the signal processor by sweeping frequency in the range from 0 to 356.982 kHz. This frequency corresponds to the turn-by-turn repetition frequency of 693.964 kHz (499.654 MHz/720), since 720 bunches are circulated in the storage ring with a duty ratio of 500:220.

Fig. 6 (a) shows the results of the MATLAB model, and Fig. 6 (b) shows the test results of the hardware, which concord well with each other. This means that we have achieved the functionality as expected.





(b)

Fig. 6. The spectrum of simulating and testing frequency response. (a) MATLAB simulating results; (b) testing results. The blue curve is the amplitude-frequency response, and the red curve is the phase-frequency response.

IV. CONCLUSION

A bunch-by-bunch beam transverse feedback electronics was designed for the SSRF. Through high-speed high-resolution Analog-to-Digital conversion, DSP algorithms in FPGA, and high-speed Digital-to-Analog conversion, the feedback controlling voltage can be obtained for each bunch. Initial tests were also conducted, and the results indicate that an ENOB better than 9.5 bit is achieved in the frequency range up to 300 MHz, and the functionality of this system also concurs well with expected.

REFERENCES

- [1] L. Han, R. Yuan, L. Yu, and K. Ye "Front-end signal analysis of the transverse feedback system for SSRF" in Nuclear Science and Techniques, 2008, 19(5): 274-277.
- [2] S. Khan, T. Knuth, W. Barry, J. Byrd, and G. Stover, "COMMISSIONING RESULTS OF THE TRANSVERSE FEEDBACK SYSTEM AT BESSY II" in Proceedings EPAC2000, Vienna, Austria. 2000.
- [3] M. J. Spencer, G. Leblanc, and K. Zingre, "DESIGN AND COMMISSIONING OF A BUNCH BY BUNCH FEEDBACK SYSTEM FOR THE AUSTRALIAN SYNCHROTRON" in Proceedings of EPAC08, Genova, 2008: 3306.
- [4] W. Höfle, G. Kotzian, E. Montesinos, M. Schokker, D. Valuch, and V. M. Zhabitsky, "BEAM TESTS OF THE LHC TRANSVERSE FEEDBACK SYSTEM" in Proceedings of RuPAC, 2010: 275-279.
- [5] W. Z. Wu, Y. Kim, J. Li, P. Wang, M. Busch, G. Swift, and Y. K. Wu, "DEVELOPMENT AND COMMISSIONING OF BUNCH-BY-BUNCH LONGITUDINAL FEEDBACK SYSTEM FOR DUKE STORAGE RING" in Proceedings of 23-rd Particle Accelerator Conference. 2009.
- [6] IEEE Standard for Terminology and Test Methods for Analog-to-Digital Converters, IEEE Std. 1241-2010, Jan. 2011.