Online calibration of the TRB3 FPGA TDC with DABC software

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Abstract
The TRB3 - Trigger Readout Board - features 4 FPGA based TDCs with a total of up to 264 channels and a time precision of 8 ps RMS [1]. It was applied for various beam tests and is going to serve as a standard DAQ hardware for FAIR detectors, such as HADES, PANDA, and CBM. To achieve the best time precision, however, each TDC channel must be calibrated individually.

First of all, fine counter calibration should be done by means of random test inputs and it should be repeated, if the calibration function changes (in most cases due to temperature change). Additionally, temperature dependency of each channel can be calculated in advance and compensated using the temperature information from the sensors around the FPGAs. Another compensation should be applied to the mean value determination caused by the temperature change. And finally, stretchy latency (used for TDC measurements), which also depends on the temperature change, should be measured in advanced and compensated during the measurements.

All these calibration tasks can be carried out already during data taking within the event building DAQ software DABC. Produced time values can either be stored with the original raw data or replanned. The calibration analysis code has been implemented with the C++ stream framework and can run as plug-in for DABC as well as with ROOT-based analysis environments, like HYDRA or G4.

An HTTP server in the DABC process provides online monitoring and control of the TDC calibration from a standard web browser.


TRB3 hardware
- Main board with 5 Lattice ECP3 reduced variant
- 8 SFP connectors
- 4 peripheral FPGAs as TDCs with 260 channels
- central FPGA for trigger system and G&H controller
- TofIn (control) and UDP/IP & G&E (data) protocols
- 8 SFP connectors
- 4 highspeed 288 pin connectors for various Adapters
- 6 part hubs, NAMECIC, ADC, 100M ps, PADIWA...
- reduced variant TRB3c exists (1 FPGA each for 19" crate system)

FPGA TDC
- Time stamp
- TDC_C014/D1 Fast rising front
- TDC_C014/D1 Rising calibration function
- Data file directory
- The control panel
- The complete DAQ process, including data taking, TDC calibration and files storage, can be monitored and controlled by a web interface. One can also access various histograms produced in the TDC calibration process. This web UI has been implemented using the JavaScript ROOT library (http://root.cern.ch).

Timestamp counters
Dump of acquired TRB3 TDC data with DABC hdpin utility:

```
[SP:40627065] 0 809372f3 8051aae9
[SP:40627065] 1 809372f3 8051aae9
[SP:40627065] 2 809372f3 8051aae9
```

The hit time $t_{\text{stamp}}$ is evaluated from epoch marker, coarse counter $t_{\text{coarse}}$, and calibrated fine counter $t_{\text{fine}}$, as denoted by different colors:

$\text{t}_{\text{stamp}} = (\text{epoch} \times 2048 + \text{t}_{\text{coarse}}) \times 5\text{s} = \text{Calibr}_{\text{fine}}$

The Time over Threshold $T_o_T$ is derived from consecutive hits with “rising edge” and “falling edge” properties (“rising” 1 or 0):

$T_{oT} = t_{\text{stamp}}_{\text{rising}} - t_{\text{stamp}}_{\text{falling}}$

Statistical calibration approach
Assuming input signals with an uniformly fine time distribution, the TDC fine time counter values should also be uniformly distributed in the ideal case. The measured deviations from such uniform distribution can be used to evaluate a fine time counter calibration $Calibr_{\text{fine}}$. Practically this can be implemented as lookup-table or as parameterized function. This calibration requires, however, a sufficient statistics of acquired time values (“hits”) for each TDC channel. The calibration procedure may be performed with special triggered signals either once before the actual detector data taking, or it may be repeated frequently, e.g. during accelerator spill pauses.

Temperature dependency
Temperature significantly affects the FPGA TDC fine-counter calibration function. A difference of several degrees K leads to increase of timing errors in 20-40 ps, which is much higher than obtained 8-12 ps resolution of a TDC with constant temperature. To avoid such effects, temperature should be stabilized or calibration should be repeated constantly, taking into account any possible changes.

The described correction compensates most temperature effects on fine-counter calibration. Since a temperature sensor near each FPGA is continuously read out, such correction can be applied online during data taking. The resulting precision of time measurement in 55°C temperature range remains below 10 ps.

ToT temperature corrections
Time over Threshold (TOT) values measured with the FPGA TDC are also affected by temperature. Both the fine time counter calibration and the stredger offset for the trailing edge signal are temperature dependent. This determination of ~100 ps °C can be compensated by individual channel calibration with a pulser signal of known TOT. Such correction can be applied in stream/DABC software already during data taking, since the actual temperature data is also read out from the FPGA. Taken from [1].

Online software
Data acquisition for TRB has been implemented with DABC framework (http://dabc.gsi.de). UDP packets, retrieved from several TRB boards, are verified, filtered and combined together into HL6 formatted events, which are then stored on disk.

The code for FPGA TDC calibration and temperature compensation has been implemented with C++ based stream framework (https://root.cern.ch/twiki/bin/view/ROOTWeb/StreamAnswer). This code can be embedded into various high level frameworks, like ROOT, G4, DABC or HYDRA. DABC allows to run TDC calibration code directly in the DAQ process, providing ready-to-use data for further analysis. This simplifies the task of building heterogeneous suites, where different kinds of TRB boards (with and without TDC) can be used. The same code can be run also offline, using HL6 files as inputs. All stages can be monitored with G4 GUI or with a web-based UI.