Field Waveform Digitizer for BaF_2 Detector Array at CSNS-WNS

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1. Introduction

In CSNS-WNS (White Neutron Sources at China Spallation Neutron Source), BaF_2 (Barium fluoride) detector array is designed for neutron capture cross-section measurements with high accuracy and efficiency. Once proton beam collides with the target specimen, neutron will be excited and flight from the target to BaF_2 array. The time of flight corresponds to the energy of the neutron. To identify signals from BaF_2 crystal excited by which particle, alpha or gamma, pulse shape discrimination technique is usually adopted according to the ratio of fast and slow components in the signal. Waveform digitization is a valid supporting technology for pulse shape discrimination. Conventionally, two digitization channels are used for one crystal segment so as to capture both higher and lower detector signals. To precisely obtain the wave and time information carried by detector signal, and maximally cover the dynamic range of signal, high speed ADC with sampling rate of 1 GSps and 12-bit resolution is used in the readout system for CSNS-WNS BaF_2 detector array. The detector array consists of 92 BaF_2 crystal elements with completely 4π solid-angle coverage, which results in 92 analog channels for waveform digitization and time of flight measurement in total. High speed, high resolution and large number of channels inevitably lead to the data amount increasing drastically. To read the massive data out in real time, PXIe platform is adopted for data readout. In each PXIe crate, there are several field digitizer modules (FDM) for waveform digitization. Besides, there also are several modules for clock and trigger signals distribution.

2. IMPLEMENT OF THE FDM

As illustrated in Fig. 1, each FDM is composed of analog signal conditioning, ADC, clock synthesis, FPGA, DDR3 ping-pong memories, and PXIe readout interface etc.

To digitize up to 92 detector channels, there are 46 FDMs each of which has two digitizing channels. FDMs are settled in 4 distributed PXIe crates, which makes the readout system a distributive architecture. The analog signal from detector is signaled with differential level and fed into an anti-aliasing filter to filter out unwanted harmonics before entering ADC. To transmit massive data in real time, FDM is integrated with PXIe interface based on FPGA and designed as a standard PXIe 3U module. Two DDR3 memories works in Ping-Pong mode to reduce dead time of data readout. The capacity of each memory is up to 4G bit, which makes it benefit for caching data with long sampling period when receiving, processing and transmitting data on board. Besides a spare local clock source, FDM also receives the reference clock from PXIe differential star bus to synchronize itself with the global clock precisely. The clock synthesis module cleans jitter, synthesizing frequency and then feeds the high quality clock to ADC and FPGA. To eliminate invalid data, external trigger signal can be fed into FDM through PXIe backplane star bus or micro-miniature coaxial cables from front-panel.

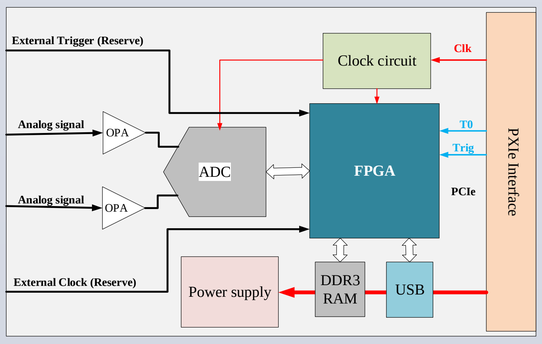

Fig. 1. Block diagram of FDM

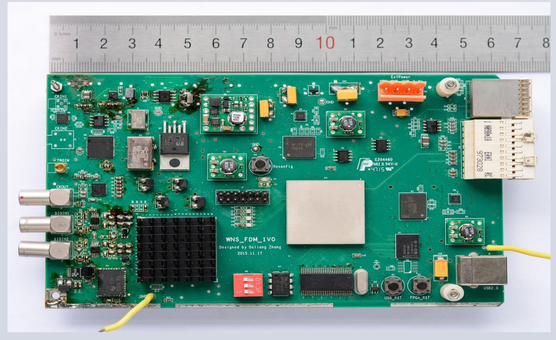

Fig. 2. Photograph of the FDM

On each FDM module, FPGA takes the task of data acquisition and processing in real-time. The logical structure in FPGA is shown in Fig. 3. In order to process data in FPGA easily, the input stream of each ADC channel at 12Gbps line baud rate is split into 2 streams concurrently. The line rate for each stream is down to 6Gbps that is reasonable for FPGA processing. Data acquisition is running in trigger mode. Once a valid trigger signal occurs, in each branch, data cell will be extracted as soon as possible from bit stream and stamped with a trigger ID. On the contrary, data cell will be discarded if there is no valid trigger signal.

Time of flight (TOF) can denote the energy of neutron. In BaF_2 readout electronics, TOF measurement is achieved by a TDC (Time to Digital Converter) implemented in the FPGA on FDM. The T0 signal denoted as the start time triggers TDC measuring. While a specific trigger signal denoted as the stop signal finishes the process of time measuring and triggers a valid data buffering for output. Besides the trigger ID stamp, each data packet is also stamped with time information by this TDC.

After being deserialized, stamped with trigger and time information, package stream is ready for readout. However, besides the trigger driven process of data readout, to reduce the pressure of readout, data package is compressed with zero compression algorithm in real time. Thus the data rate can further be decreased.

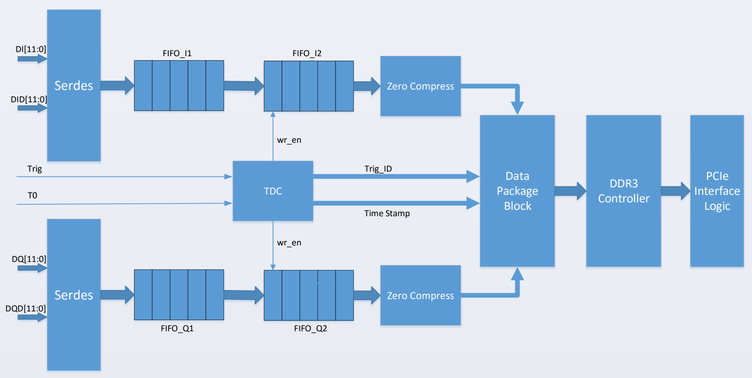

Fig. 3. The logical structure of FPGA

In Fig. 3, there are also some modules, such as DDR control, PCIe interface. They are used to transmit data to crate controller through PCIe bus on back plane.

Actually, with the technique of waveform digitization and utilizing of FPGA with reconfigurable firmware, FDM can be easily considered as a universal digitization platform with advantages of scalability and versatility. By taking full advantages of FPGA resource and waveform digitized data, FDM can also run with full digital trigger mode, which can make it possible to remove most traditional analog trigger cables. Readout electronics with digital trigger mode has clear advantages of simplicity and ability of reconfiguration for trigger algorithm. Based on this digital platform, pulse shape discrimination algorithm can be implemented in FPGA.

3. EXPERIMENTS AND VERIFICATION

To verify the design of FDM proposed in this paper and evaluate its specification, a 3U FDM prototype has been implemented. A sine waveform with the frequency of 98.740MHz is used for the ADC evaluation. As shown in Fig. 4, the SNR (Signal to Noise Ratio) can reach to 56.23 dB. The ADC's INL (Integral Non-Linearity) is range from -2.5 LSB (Least Significant Bit) to +1.5 LSB and the DNL (Differential Non-Linearity) is range from -0.2 LSB to +0.2 LSB. As shown in Table. 1, The data rate of FDM via PCIe bus with DMA method is also evaluated.

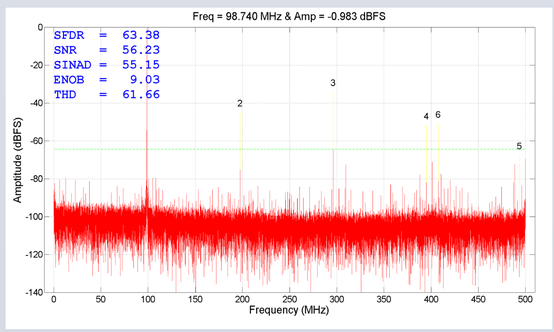

Fig. 4. A Test Result of the ADC evaluation

Lane Width	MPS	Theoretical estimation data rate（DMA）	Measured data rate（DMA）
x1 lane（Gen1）	256B	1.852Gbps	1.820Gbps
x1 lane（Gen2）	256B	3.704Gbps	3.632Gbps
x2 lane（Gen1）	256B	3.704Gbps	3.640Gbps
x2 lane（Gen2）	256B	7.408Gbps	7.285Gbps
x4 lane（Gen1）	256B	7.408Gbps	7.283Gbps
x4 lane（Gen2）	256B	14.816Gbps	14.568Gbps
x8 lane（Gen1）	256B	14.816Gbps	14.588Gbps

Table. 1. Transmission rate of PCIe bus on FDM

4. CONCLUSION

Field waveform digitizer for BaF_2 detector array at CSNS-WNS is proposed in this paper. It has the ability of digitizing analog signal at 1GSps sampling rate with 12-bit resolution. Compared with traditional neutron facility, it has advantages of simplicity, high resolution, ability of reconfigurable for data processing and trigger algorithm. Each digitizing channel can cover the high dynamic range of a BaF_2 detector channel with the advantage of high resolution. To measure neutron time of flight, a FPGA TDC is implemented in each digitizer. As a flexible, versatile, scalable waveform digitization platform, full digital trigger mode and real time data compress algorithm can be implemented in FDM.