Contribution ID: **41** Type: **Poster presentation**

Readout System with 2-Channel 8-Bit 1GHz FADC and Gigabits Ethernet Based on RAIN1000Z1 ZYNQ Module for Crystal Detector

Friday, June 10, 2016 10:30 AM (1h 35m)

RAIN1000Z1 is a high performance readout module we developed last two years. It is based on the ZYNQ architecture SOC chip from Xilinx and ZYNQ is the new architecture of FPGA with dual high performance ARM Cortex-A9 processors and high capacity programmable logic. We developed a series of readout system with the RAIN1000Z1 module based on ZYNQ architecture. For the crystal detectors, such as CsI(Tl) crystal detector we used for neutron background measurement in the CJPL (China JingPing under-ground Lab) experiment, we developed a two channels 8-Bit 1GHz FADC readout system with RAIN1000Z1 module. With the two PMTs in the dual end of crystal detector, the analog signal is send to FADC and the digital results is triggered and anticoincidence in the FPGA logic, the final data is send to computer by gigabits Ethernet with ARM processor running Embedded Linux. HMCAD1511 from ADI is used for 8-Bit 1GSPS analog data converter, and the high speed, low jitter 1GHz clock is generated by LMK04803B from TI. With the benefit of high bandwidth and high performance inter connected HP bus between ARM processor (PS) and FPGA logic (PL), the FADC's data gathered by FPGA logic is buffered and transferred to the ARM processor's DDR3 SDRAM running at 1066MHz with CDMA function without many CPU time. The readout interface's data throughput can reach more than 600Mbps with gigabits Ethernet. In this paper, details of the hardware design and HDL design will be introduced.

Primary author: Dr XUE, Tao (Tsinghua University)

Co-authors: Dr GONG, Guanghua (Tsinghua University); Dr LI, Jianmin (Tsinghua University)

Presenter: Dr XUE, Tao (Tsinghua University)

Session Classification: Poster Session 2

Track Classification: Front End Electronics and Fast Digitizers