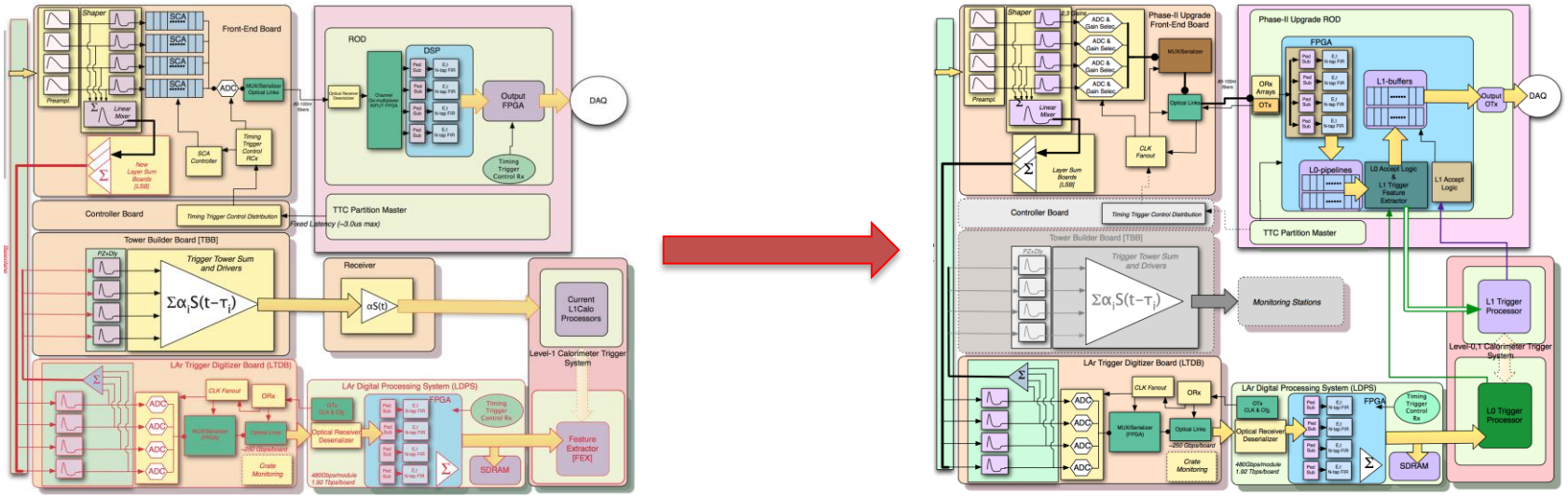
Development of ATLAS Liquid Argon Calorimeters Readout Electronics for HL-LHC

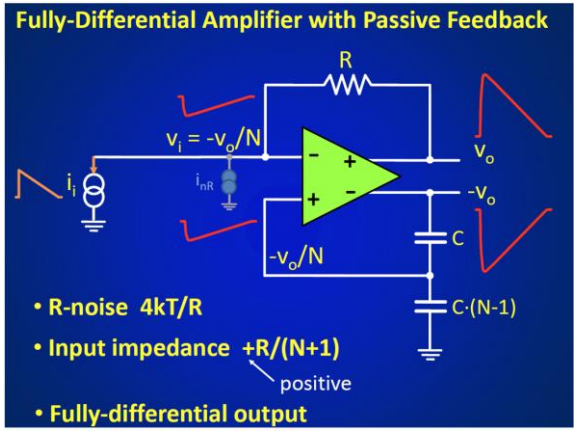


Upgrade of the readout architecture from Phase-I to the HL-LHC

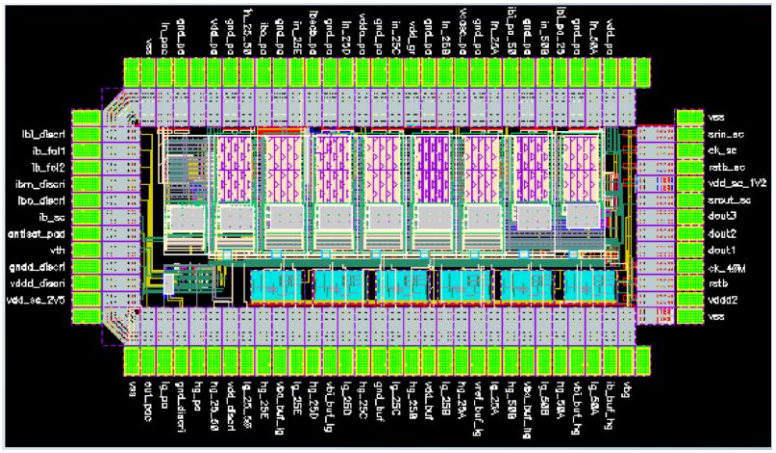
- New Front-End board:
  - Amplifier, shaper, ADC, serializer are under research & development
  - The best result will be to integrate these ASIC designs in one FESOC (Front-End System On Chip)
- New Back-End board:
  - Digital shaping and high performance filtering will be implemented.
  - The LDPB (LAr Digital Processing Blades) board of Phase-I upgrade will be used as prototype.

Kai Chen, on behalf of the ATLAS Liquid Argon Calorimeter Group

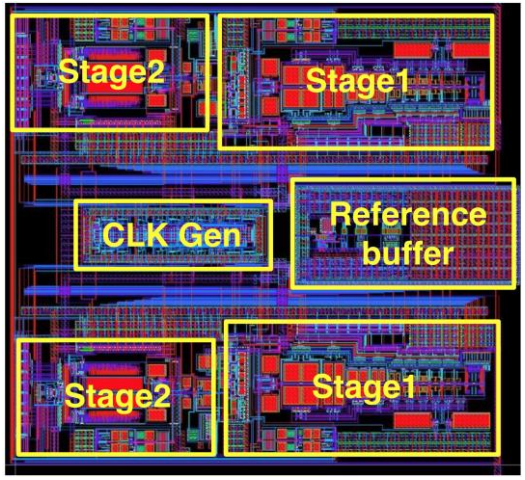
Development of the ASICs for the Front-End Board



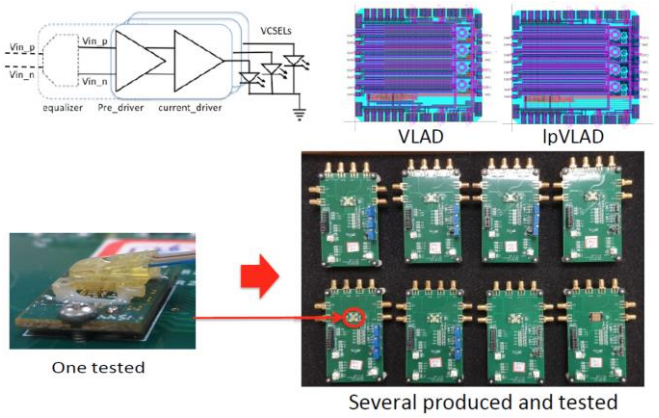
The fully-differential amplifier (65 nm CMOS technology, 1.2V)



Layout of the line-termination preamplifier (130 nm CMOS technology, 2.5V)



The split-SAR ADC (65 nm CMOS technology), preliminary results:12.1 bits ENOB



The optical transmitter VLAD (VCSEL Array Driver): 65 nm, 20 mW/ch for lpVLAD