A cosmic ray readout system for qualifications of small-strip Thin Gap Chambers of the ATLAS Muon Spectrometer Phase-I upgrade

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System Development

Fig. 1 The block diagram of the cosmic ray readout system.

Fig. 2 Photo of the pFEB

Fig. 3 Interface of the host computer software
Experiment Results

Fig. 1 The analog signal of sTGC pads

Fig. 2 The charge distribution of sTGC pads signals
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Introduction
The ATLAS experiment at the CERN Large Hadron Collider (LHC) will be upgrading its Muon Spectrometer during LHC phase-I upgrade in around 2021 to benefit from high luminosity and high energy runs at the LHC. The upgrade will replace the innermost detector, namely the Small Wheel (SW) of the Muon Spectrometer in the forward region with the so-called New Small Wheel (NSW). In order to improve its Level-1 trigger in the high background rate environment, the NSF employs two types of high rate capable gas electron detectors: namely Microstrip Gas Electron Delay Line (MGD) and small-strip Thin Gap Chamber (STGC). For on-line reconstruction of muon segments with pointing accuracies of 1 mm, STGC primary triggers similar to those Thin Gap Chambers (TGC) are present in the present ATLAS Muon Spectrometer but with the readout strips, which allow about 4096 readout channels to discriminate bunch crossing in 20 ns and determine hit positions with a precision of about 100 pm per readout layer. Stringent requirements on the timing and spatial measurement performances, large number of readout channels all impose significant challenges to both the detector construction as well as readout and control system design. The readout front-end boards under development for the TGC detector will carry four to eight 54-channel embedded analog and digital ASIC, four trigger data processing ASICs as well as readout and control chips. These boards are expected to carry hundreds of channels of sensitive analog signals as well as high speed serial links with speeds up to 4 Gbps to output trigger data off-detectors. Large amount of data is to be processed on detector and moved out in both trigger and precision readout paths with low latency requirement are of big concern. We will present the development of the first prototype of the front-end board for the TGC detector, readout firmware and firmware for the mini data acquisition system that has been used to characterize the amplifier and digitizer ASIC as well as for integration test with a prototype detector. Results from the front-end board and the prototype detector integration as well as plans to develop a full data acquisition system to verify the front-end electronic design will be discussed.

The block diagram of the cosmic ray readout system

The signals of the STGC prototype detector pads and wire are gathered by an adopt board and then come through the GTF connector to the STGC. The GTF connector has 1730 pads and 256 channels will be used for signal channels and others will be used as ground connections. The 256 signal channels will be sent into the VAMs chip, which is an application-specific integrated circuit (ASIC), that is designed specifically to amplify, shape, and digitize the signals from the chambers. Information on amplitude and timing of each hit will be passed to the GTF connector. The GTF connector will be used for communication via Ethernet, including receiving commands and configuration data and sending data processed from VAM.

The typical analog signal of the STGC pad signal

The amplitude distribution of the STGC pad signal

Conclusion
In this paper, a cosmic ray readout system has been built for small-strip Thin Gap Chamber (STGC) qualification. We designed the pads from front-end board and a CAM prototype based on FPGA and Ethernet communication to PC and external trigger acceptance. Test results show that the system is able to measure the noise-reject, efficiency, amplitude and timing which is important for STGC qualification.