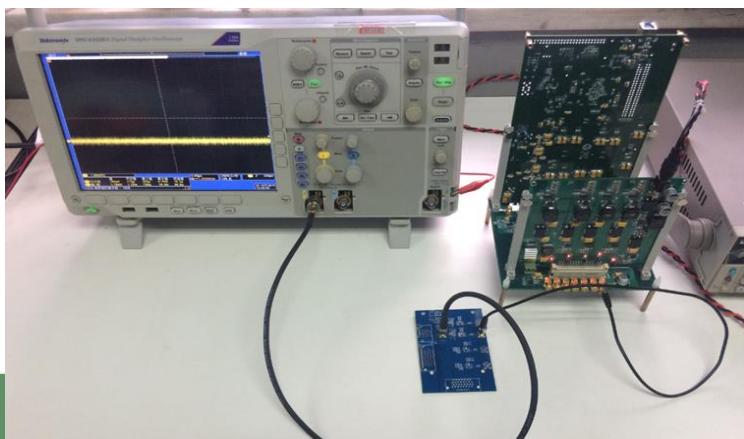
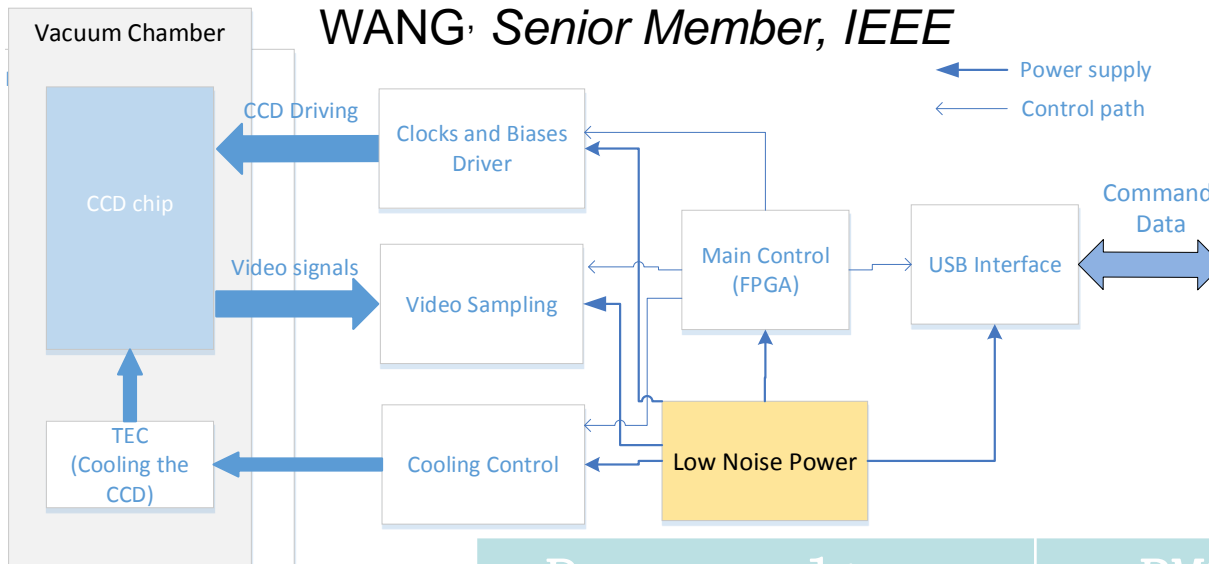




Design of Ultra-low Noise Power System for High-precision Detectors

Jian-min Wang, Hong-fei Zhang, Sheng-zhao Lin, Yi Feng, Dong-xu Yang, Jian

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Power voltage	RMS Noise
+17V	64.8 μV
-17V	66.8 μV
+5V	40.7 μV
-5V	40.7 μV
+33V (Bias Power)	31.0 μV

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Introduction

1. Introduction

Scientific CCD detector systems are widely used in many areas as high-energy physics, nuclear physics and astronomy for its high quantum efficiency and low readout noise. For example, some experiments as soft-x-ray CCD imaging, dark matter search based on CCD, astronomical optical band CCD imaging, infrared CCD camera could benefit from ultra-low noise readout of scientific CCD systems. The functional structure of our scientific CCD detector system developed for Antarctic is shown as Fig.1

The Low Noise Power module supplies power for each part of the system, especially supplies ultra-low noise power for the Clock and Biases Driver module and the Video Sampling module. Its performance will influence the performance of whole CCD controller.

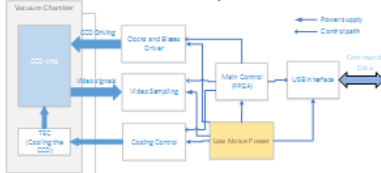


Fig. 1 Functional structure of the scientific CCD detector systems

2. SYSTEM DESIGN

front-end electronics (FEE) of the detector system is generated. The FEE mainly consists of the clocks and biases circuit for driving the CCD, the CCD signal processing circuit and AD circuit for sampling the CCD outputs. The power noise of the biases circuit and the CCD signal processing circuit need to be under $40\mu V_{rms}$, the power noise of the clocks circuit could be a little higher as about $1mV_{rms}$. The third part is the digital controlling circuit including FPGA, clock chip and USB interface chip etc., the power noise requirement of which is just about $1mV_{rms}$ also. The power supply structure of the CCD detector system shown as fig. 2.

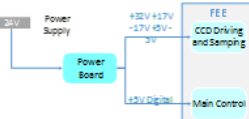


Fig. 2 Power supply structure of the CCD detector system

A mother board (MB) is designed and reliable connectors are used between the power board (PB) and the FEE. Meanwhile the MB is connected with CCD detector through vacuum connectors, immobilizes the PB and the FEE, and transfers power from the PB to the FEE. With this structure, a long cable is avoided to be used to transfer power. Thus noise coupling and voltage drop loss is decreased without the long cable. The MB supplies an integrated analog ground plane for protecting the power signals, and increases the filter circuit to reduce the power noise even further. In the scientific CCD detector system, the MB also supply connects and preamplifier circuits for the CCD output signals. The structure of the system consisted with the PB, the MB, and the FEE is shown as Fig. 3.

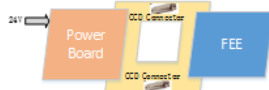


Fig. 3 Connecting structure of the power supply system

3. POWER GENERATION AND FILTERING

In the power system a 24V power input is used. DC-DC power converters are used to generate multi-channel voltages. The energy conversion efficiency is very high in this way, and it's convenient to convert the 24V to multi-voltages of system requirement. But the power noise of the DC-DC devices is usually as high as about $100mV$, so it is much higher than the demand of the ultra-low noise power. Thus it is necessary to use multi-stage filters to absorb the ripple and use low dropout regulator (LDO) which has very low output noise.

When the power generated by LDO is transferred to the MB from the PB and to the FEE from the MB through connectors, filter circuits are used once more to insure the noise power is as low as expect. The figure 3 shows the structure of the power generating from the 24V power input to the multistage filters.



Figure 3 Block diagram of the power generating and filters of the power system

The filter is mainly consist of capacitor and BNX024H01, which can filter noise in specific bandwidth precisely. As for DC-DC part we use TPS55340 and LM2576, the ripple amplitude of the two chips is small. Further, we use TP57A47/TP57A33 series chip to decrease noise. On the MB&FEE, there is similar structure to reduce EMC and temperature resistant.

4. Test

The power system has been tested for noise performance, efficiency, stability, low temperature environment as shown in Fig.4. The noise of every channel of the power system has been tested. The result is shown in Table 1.

Table 1 Result of noise of five channels

Power voltage	RMS Noise
+17V	64.8 μV
-17V	66.8 μV
+5V	40.7 μV
-5V	40.7 μV
+33V(Bias Power)	31.0 μV

Fig.4 the power noise testing system

In order to know the power density distribution of the power channels, the power channels were also measured by a spectrum analyzer to obtain the noise spectrum as shown in Fig.5. Additionally, in order to test the stability of the system in the low temperature environment, a refrigerator which can simulate the low temperature environment as low as 193K is used to test if the output voltages of the power system are normal and stable. The figure 6 shows the +33V voltage changing with temperature range from 260K to 193K.

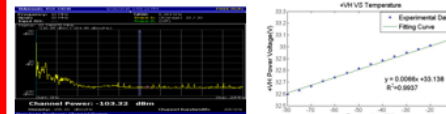


Fig.5 Spectrum measured by the spectrum analyzer

Fig. 6 +33V voltage change V_o versus temperature.

The linearity of the fitted curve is about 99.37%, and the change range of the voltage less than 0.5V. It is worth mentioning that the controller of the CCD detector system has the function of monitoring and calibrating, which can adjust the voltages accurately when temperature changes. Besides, the power system has been tested for 7*24 hours continuous work in the 193K environment.

The ultra-low noise power supply system plays an important role in a variety of detector readout electronics systems. we implement multi-channels power generation with noise below $40\mu V_{rms}$, by using DC-DC and LDO chips, multi-stage filters, secondary LDO, reliable and short connectors instead of cables, etc. The system has been tested in efficiency, noise level, spectrum and performance at low temperature environment. And the power system has been used in our scientific CCD detector system which is designed with ability of adapting to extreme environment.

Bibliography

1. A. G. D. Beyer, P. Cabanillas, et al. "Digitized Low-Voltage System for the Front-End of the MADS Timing RPC Wall." IEEE Transactions on Nuclear Science, 55(2):282-287, 2009.
2. G. J. Martin, K. V. Sureshbabu, C. Vaita. "High-resolution CCD camera for industrial imaging." SPIE, doi:10.1117/12.144777, 1992.
3. Piotr Dobrzanski, Grzegorz Knapowski, S.R. Bywater. "Digital techniques for noise reduction in CCD detectors." PHOTONICS LETTERS OF THE OPTICAL SOCIETY OF AMERICA, 2010.
4. W. S. Gardner, N. 1998. Alpha particles, proton and X-ray damage in fully depleted junction CCD detectors for X-ray imaging and spectroscopy. IEEE Transactions on Nuclear Science, 45(1):2449-2056.
5. Deanevic D. 2004. Low-noise silicon nitride X-ray sensor with wide operating temperature range. Electronics Letters, 40(2):175-174.
6. Barnes J., Cassin H., Dain H. T. 2012. Direct Search for Low Mass Dark Matter Particles with CCDs. Physics Letters B, 711(2):4264-4269.

Power Generation and Filtering

System Design

Test and Result

