A DAQ Prototype for the ATLAS small-strip Thin Gap Chamber Phase-I Trigger Upgrade

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Experiments and Results

The schematic block diagram of the DAQ prototype is illustrated in Fig. 1. The core of the prototype is based on a Kintex-7 FPGA, which is configured by a Serial Peripheral Interface (SPI) flash. Two VMM2s, which are interconnected using a daisy chain, are used to read out the signals from the sTGC detector. The mini-SAS connector is designed to receive the external trigger and the 40MHz synchronized clock. The Ethernet interface is used for connection between the hardware and a computer.

Fig. 2 The output noise of the DAQ prototype shielding the input charge signal.

Fig. 3 The linearity test of a channel at the gain of 4.5 mV/fC.
1. Introduction

2. Prototype Architecture

3. Data Format

4. Experimental Results

5. Conclusions

References