PLAS: A 32-channel, dead time-less analog memory ASIC for the TRACE detector

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Classical Analog Memory: SCA (Switched Capacitor Array)

- Capacitors charged consecutively, **high write frequency**
- On trigger, SCA is stopped and contents are held
- **Slow read frequency**, voltage is digitized externally
- SCA is replicated for each input channel
Problem: SCA cannot be rewritten until read out.

Low read frequency implies very long dead time.

Existing solutions: partial readout, replication.

Write: close $w$ and $f$. Read: close $r$. 

Diagram of a switched capacitor array (SCA) with nodes $C_1$, $C_2$, $C_3$, ..., $C_L$, and switches $a_1$, $b_1$, $a_2$, $b_2$, $a_3$, $b_3$, $a_4$, $b_4$.
New Analog Memory Structure: PLAS (PipeLined Asymmetric SCA)

Proposed solution: Split the memory into two sequential SCA stages

- No deadtime
- Decreased number of capacitor cells
New Analog Memory Structure: PLAS (PipeLined Asymmetric SCA)

**Stage 1:** Many short SCAs for **pre-trigger** samples

- One per input channel
- Continuous capture until trigger, then stop
New Analog Memory Structure: PLAS (PipeLined Asymmetric SCA)

Stage 2: Few **long** SCAs for **post-trigger** samples
- Shared between all inputs
- Idle until trigger, then start capturing
- Include **buffer SCA** where contents of stage 1 are copied
Come and see!

2nd poster session
Poster no. 42

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