Real Time Control Of Suspended Masses In Advanced VIRGO Laser Interferometer

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http://www.virgo-gw.eu/

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Virgo is a laser interferometer designed to detect and observe gravitational waves. It is operated in Cascina, near Pisa on the site managed by the consortium European Gravitational Observatory (EGO), by an international collaboration of scientists from France, Italy, the Netherlands, Poland, and Hungary.
VIRGO Interferometer
Gravitational Waves

GW Signal is incredibly small: actual relative displacement is in the order of $6-8 \times 10^{-18}$ m (peak-to-peak)

LIGO Hanford & Livingstone data: first direct detection
Adv VIRGO Design Sensitivity

![Graph showing the design sensitivity of VIRGO with various noise contributions labeled.](image)
Seismic Isolation

$10^{15}$ @ 10 Hz of passive attenuation!!
Mirrors
Each of 10 seismic isolation systems is equipped with inertial sensors (accelerometers), displacement sensors (LVDT and optical levers), stepping motors and magnet-coil actuators.
New Control System: Design Drivers

- Move out of VME standard (limiting board-to-board communication bandwidth)
- Eliminate physical gap between analog-front end and data converters (in average we had more than 40 meters STP cabling, multiplied by about 100 signals for each of the 10 suspensions)
- Get out of rigid single sampling frequency operation (usually 10 kHz) and move on a more performing and flexible multi-rate system
- Further increase of locally available computation power to increase data quality analysis capabilities and properly assist control design and implementation mainly for the last stage of suspension and new payloads
UDSPT Board

Result of design effort is a high performance signal conditioning, signal conversion and processing platform that enables users to implement state of the art hard real time control system. Board can be operated in standalone mode or in cooperation with other boards.

Form factor is a variation of a Double Compact Module PICMG® AMC.0 R2.0 AdvancedMC module (variation consists in a wider board than what specified for a Double Module)

Key features of the UDSPT board include:

- Texas Instruments' multi-core DSP – TMS320C6678
- 512 Mbytes of DDR3-1333 Memory
- Two Gigabit Ethernet ports supporting 10/100/1000 Mbps data-rate
- 170 pin B+ style AMC Interface containing SRIO and Gigabit Ethernet
- IRIG-B input
- Module Management Controller (MMC) for Intelligent Platform Management Interface (IPMI)
- Powered by DC power-brick adaptor (12V/3.0A) or AMC Carrier backplane
- Two on board FPGA: one Xilinx Spartan3 dedicated to processing unit and one Altera Cyclone IV interfacing data converters
- 6 x 24b 3.84 MHz ADC converters
- 3 x 24b 320 kHz DAC stereo converters (6 channels individually addressable)
- Converters sampling frequency DSP IRQs synchronous with IRIG-B signal
- Fully differential input channels and balanced output channels
UDSPT Board

Board complexity (250 different parts, a total of 2500 components) was compensated by a modular design. Processing, data converters and front-end occupy pre-defined areas. Strong effort in interfaces design.
Performances

Digital I/O

- Gb Ethernet Board- Rest of The World communication
- PCIe (2 x 2.5 Gbps) On-Board communication
- SRIO (4 x 5 Gbps) Board-to-board communication

DSP Software

- Operation up to 320 kHz sampling rate (3.125 usec interrupt request repetition cycle)
- Matrix(n,m)*Vector(m,1) double precision multiplication requires 0.5*nm+n+m nanoseconds:
  - State space with 3 inputs, 3 outputs and 12 states requires less than 200 nsec
DAC Performances

74.75 Hz

THD = -118 dB

DAC Conversion Rate: 320 kSPS
Signal set at 0.9 x Full Scale (FS = 20Vpp)

Virgo/Virgo+ DAC Noise
DAC output spectrum when converting a white spectrum signal low pass filtered (4 poles @ 1Hz + 4 zeroes @ 10 Hz) and stopband (30-50 Hz, Bessel 12th order, 0.1dB ripple, -60 dB stopband). Signal amplitude was set to 0.6Vpp
ADC

ADC Noise

ADC Conversion Rate: 3.84 MSPS
12 x decimation → 320 kSPS
0 Vdc output (FS = 10Vpp)

PSD/V/√Hz

Frequency (Hz)

74.75 Hz

THD = -96.8 dB

dB/√V

0 200 400 600 800 1000 1200 1400 1600

Frequency (Hz)
DAC-DSP-ADS Transfer Function

Group delay ~ 42 usec (~650 usec in Virgo+)
Performances tests on suspensions went beyond our expectation. Placing converters at front-end electronics level, together with introduction of digital demodulation, drastically improved noise immunity. Following picture shows improvement in vertical position sensors readout.
In a single 6U x 19” crate we can concentrate 72 ADC + 72 DAC channels supported by 720 GFLOPs, 12 x 1 Gb Ethernet ports + 12 x 1 Gb Optical Link for digital IO and a total power consumption less than 500 Watts
Recently we completed the installation of 20 Local Contro Units for a total of 150 boards, 900 ADC channels and 900 DAC channels
Digital Signals Path

Gb ETH
IRIG-B
Gb Optical Link

UDSPT #1
UDSPT #2
UDSPT #3
UDSPT #4
UDSPT #6
UDSPT #7
UDSPT #11
UDSPT #12

4 x 5Gbps

IRIG-B

ETH
MCH
SRIO
CLK

Front Panel

A. Gennai (INFN)
For initial AdV, software shall support about 150 boards. At system startup each board loads boot code via tfpt from a dedicated boot server. This code is actually a sort of basic OS. In a second phase software supervisor (based on software toolkit Tango Controls) downloads in each processor the hard real-time code.
A nice tool for system debugging is a real-time scope that can access any single variable declared into the source code. Work is in progress to provide real-time fft and few more functionalities.
Each DSP core, excluding C#0, runs a single task activated at a fixed frequency lower or equal to 320 kHz.

Communication is memory mapped using a 2 stages FIFO (ping-pong table).

5 out of the 8 cores available are user programmable.
From a source code written in a simple object-oriented language we generate asm code for the cross-compiler that produces DSP binary code.

A. Gennai (INFN)
Conclusions

A new system to control suspensions and mirrors was developed and installation is now completed.

Extensive use of supervising software, mysql databases and third parties tools will simplify operation and maintenance.

Simple user interfaces allow writing real-time DSP code without having specific training.