BI-TB on BST Systems

- Introduction (L. Jensen)
- Hardware for SPS/LHC masters and receivers (old and new) (JJ. Savioz)
- Software for masters and receivers (L. Jensen)
- BST systems used for LHC experiments (S. Baron/L. Jensen)
- RF signal distribution for SPS and LHC (W. Hofle)
- Consolidation ideas for the BST systems (J. Serrano)
- Beam synchronous signals for PS (H. Damerau)
- Conclusions and outlook (All)

Introduction

- Transmission of ‘hardware’ signals (Frev, 40MHz, pre-pulses) + message (LHC: 64 bytes / turn)
- Hardware consists of:
  - 3 central masters:
    - SPS
    - LHC Beam 1
    - LHC Beam 2
  - BOBR receivers (+new VFC-based modules)
- Main use (BI):
  - Acquisition clocks and triggering + time-stamping of BI systems (“DAB64x”) through the BOBR receiver
    - BPM, BLM, BRAN, BSRA, BSRT, BCTF ..
    - LHC: presently have >130 BOBR devices
- Objectives for the meeting today:
  - Inform of what’s available today
  - Agree on responsibilities (present and future)
  - Discuss consolidation plans (SPS/LHC)
  - Details concerning PS BST (Heiko)

Master Message

- LHC Message:
  - http://bdidev1.cern.ch/bdisoft/operational/abbdisw_wiki/LHC/BST-config
- EDMS document (2008):
  - https://edms.cern.ch/document/638899/2.0

BST message layout

Position	Content	BST Task
0 → 7	GPS absolute time	(automatically sent by BST Master)
8 → 12	Acquistion triggers	(see separate table below)
13 → 15	Acquistion spare triggers	Unused for now, to be used in the future.
16	AB-BI diagnostics byte	diagnostics
17	BST Master status register	values
18 → 21	Turn count	(automatically sent by BST Master)
22 → 25	LHC fill number	values
26 → 27	Beam mode	values
28	Particle type ring #1	values
29	Particle type ring #2	values
30 → 31	Beam momentum	values
32 → 35	Intensity ring #1	values
36 → 39	Intensity ring #2	values
40 → 43	Intensity from BCTF, ring #1	bctf_udp
44 → 47	Intensity from BCTF, ring #2	bctf_udp
48 → 49	Bunch count from BCTF, ring #1	bctf_udp
50 → 51	Bunch count from BCTF, ring #2	bctf_udp
52 → 55	LHC Telegram values	values
56 → 58	External triggers	automatic by CTG

BI acquisition triggers (defined and used for BPM/BLM)

Acquisition triggers

Byte	Bit	Content	BST Task
8	0	Global PM start	pm_start
	1	BPM Post Mortem freeze	pm_freeze
	2	BLM Post Mortem freeze	blm_pm_freeze
	3	BCTF Post Mortem freeze	pm_freeze
	4		
	5		
	6		
	7		
9	0	BPM capture start	bpm_capture
	1	BPM orbit trigger	bpm_orbit_trigger
	2	BPM Bunch Orbit	bpm_bch_orbit_trigger
	3	BPM XPOC freeze	xpoc_freeze
	4		
	5		
	6	BPM injection prepulse	prepulse
	7		
10	0	BLM capture start	blm_capture
	1	BLM XPOC freeze	blm_xpoc_freeze

- Allow triggering all distributed systems within n*100ps for timing events on 1msec frame

Master software

- BST Master project started as collaboration in 2004
  - P. Karlsson (BI), D. Dominguez (CO), J. Lewis (CO)
- VME hardware clone of “MTG” module -> “BST-CTG” (FPGA micro-controller)
  - Tasks with software written in assembler-language, compiled before download
    - Global (GR) and per task registers (R)
- FESA (2.10) class and BST tasks developed and maintained by BI/SW
  - PPC4 OS - port to L865 will likely await 2014
- Regular orbit-trigger every “GR11” msec

```
700:
        WTRIGX 0x0010
        WTURNR 1
        LOAD R15 0
        JUMP G1

G1:
        LOR GR2 0x2     % byte 9, bit 1
        XMIT0 GR2 9
        WTURNR 1
        LAND GR2 0xFFFD % LAND without that bit
        XMIT0 GR2 9
        WTURNR 1
        LAND GR2 0xFFFD % LAND without that bit
        XMIT0 GR2 9
        ADDV R15 1
        MOVR R0 GR11    % Delay between triggers is set here, copy value in GR11 to R0
        JUMP G2

G2:
        WTRIGX 0x0002 % Wait for millisecond trigger.
        WTURNR 1
        SUBV R0 1
        SKPNZ R0
        JUMP G1
        JUMP G2
```

Initialisation – wait for 1 PPS event

Orbit on bit #2 of byte 9

Count-down

BOBR software

- BDI_BOBR hardware-type in CCDB
- Device driver for PPC4 and L865 based on ‘dgII’
- Handling of two hardware-bytes sent on the **BI-only** Wiener-crates (P0 lines rows D/E)

Pos	Row a	Row b	Row c	Row d	Row e
1	HW Low Byte 1 bit 0	HW High Byte 1 bit 0		HW Low Byte 2 bit 0	HW High Byte 2 bit 0
2	HW Low Byte 1 bit 1	HW High Byte 1 bit 1		HW Low Byte 2 bit 1	HW High Byte 2 bit 1
3	HW Low Byte 1 bit 2	HW High Byte 1 bit 2		HW Low Byte 2 bit 2	HW High Byte 2 bit 2
4	HW Low Byte 1 bit 3	HW High Byte 1 bit 3		HW Low Byte 2 bit 3	HW High Byte 2 bit 3
5	HW Low Byte 1 bit 4	HW High Byte 1 bit 4		HW Low Byte 2 bit 4	HW High Byte 2 bit 4
6	HW Low Byte 1 bit 5	HW High Byte 1 bit 5		HW Low Byte 2 bit 5	HW High Byte 2 bit 5
7	HW Low Byte 1 bit 6	HW High Byte 1 bit 6		HW Low Byte 2 bit 6	HW High Byte 2 bit 6
8	HW Low Byte 1 bit 7	HW High Byte 1 bit 7		HW Low Byte 2 bit 7	HW High Byte 2 bit 7
9					
10					
11					
12	Bunch Select 1 Bit 0	LVDS Turn clock Delay 1 +		Bunch Select 2 Bit 0	LVDS Turn clock Delay 2 +
13	Bunch Select 1 Bit 1	LVDS Turn clock Delay 1 -		Bunch Select 2 Bit 1	LVDS Turn clock Delay 2 -
14	Bunch Select 1 Bit 2	TTL Turn clock Delay 1 +		Bunch Select 2 Bit 2	TTL Turn clock Delay 2 +
15	Bunch Select 1 Bit 3	TTL Turn clock Delay 1 -		Bunch Select 2 Bit 3	TTL Turn clock Delay 2 -
16	Bunch Select 1 Bit 4	LVDS 40 MHz Clock 1 +		Bunch Select 2 Bit 4	LVDS 40 MHz Clock 2 +
17	Bunch Select 1 Bit 5	LVDS 40 MHz Clock 1 -		Bunch Select 2 Bit 5	LVDS 40 MHz Clock 2 -
18	Bunch Select 1 Bit 6	TTL 40 MHz Clock 1 +		Bunch Select 2 Bit 6	TTL 40 MHz Clock 2 +
19	Bunch Select 1 Bit 7	TTL 40 MHz Clock 1 -		Bunch Select 2 Bit 7	TTL 40 MHz Clock 2 -

Table 7: Pin allocations on P0 (Front view)

- VME interrupts based on setup of message byte and bit masks
- FESA 2.10 class developed and maintained by BI/SW (ported to L865)