Beam Synchronous Timing

BE-CO-HT status and plans

Javier Serrano

Geneva, 17.10.2013

Current BST Master

- Standard module supported by BE-CO-HT.
- We cover: hardware, gateware, driver, library and test program.
- Migration to Linux 64 bit well underway. Deployment expected before end of LS1.
- No plans to modify our level of support.

Ugly bits of the current system

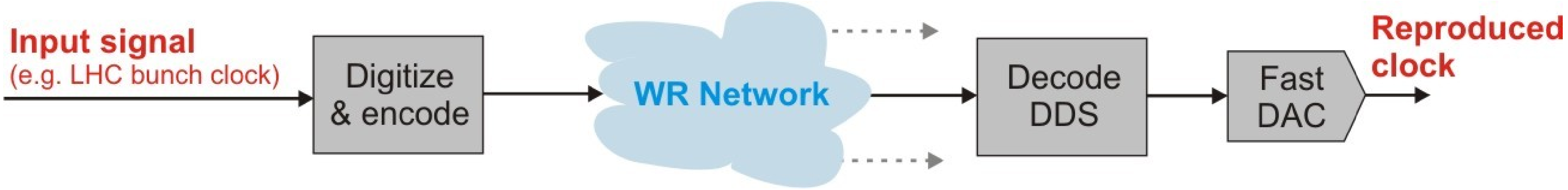
- Awkward connection between BST and GMT.
- Two different networks needed for LHC BST: ring 1 and ring 2.
- No phase compensation.

Potential issues looking at LS2

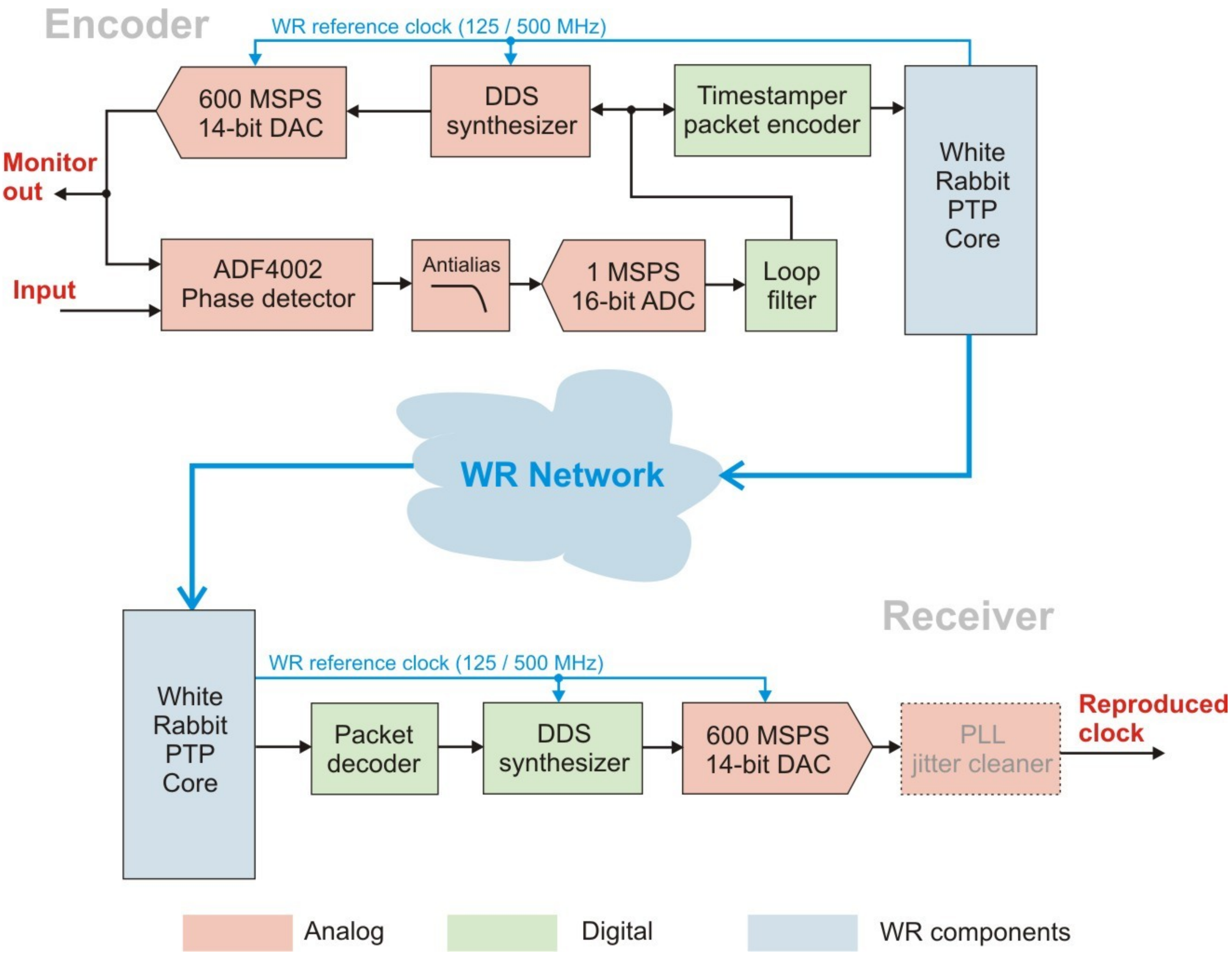
- Some obsolete equipment with unclear (to us) evolution plans: big laser box, encoding boards, TTCrx chip...
- Question open on whether the TTC physical layer can cope with the variations of RF frequency in SPS.

One more trick in our bag of tricks

- Input any reasonably stable (FM bandwidth: ~ 20 kHz) clock signal,
- Digitize it and broadcast over a synchronous network,
- Reproduce the original signal at any number of receivers,
- Share the network with other applications.



Distributed DDS



Distributed DDS

- Use a fast DAC driven by a DDS as a tunable oscillator,
- Put it inside a PLL, referenced with the clock that we want to transmit,
- Postprocess, encode and broadcast the oscillator tuning values over the WR network,
- Drive any number of identical DDS cores with the received data stream,
- Since WR ensures phase-compensated 125 MHz reference clock at every node in the network, slave DACs will produce a **copy of the master's clock**.

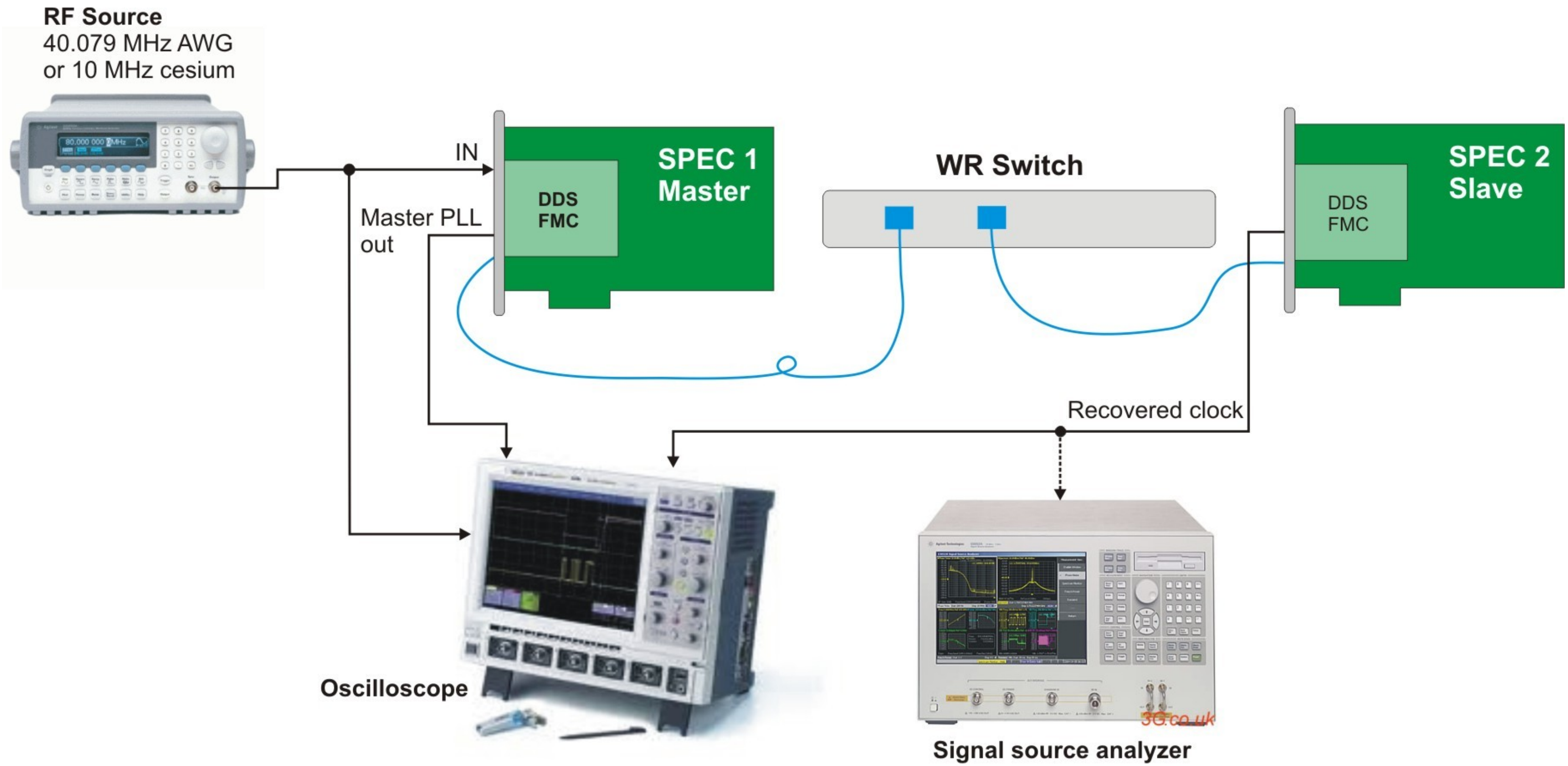
Test system

- 2 SPEC cards with 2 DDS FMC mezzanines.

  http://www.ohwr.org/projects/fmc-dac-600m-12b-1cha-dds/wiki
  http://www.ohwr.org/projects/spec

- Point-to-point link.
- Test frequency: 10 MHz cesium standard, loop bandwidth: 10 kHz, broadcast rate: 110 kHz.
- Encoder PLL performance: 6 ps rms jitter (10 Hz – 5 MHz), -110 dBc/Hz noise floor (@ 100 Hz)
- Recovered clock: 8.5 ps rms jitter.
- Significant part of the jitter likely comes from buggy PCB design (1st prototype)

Test system



RF Source
40.079 MHz AWG
or 10 MHz cesium

IN

Master PLL
out

DDS
FMC

SPEC 1
Master

WR Switch

DDS
FMC

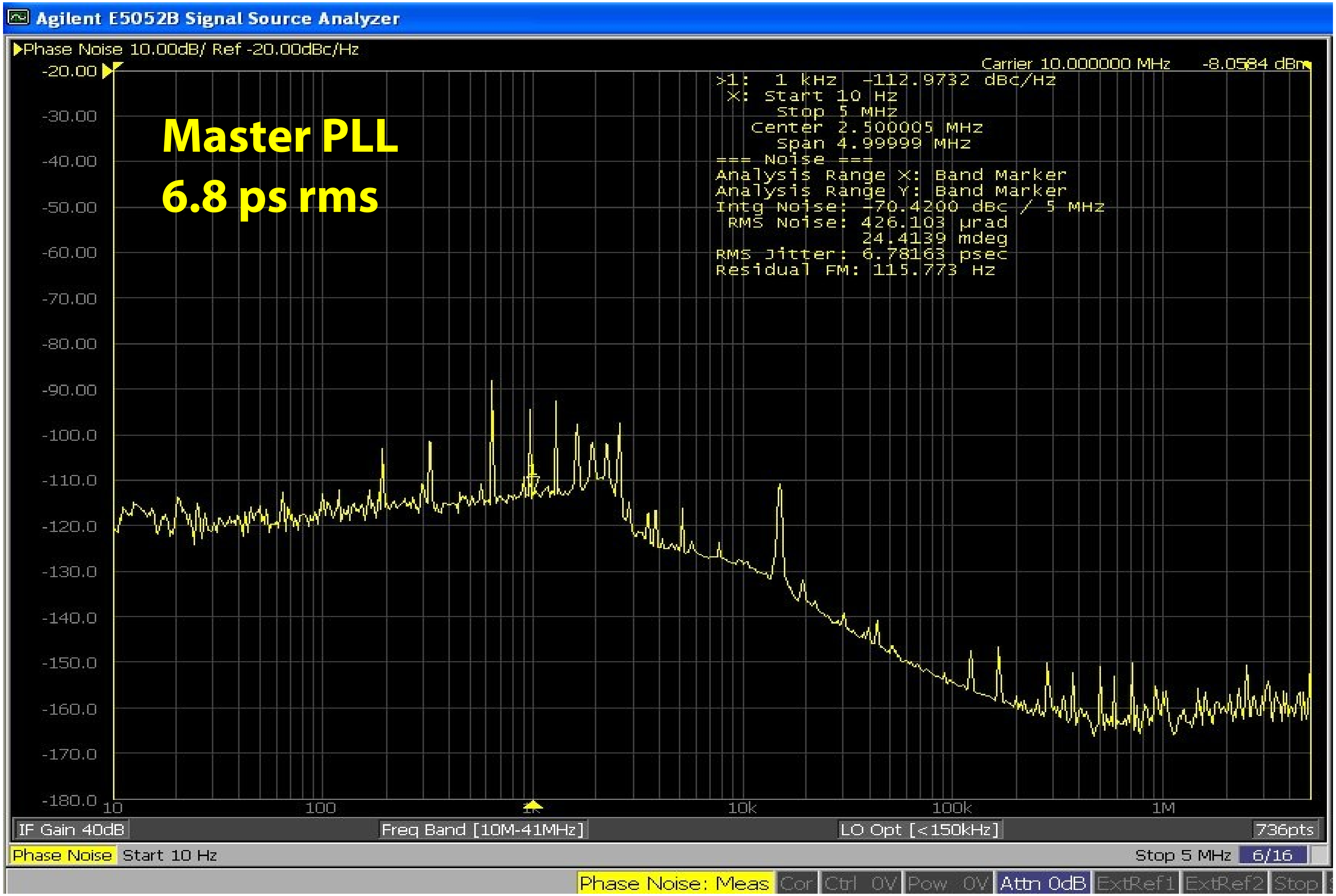
SPEC 2
Slave

Recovered clock

Oscilloscope

Signal source analyzer

Performance



Master PLL

6.8 ps rms

Agilent E5052B Signal Source Analyzer

Phase Noise 10.00dB/ Ref -20.00dBc/Hz

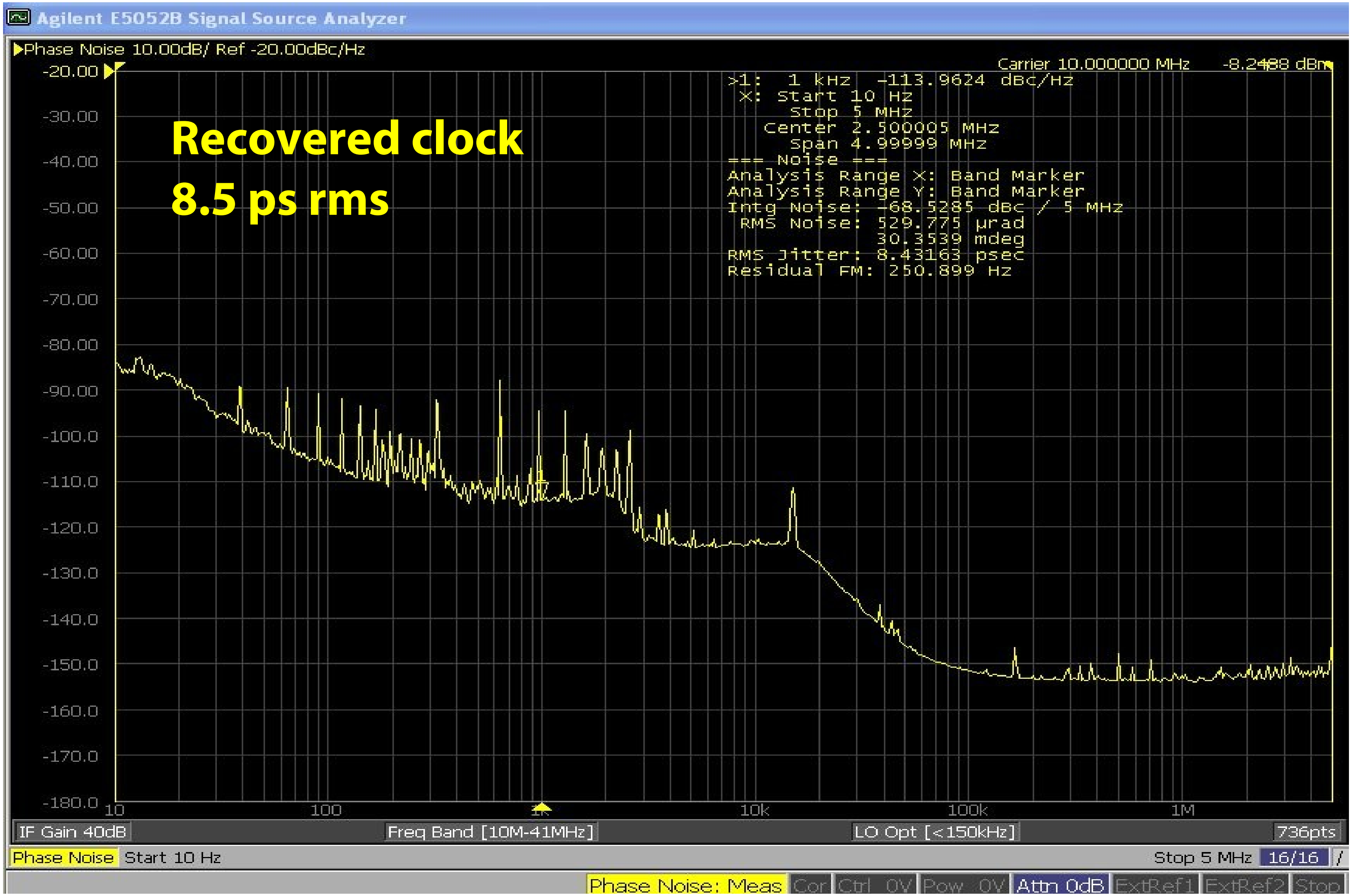
Carrier 10.000000 MHz -8.0584 dBm

```
>1:  1 kHz  -112.9732 dBc/Hz
 X: Start 10 Hz
      Stop 5 MHz
    Center 2.500005 MHz
      Span 4.99999 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -70.4200 dBc / 5 MHz
 RMS Noise: 426.103 µrad
            24.4139 mdeg
RMS Jitter: 6.78163 psec
Residual FM: 115.773 Hz
```

IF Gain 40dB | Freq Band [10M-41MHz] | LO Opt [<150kHz] | 736pts

Phase Noise | Start 10 Hz | Stop 5 MHz | 6/16

Performance



Recovered clock

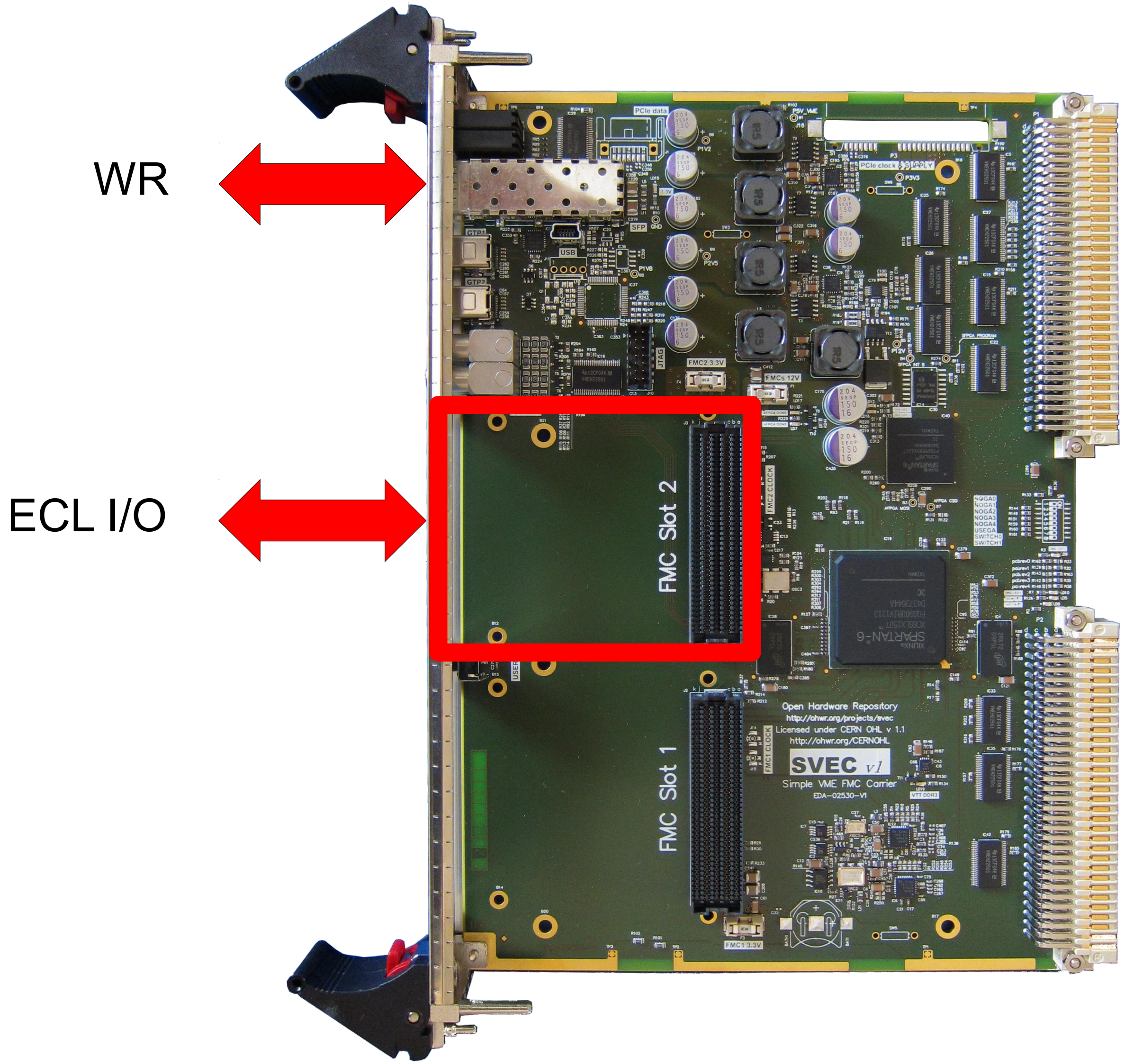
8.5 ps rms

```
Carrier 10.000000 MHz    -8.2488 dBm
>1:  1 kHz  -113.9624 dBc/Hz
 X: Start 10 Hz
      Stop 5 MHz
    Center 2.500005 MHz
      Span 4.99999 MHz
=== Noise ===
Analysis Range X: Band Marker
Analysis Range Y: Band Marker
Intg Noise: -68.5285 dBc / 5 MHz
 RMS Noise: 529.775 µrad
            30.3539 mdeg
RMS Jitter: 8.43163 psec
Residual FM: 250.899 Hz
```

To do...

- Implement point-to-multipoint transmission and simultaneous encoding of multiple clocks,
- Reduce data bandwidth requirements – better encoding (prediction-correction or jitter-bound lossy compression),
- Optimize jitter: fine-tune PLL filters, deal with PCB issues, check performance with an additional cleaner PLL.

A possible migration plan



Summary

- We plan to maintain the level of support on the BST Master side, along with an imminent migration to Linux.
- Not clear yet what we should do for LS2. Some ideas on how to transmit RF using White Rabbit:
  - With phase compensation.
  - In a more frequency-agile way.
  - With more than one RF possible per link.
- Your input and collaboration is very welcome.