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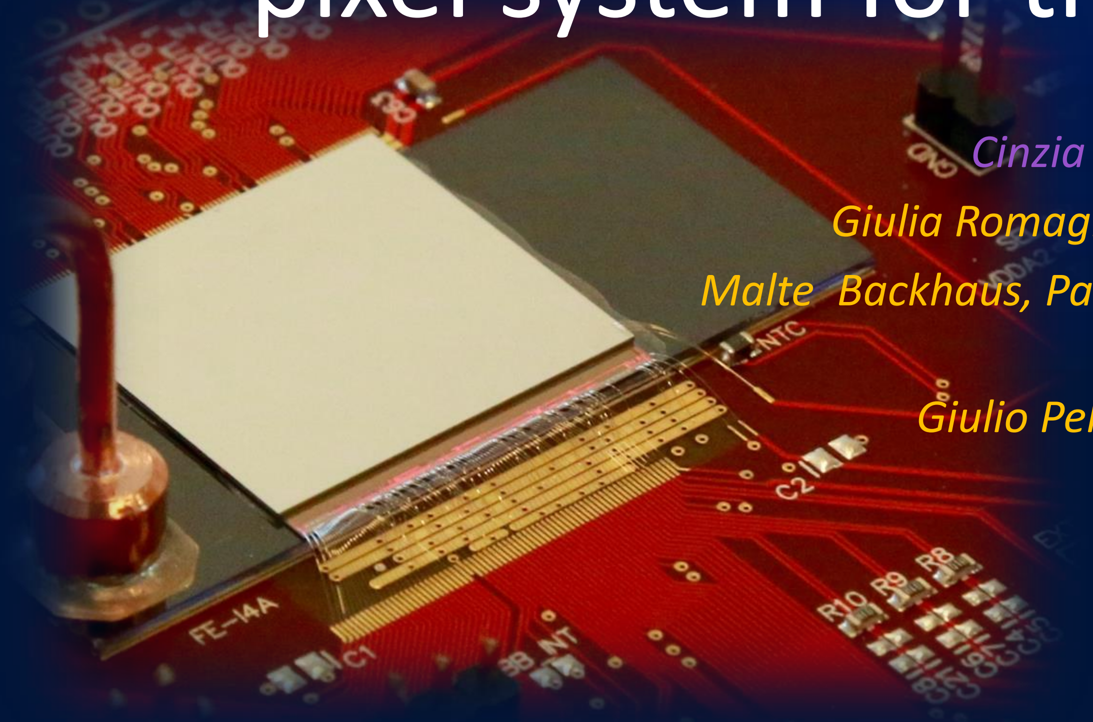
Cinzia Da Via, Manchester. Vienna Conference on Instrumentation 18-02-2016

A low mass vertically integrated pixel system for the HL-LHC



Cinzia Da Vià, (Manchester)

Giulia Romagnoli, (Manchester and CERN)

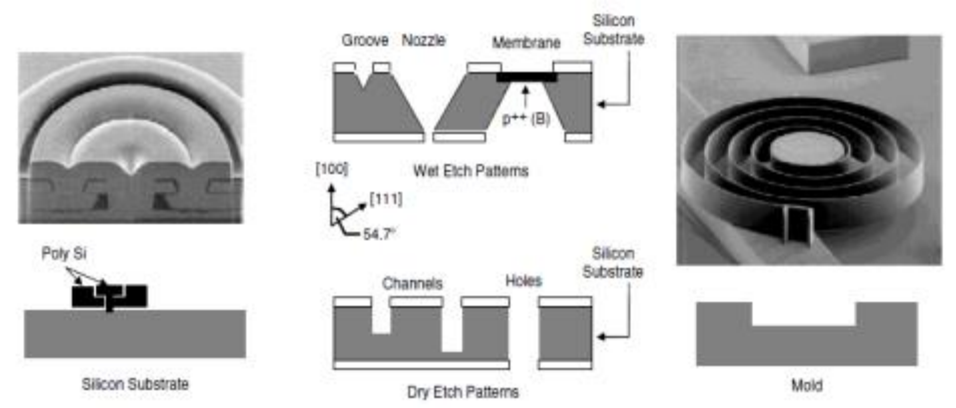
Malte Backhaus, Paolo Petagna, Desiree Hellenschmidt (CERN),

Giulio Pellegrini (CNM Barcelona)

Micro-Fabrication

In Micro-fabrication, used mainly for Micro-Electro Mechanical Systems (MEMS), the process is performed 3 dimensionally within the silicon volume.
Different processing types include:

- ❖ Surface: Structures are formed by deposition and etching of sacrificial and structural thin films
- ❖ Bulk, Volume: 3D structures formed by dry or wet etching of silicon substrates
- ❖ LIGA: 3D structures formed by mold fabrication followed by injection molding or electroplating
- ❖ 3D printing....



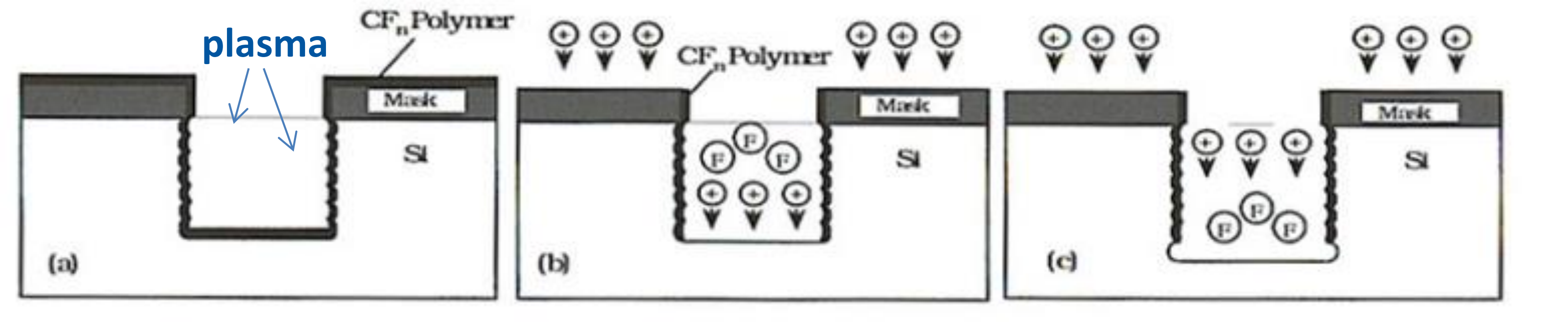
Surface Bulk LIGA

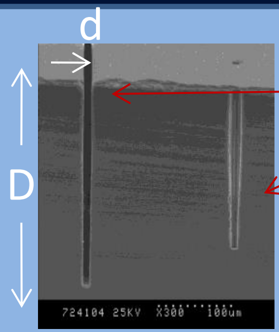
Applications:

- ➢ Everyday life (cars, portable devices..)
- ➢ Medical/Biology
- ➢ Space
- ➢ High Energy Physics
- ➢ …

Deep Reactive Ion Etching

Bosch Process

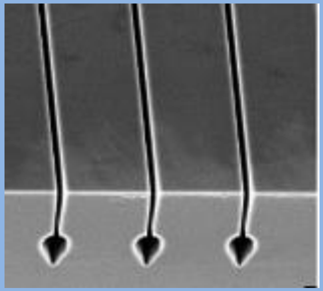




Deep pores and trenches

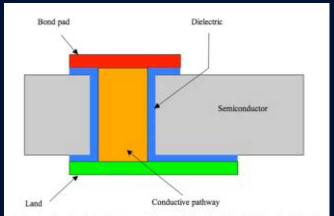
micro-channels

Aspect ratio d/D=25:1



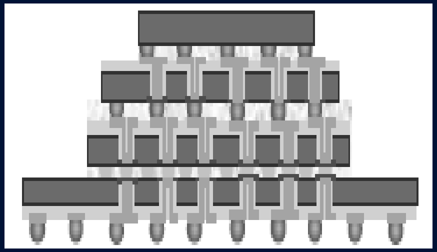
Bosi et al.
Fabricated at FBK, Trento Italy

Interconnectivity
Using TsV



1. Drawing showing the key features of a through silicon via (TSV). A TSV can be defined as "A structure that provides an electrical pathway through the thickness of a semiconductor (silicon) die between a bond pad on the front face and a land on the rear face. The pathway, bond pads and lands are all electrically isolated from the semiconductor." Drawing not to scale. Source: Tessera.

Vertically integrated electronics



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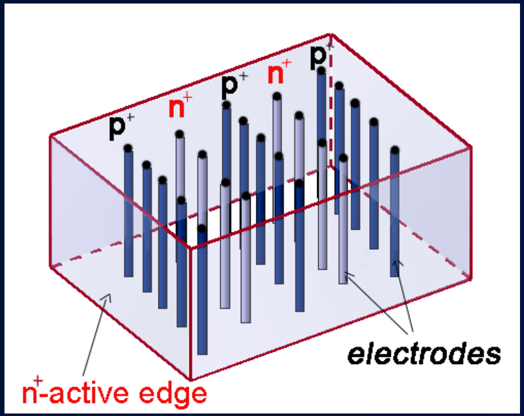
3D radiation sensors



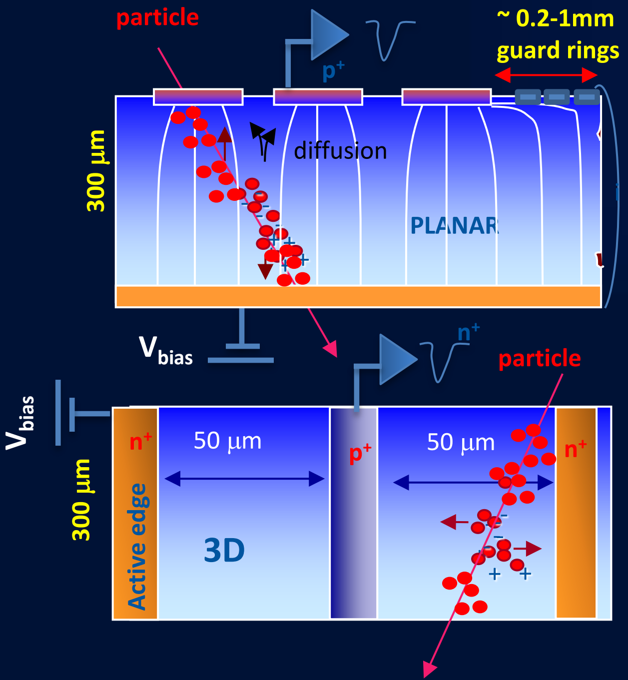
3D silicon detectors were proposed in 1995 by S. Parker, and active edges in 1997 by C. Kenney.

Combine traditional electronics processing and Micro-Fabrication technology.

Electrodes are processed inside the detector bulk instead of being implanted on the Wafer's surface.

The edge is an electrode! Dead volume at the Edge < 5 microns!

The electric field parallel to the wafer's surface and smaller inter-electrode spacing give low bias voltage, low power, reduced charge sharing and high speed – for the same wafer thickness



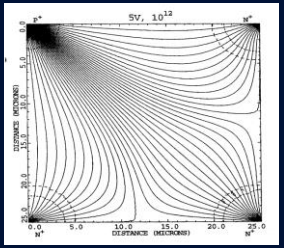
V=70V

Before irradiation

V=7V !!!

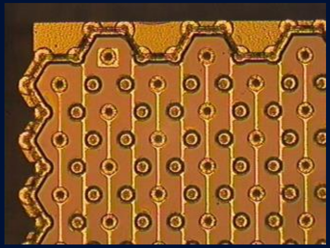
Before irradiation

Drift lines parallel to the surface



MEDICI simulation of a 3D structure

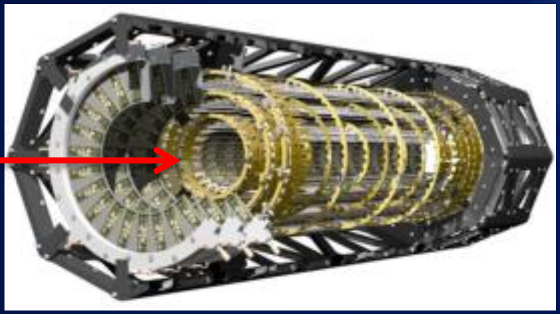
Hexagonal layout with active edges

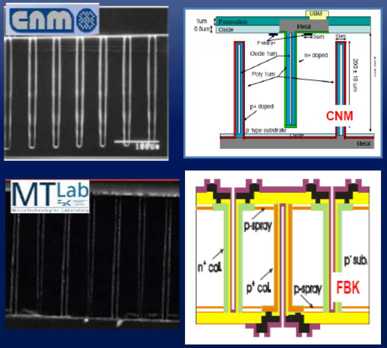


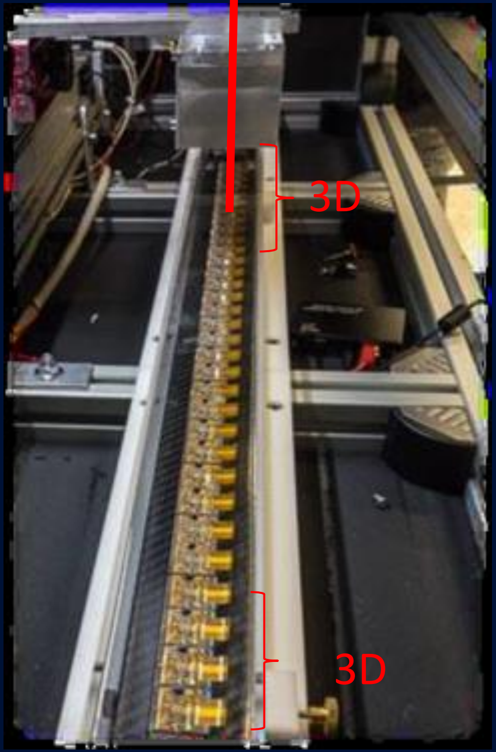
3D sensors are now in the core of ATLAS

3DATLAS R&D Collaboration

NIMA 694 (2012) 321–330
2012 JINST 7 P11010.

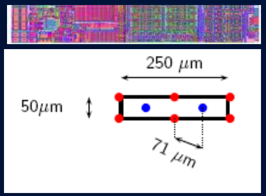




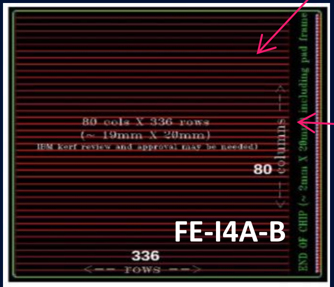


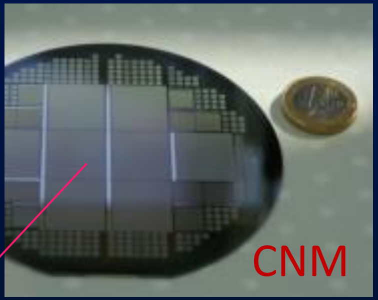
3D sensors are installed in the first LHC detector upgrade in the ATLAS –Insertable B-Layer (IBL) and took data in 2015

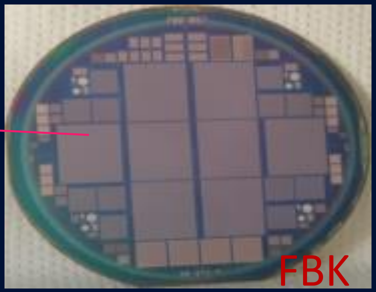
>300 sensors fabricated to cover 25% IBL



FE-I4 = 2x2cm^2
336 x 80 250x50um^2,
26880 pixels



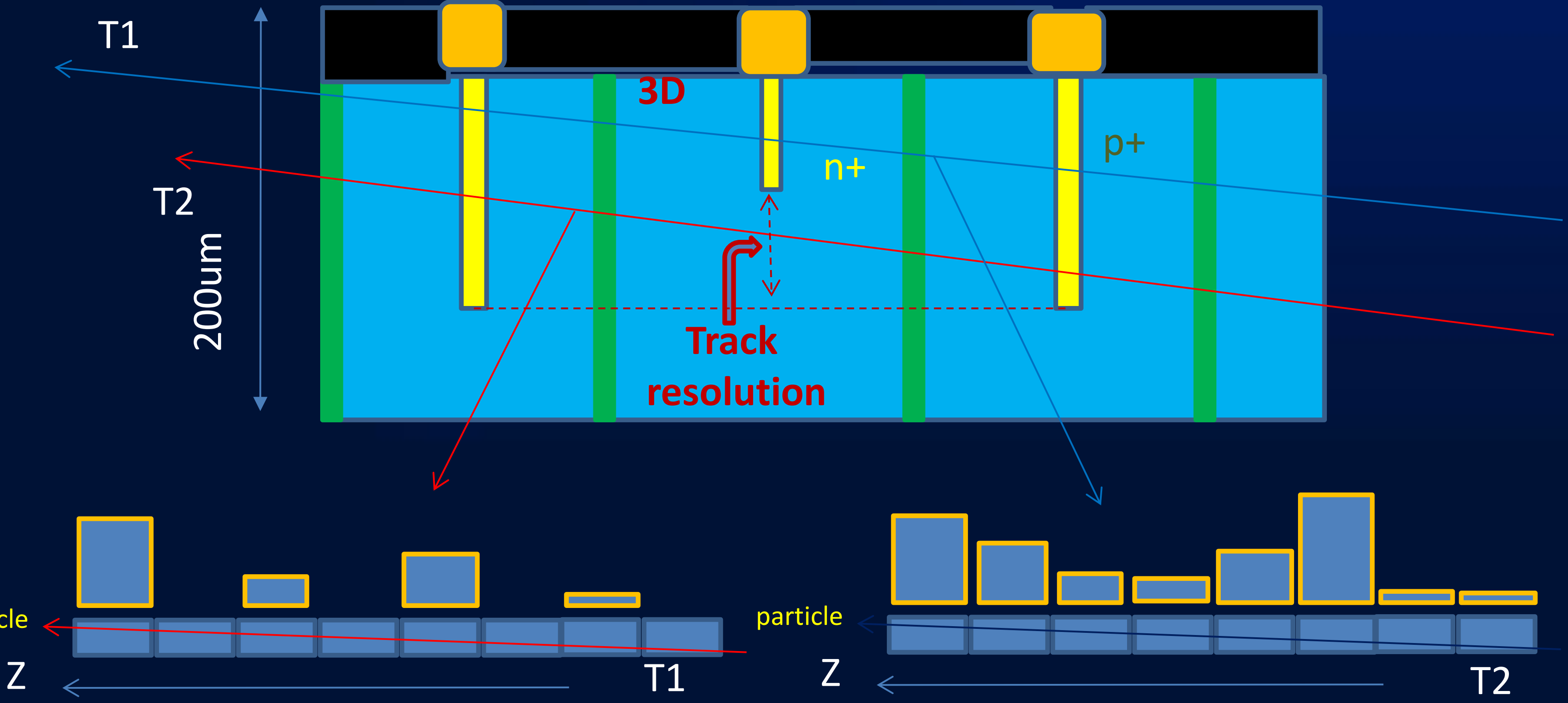




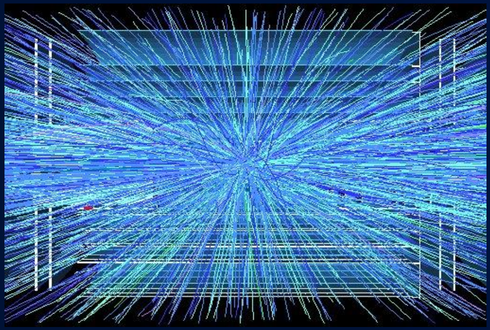
3D Silicon Sensors with variable column depth

2015 JINST 10 C04020

Column differ in depth Inside the same sensor

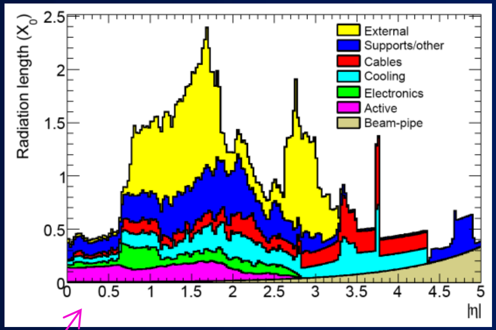


The HL-LHC Vertex detectors challenges:



Precision reconstruction

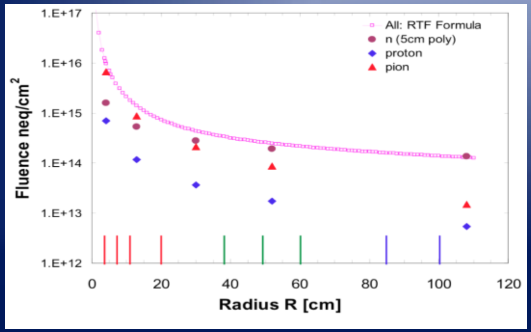
Needs the signal over threshold



Material budget

is not the sensor

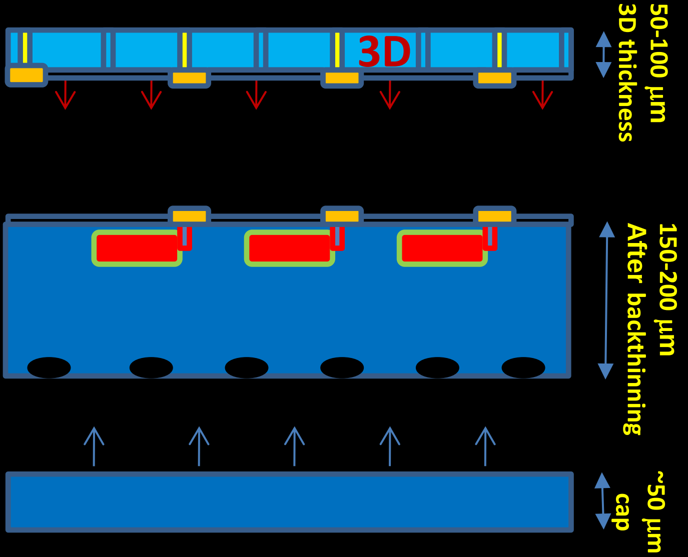
IBL 1.5%X_0



EoL fluence 2×10^{16}ncm^{-2}

Radiation tolerance and power budget

A Possible Solution is an aggressive vertically integrated system composed by:



- ❖ 3D silicon sensor modules with active edges
- ❖ Interconnected with micro-bump bonds and through chip bias supply
- ❖ Embedded micro-cooling

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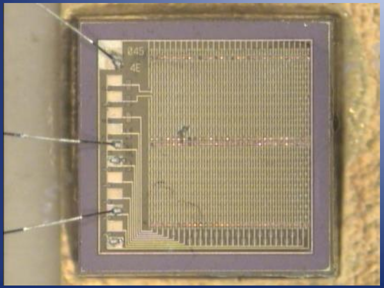
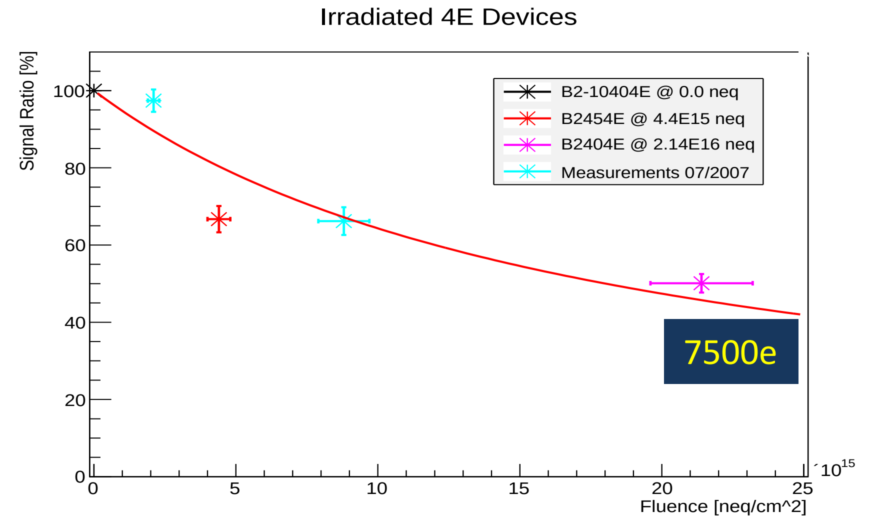
3D sensors Radiation Hardness

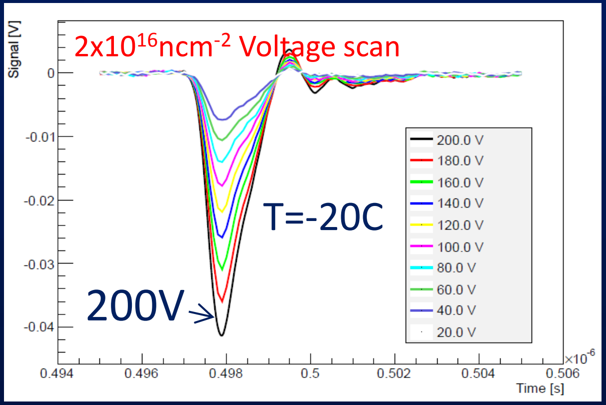
SINTEF
1cm^2 diode
IES 56 um

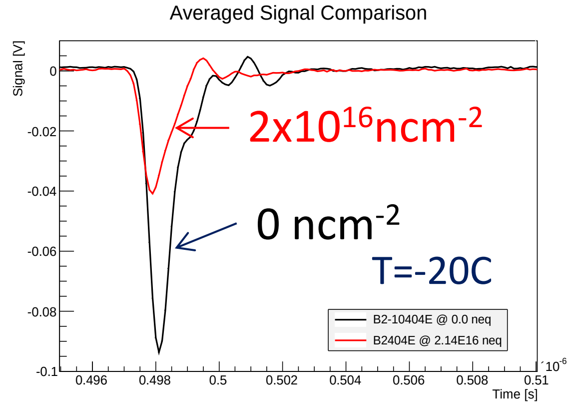




3D with 56 um inter electrode spacing and 200 micron thickness - 50% of the original charge available after 2x10^16ncm^-2

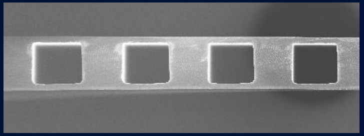
(I. Haughton PhD thesis)



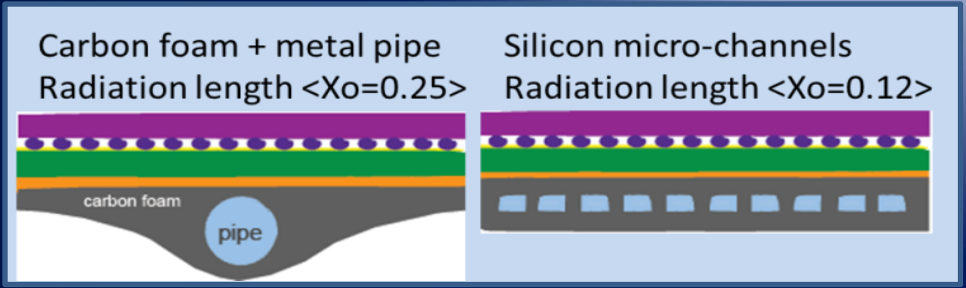


Comparison 0 and 2x10^{16}ncm^{-2}

Advantages and Open Questions of Micro-channel cooling



Si-Si



Carbon foam + metal pipe
Radiation length <Xo=0.25>

Silicon micro-channels
Radiation length <Xo=0.12>

Even lower mass :

- ❖ Reduction of ‘bulky’ thermal interface required between cooling channel and substrate

Cooling channel is integrated in the substrate:

- ❖ Can customize the routing of channels to run exactly under the heat sources.

Many parallel channels:

- ❖ large liquid-to-substrate heat exchange surface.

No heat flows in the substrate plane:

- ❖ Small thermal gradients across the module.

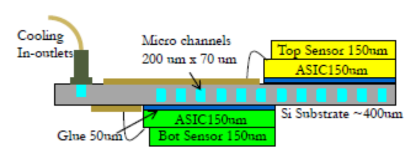
All material is silicon or silicon compatible:

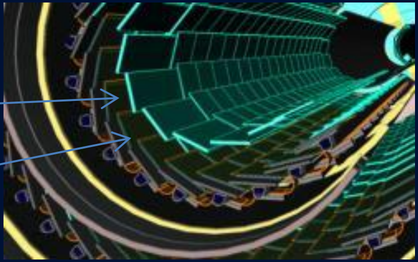
- ❖ No mechanical stress due to CTE mismatch.

- ❖ Big Open Question 1: how to homogeneously cool a 1.5m stave

- ❖ Big Open Question 2: reliable low-mass connectors for an innermost barrel layer

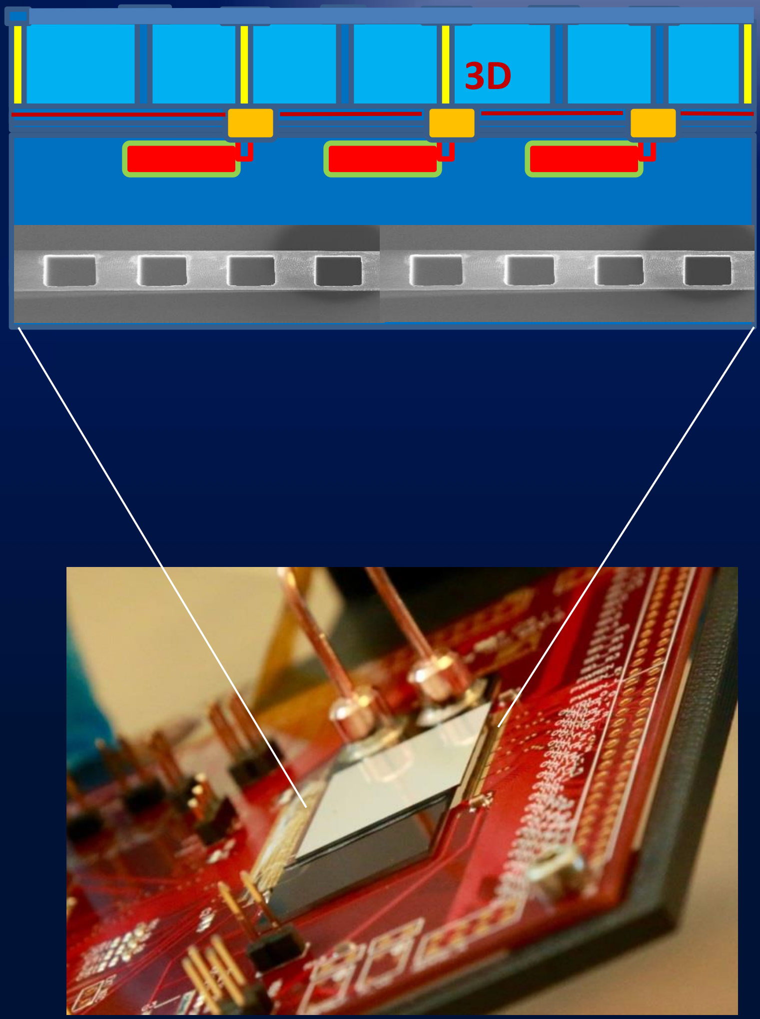
Not new in HEP:
see LHCb talk

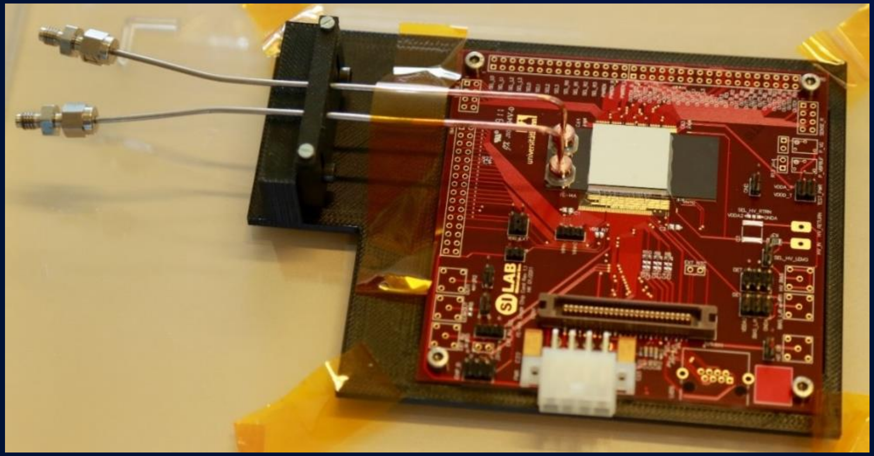




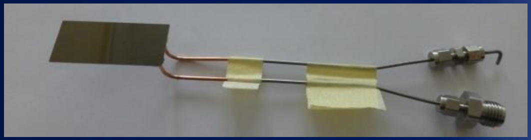
3D Vertically Integrated Module

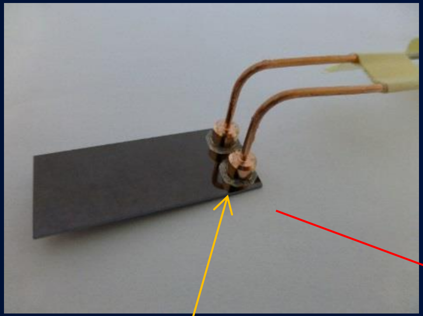
- 3D silicon : CNM double side 285 um thick IBL qualification batch
- FE-I4A: thinned to 100um at IZM
- Si-Si micro-channels designed by CERN PH-DT, produced by PH-DT in EPFL CMi cleanroom, direct bonding CSEM
- Glue: 2-components Masterbond EP37-3FLFAO

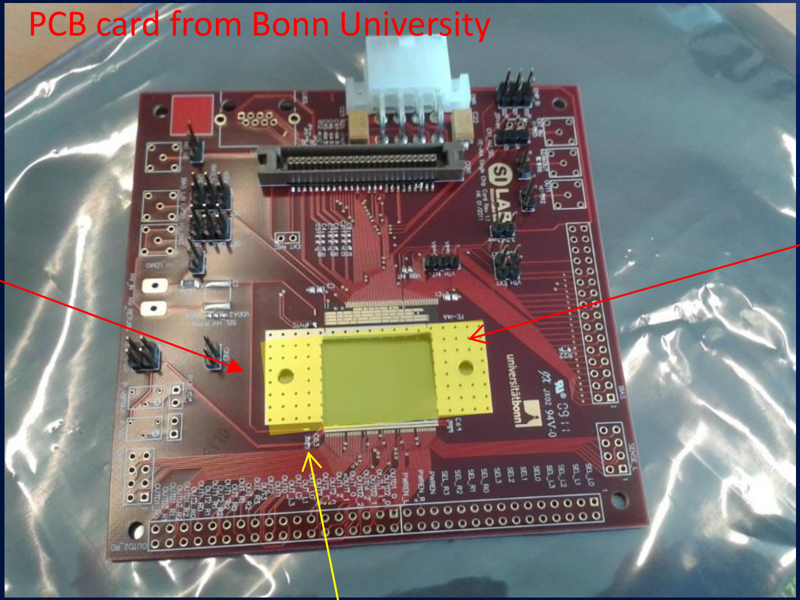


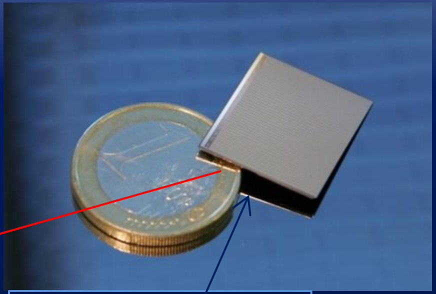


Module assembly





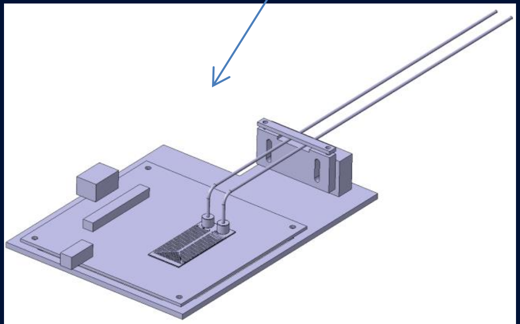

PCB card from Bonn University



3D sensor + FE-I4

Gluing area of silicon micro-channels on PCB

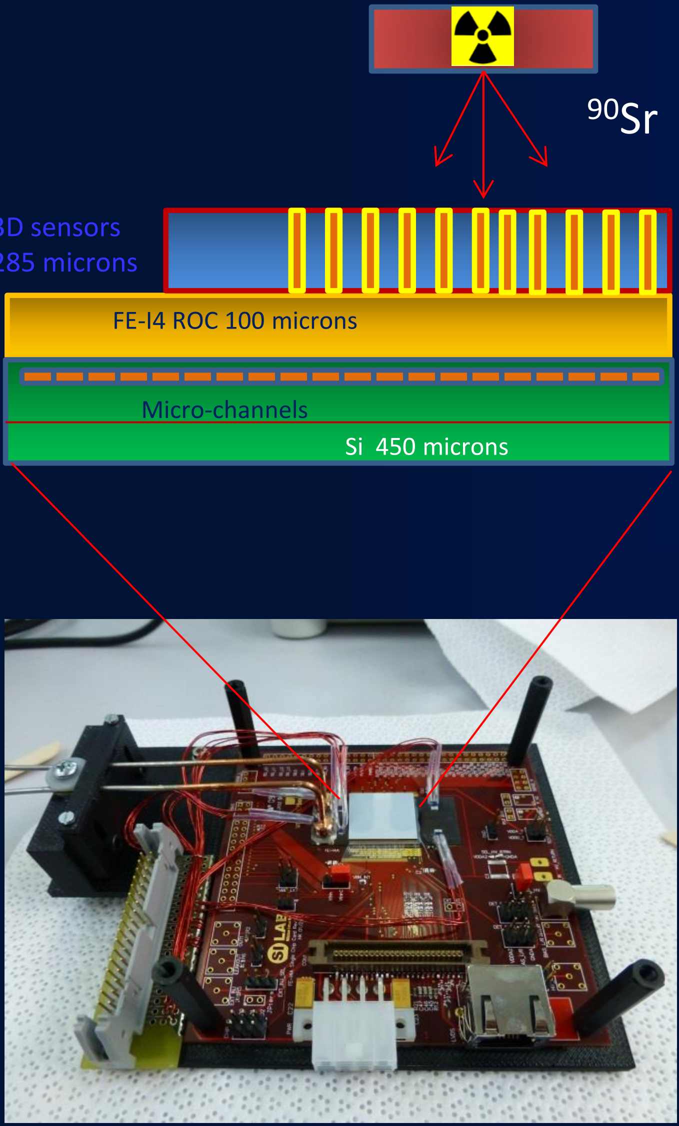
3D printed support in ABS with window inside to hold the PCB and support the micro-channels tubes!

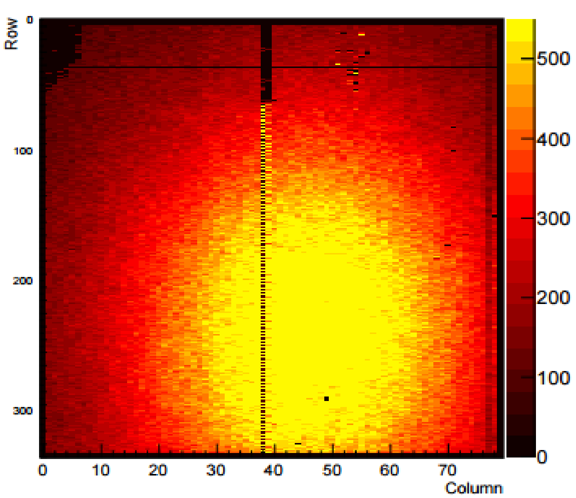


Kovar connectors laser soldered to stainless steel tube - to demonstrate the feasibility.

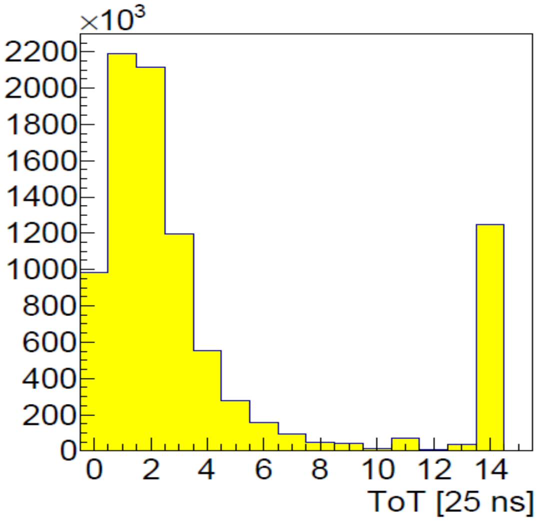
Cu coating of the connector and bending of the tube

Response to MIPs





occupancy



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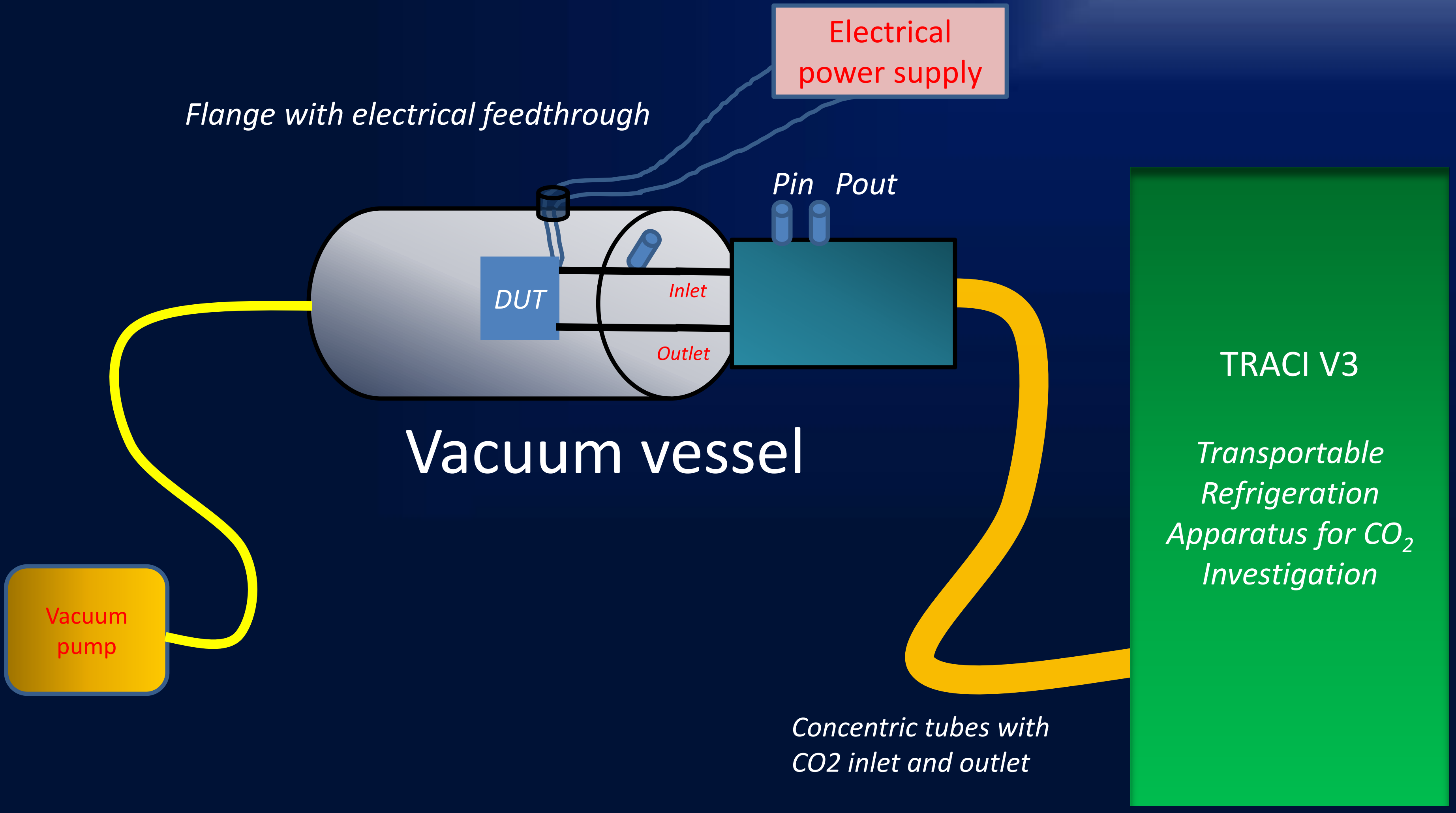
Thermal Characterization with TRACI



Installation and thermal sensors layout

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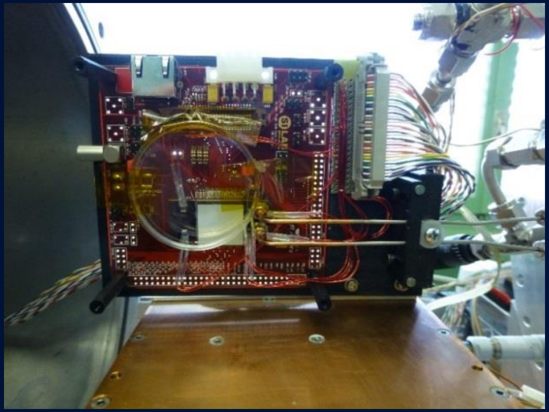
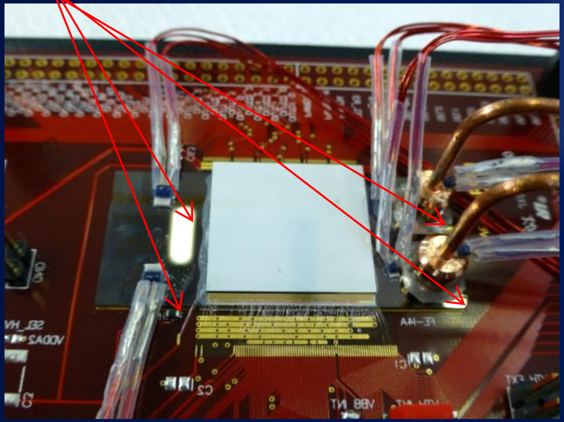
Board installed in the vacuum vessel

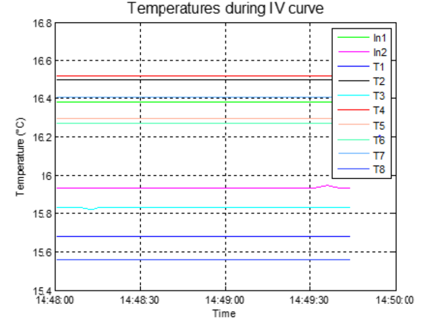


PT100s contacts **3-4-7-8**-on the micro-channel front sidechip



Vacuum level up to 10^{-3} mbar
Temperature down to -25 °C
Pressure readings

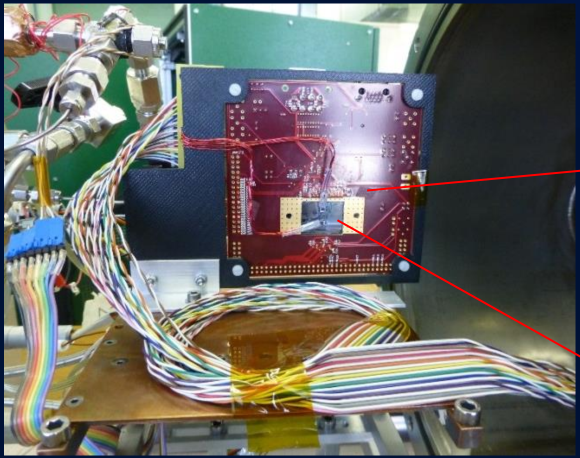
CO_2 flow from **TRACI** (Transportable Refrigeration Apparatus for CO_2 Investigation)



16.5

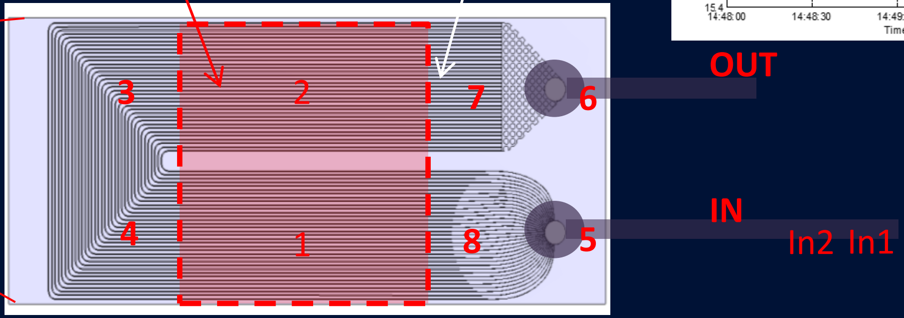
15.6

PT100 #1 and 2 glued on the back!!

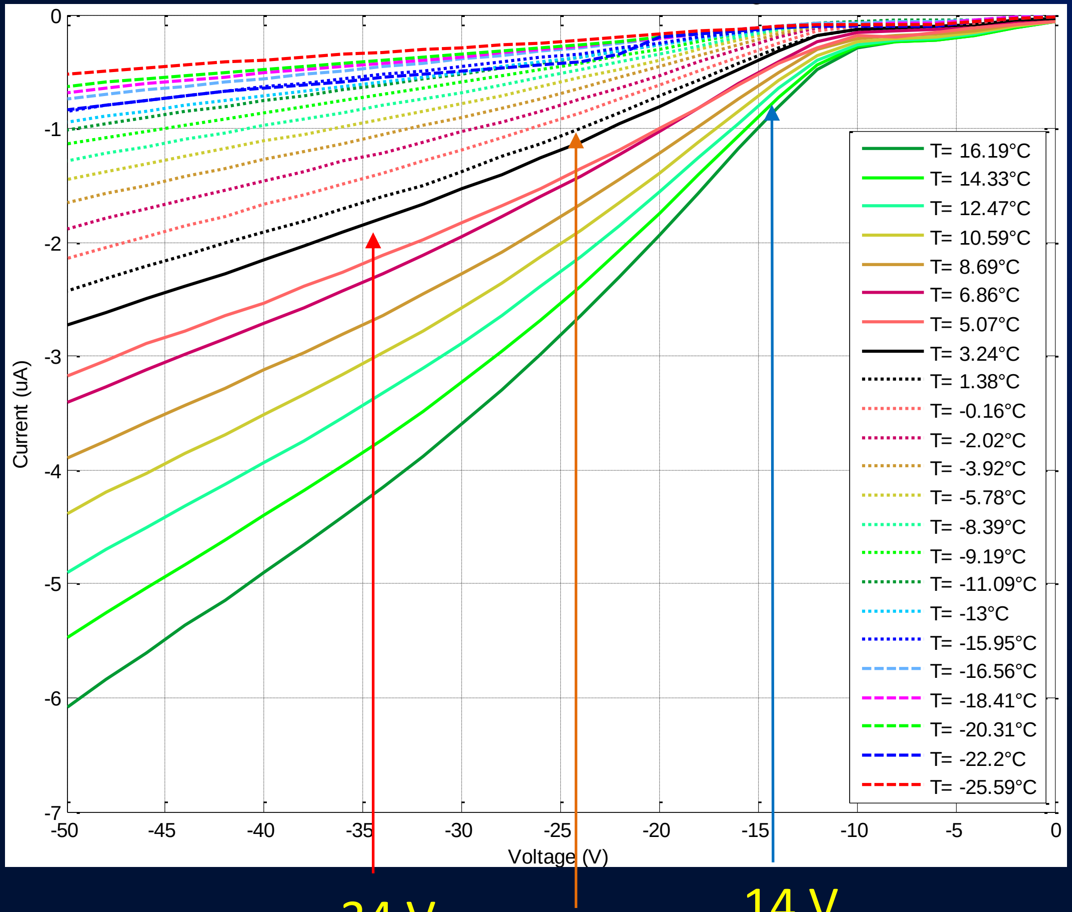


35 micro-channels
50 x 190 µm separated by 200 µm wide walls

Chip footprint



Leakage Current-Temperature Dependence



34 V

24 V

14 V

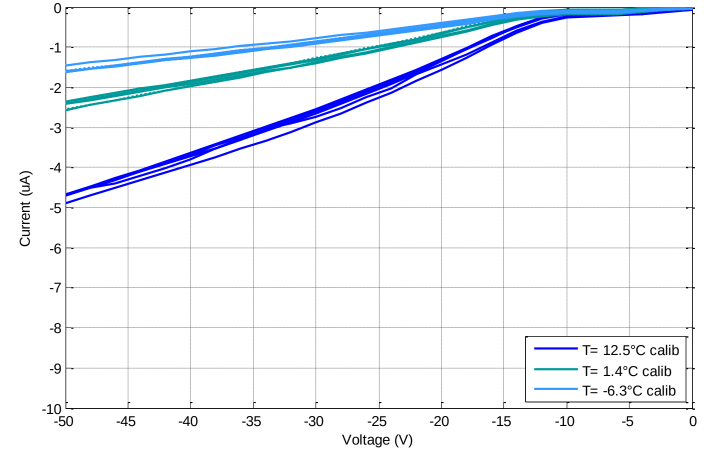
FE-I4 Chip OFF

- Δ T between T setpoint (on TRACI) and T measured is ~2°C
- T is a mean over 10 PT100 measurements on the micro channels
- Flow: CO2, 0.5 g/s

Temperature Repeatability

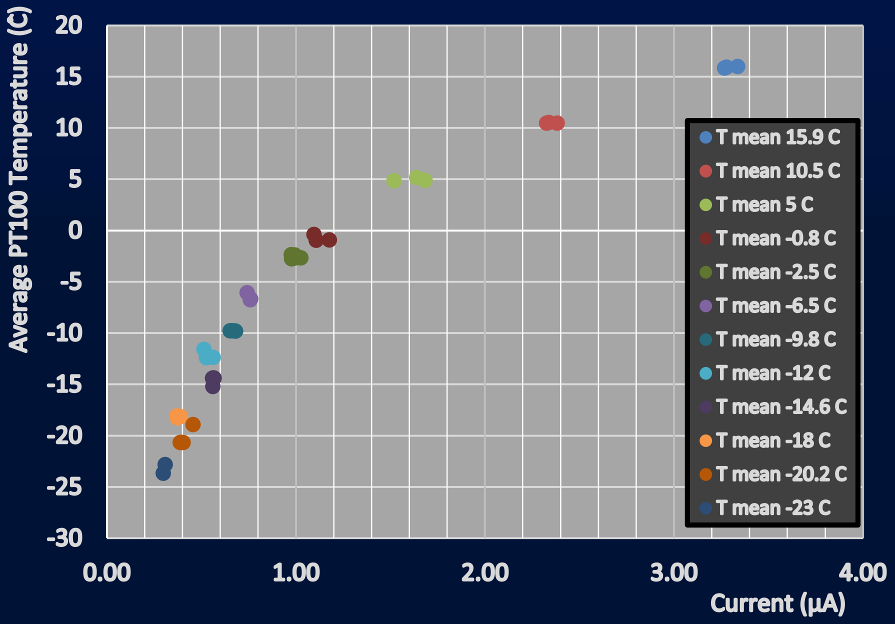
FE-I4 Readout electronics Chip OFF

- Temperature spanning done several times to check IV curves repeatability
- The resulting ΔI is due to small temperature differences between the curve and from ramp up/ramp down hysteresis

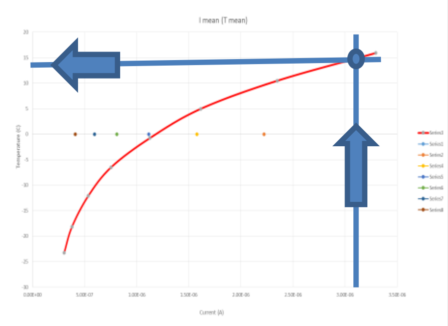


Constant Bias Voltage & varying Temperature

- Fixed Bias Voltage: **-30V**
- Various temperature points



Determination of the Thermal Figure of Merit



Extrapolated Ton or Toff

Measured current

STEP 1:

- Chip off: measure leakage current for certain temperature and fixed voltage (30V)
- Obtain curve for average leakage current

STEP 2:

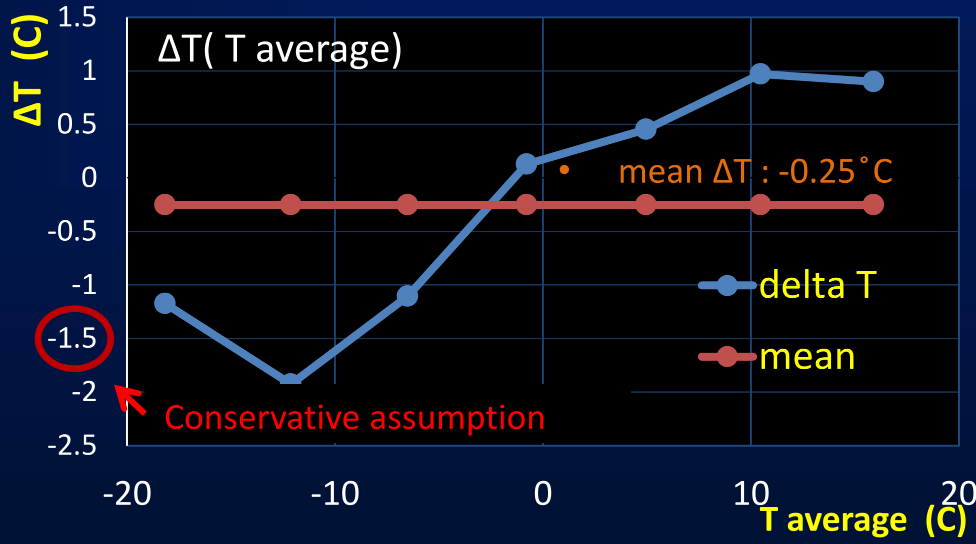
- Chip off: measure current
- Determine Toff by using curve
- As in vacuum T off = T CO2

STEP 3:

- Chip on: measure current
- Determine Ton by using curve

STEP 4:

- Determine ΔT = Toff - Ton



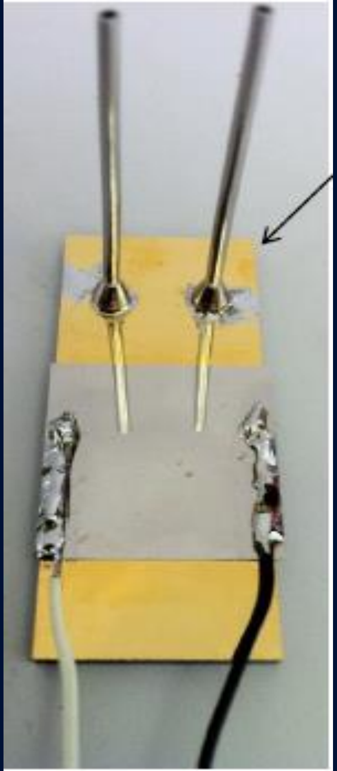
Thermal Figure of Merit (TFoM)

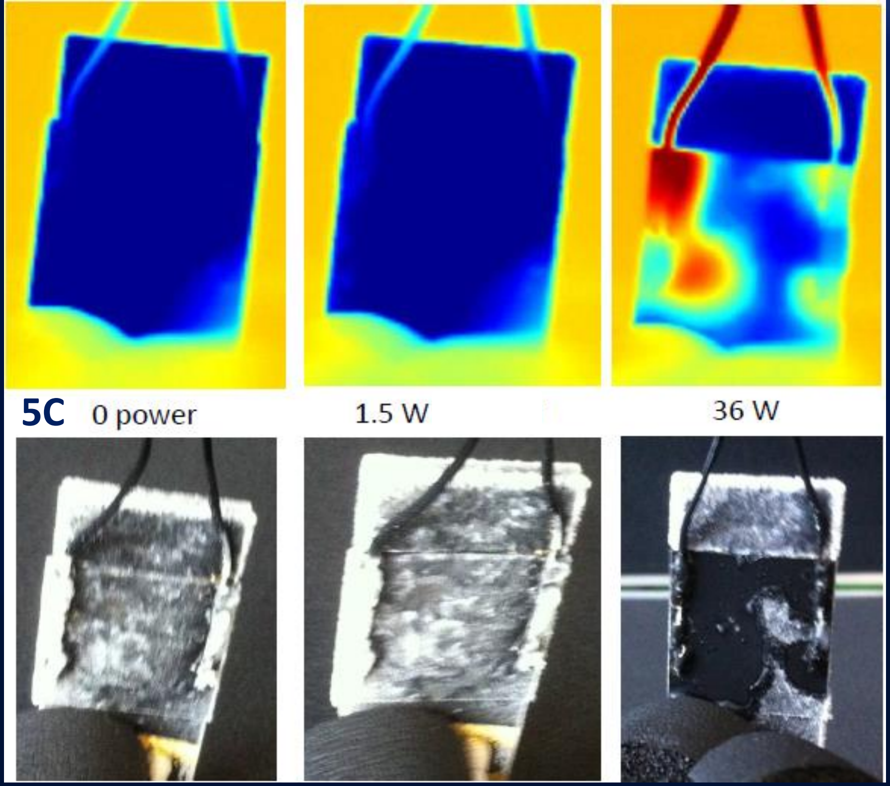
$$= \frac{\Delta T \cdot A}{Power} = \frac{1.5\ K \cdot 4cm^2}{1.5\ W} = 4\ \frac{K\ cm^2}{W}$$

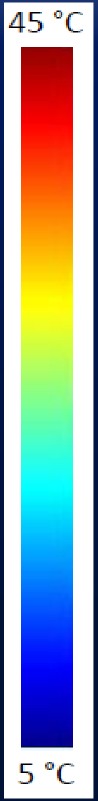
Best 2015 laboratory results for ITK studies (IBL configuration) TFoM = 13 K cm2/W

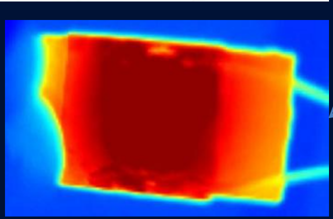
Direct Test of Thermal Figure of Merit

- Heater on a bare microchannel operated at room T to simulate power dissipation
- Temperature measured using an Infra-Red FLIR A655sc-Camera



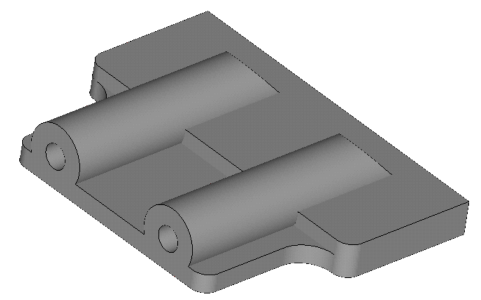




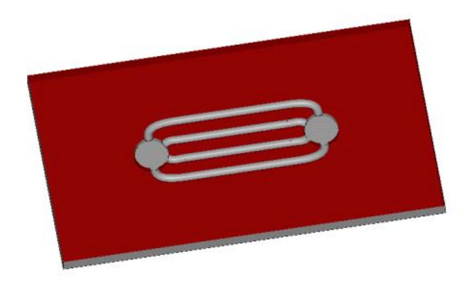


No cooling at 1.5 W!!!

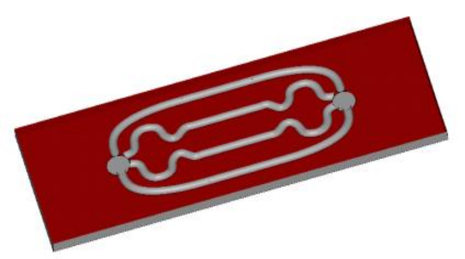
Addressing open questions
3D printed Alumina

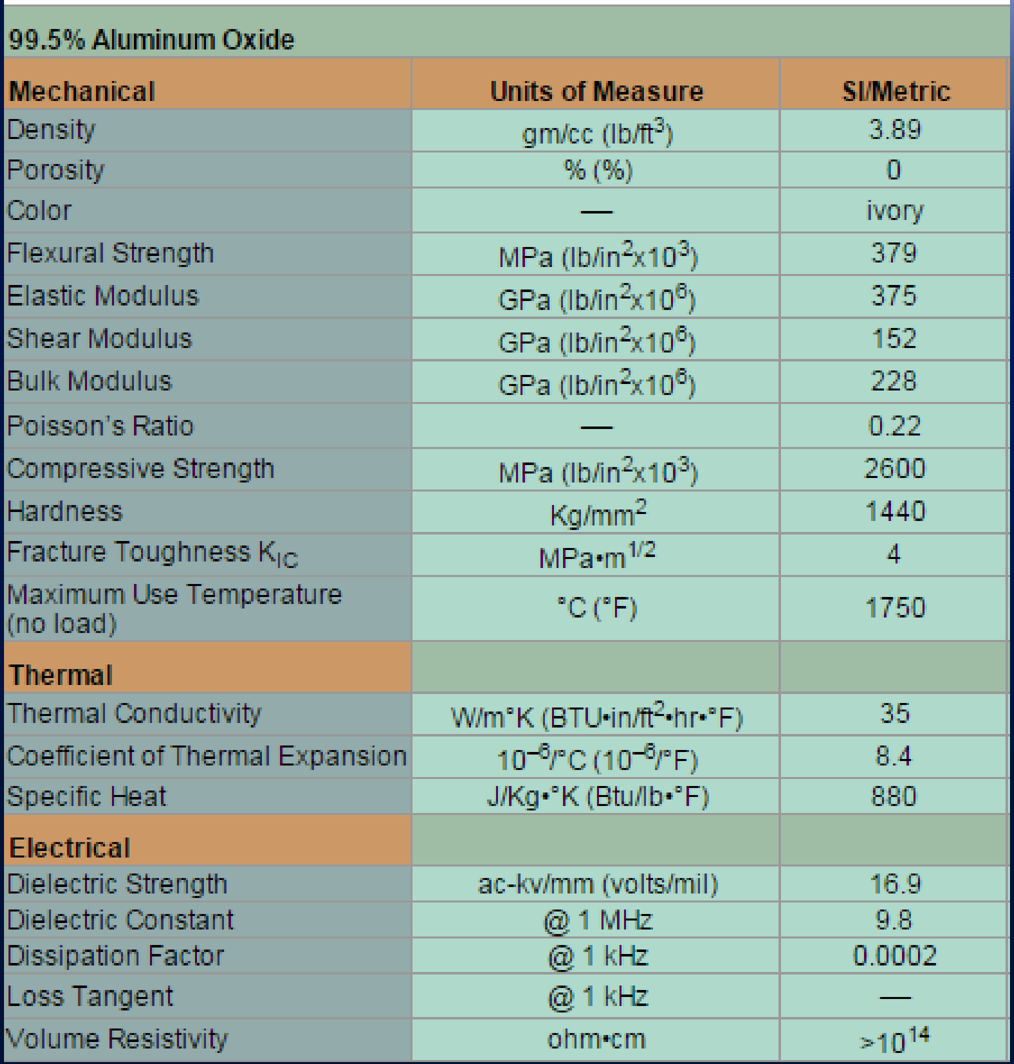


connectors



Prototypes micro-channels

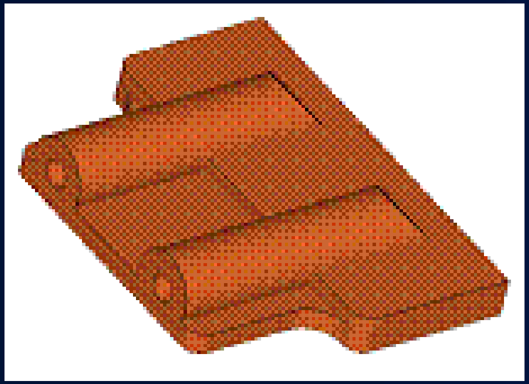




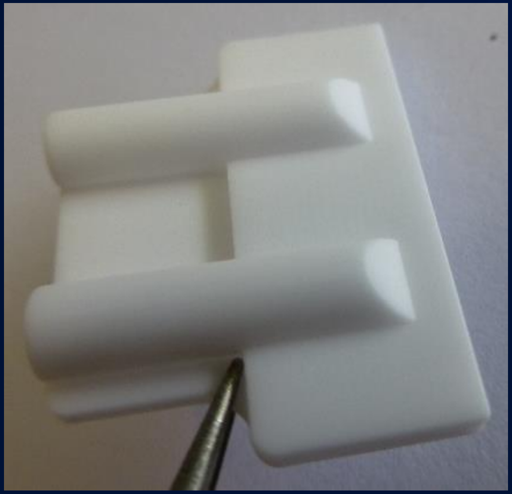
99.5% Aluminum Oxide		
Mechanical	**Units of Measure**	**SI/Metric**
Density	gm/cc (lb/ft^3)	3.89
Porosity	% (%)	0
Color	—	ivory
Flexural Strength	MPa (lb/in^{2}x10^3)	379
Elastic Modulus	GPa (lb/in^{2}x10^6)	375
Shear Modulus	GPa (lb/in^{2}x10^6)	152
Bulk Modulus	GPa (lb/in^{2}x10^6)	228
Poisson's Ratio	—	0.22
Compressive Strength	MPa (lb/in^{2}x10^3)	2600
Hardness	Kg/mm^2	1440
Fracture Toughness K$_{IC}$	MPa•m$^{1/2}$	4
Maximum Use Temperature (no load)	°C (°F)	1750
Thermal		
Thermal Conductivity	W/m°K (BTU•in/ft^2•hr•°F)	35
Coefficient of Thermal Expansion	10^{-6}/°C (10^{-6}/°F)	8.4
Specific Heat	J/Kg•°K (Btu/lb•°F)	880
Electrical		
Dielectric Strength	ac-kv/mm (volts/mil)	16.9
Dielectric Constant	@ 1 MHz	9.8
Dissipation Factor	@ 1 kHz	0.0002
Loss Tangent	@ 1 kHz	—
Volume Resistivity	ohm•cm	>10^{14}

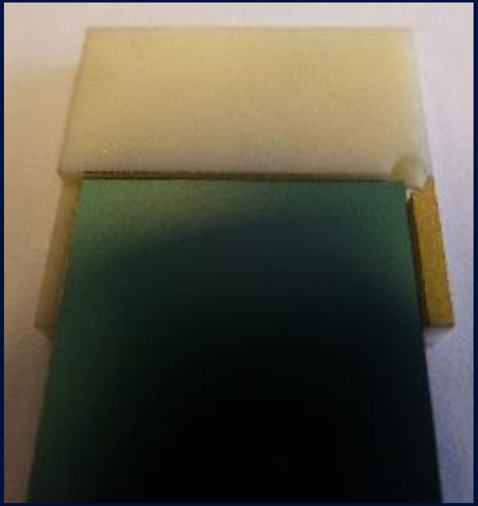
Si 2.6

Fludic connector in Alumina designed to match the ATLAS micro-channels design

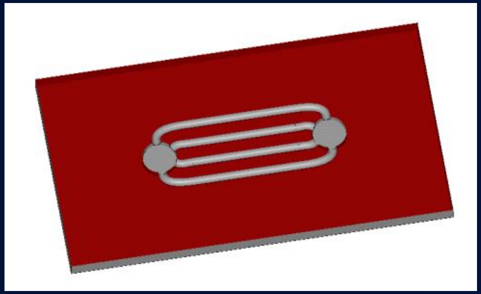


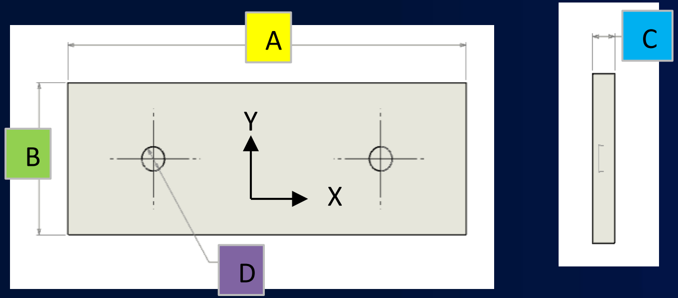
Soldering test with metallized ceramic on silicon

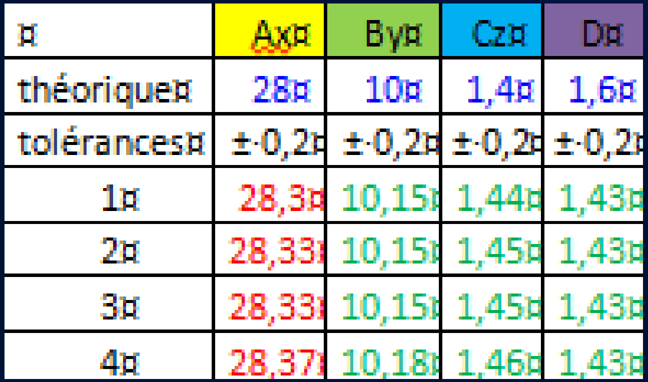




Alumina micro-channel prototype

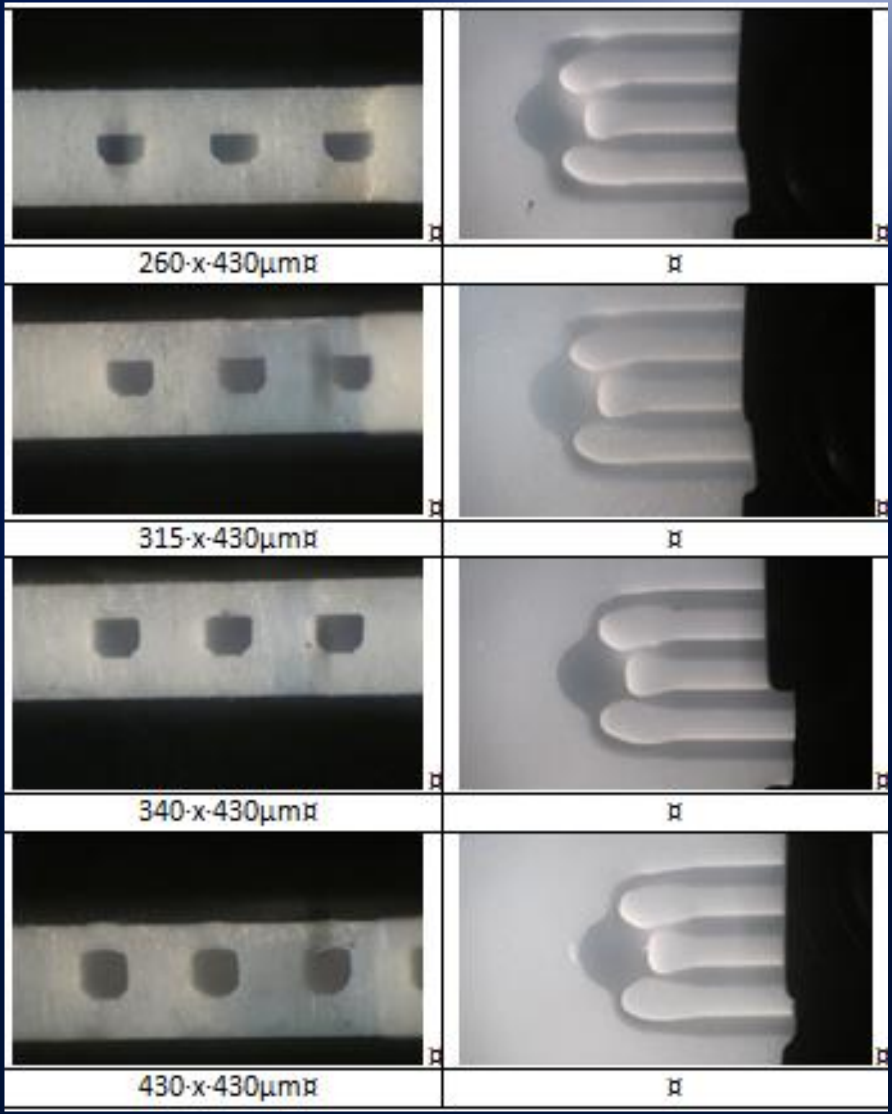






	Ax	By	Cz	D
théorique	28	10	1,4	1,6
tolérances	±0,2	±0,2	±0,2	±0,2
1	28,3	10,15	1,44	1,43
2	28,33	10,15	1,45	1,43
3	28,33	10,15	1,45	1,43
4	28,37	10,18	1,46	1,43

Scale = mm



260 x 430µm

315 x 430µm

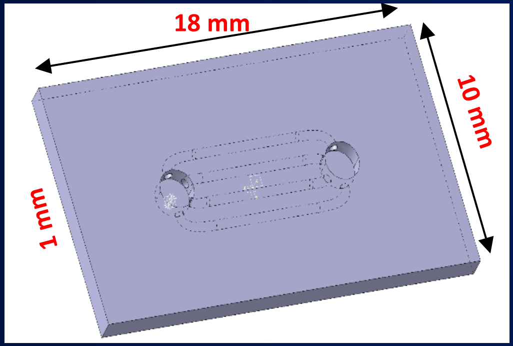
340 x 430µm

430 x 430µm

Ceramic Microchannel Prototypes

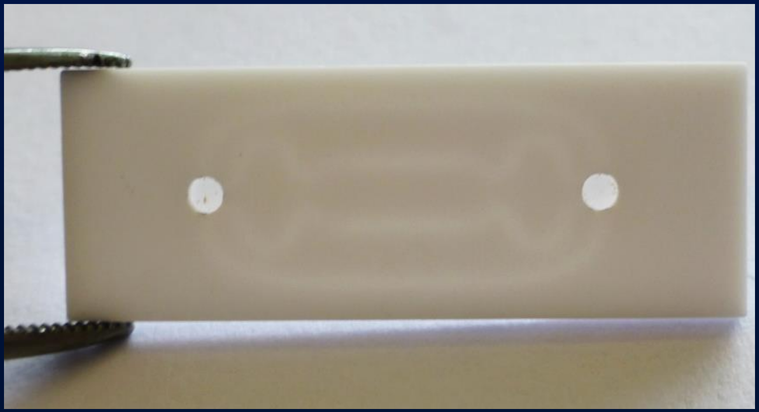
10 mm channels

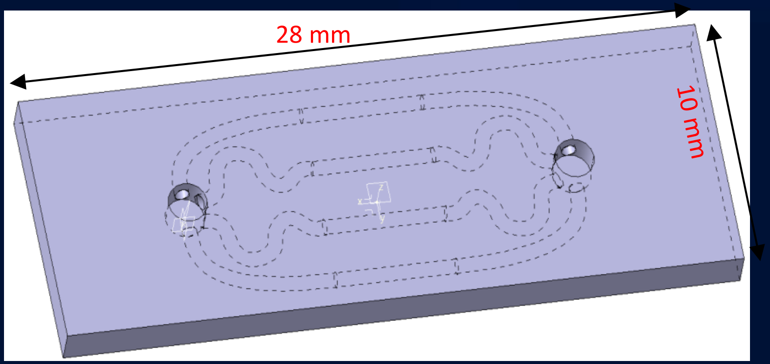
External channels lenght: 10.364 mm
Internal channels lenght: 8.26 mm
Straight part lenght: 5mm
Distance between holes: 8 mm
Inlet holes diameter: 1.6 mm



20 mm channels

4 Channels lenght: 20.52 mm
Straight part lenght: 5mm
Distance between holes: 16 mm
Inlet holes diameter: 1.6 mm





Conclusions and Plans

- ➢ The first integrated module with reduced radiation length composed by:

3D silicon sensor	285 um
FE-I4A readout chip	100 um
Si-Si microchannel cooling	500 um (not optimised)

was successfully tested showing normal electrical and thermal performances when cooled with CO2 with a figure of merit of 4 (1/3 of the current one)

- ➢ We plan to irradiate it to the FE-I4 limit (5x10^{15}ncm-^{2})

- ➢ We are planning to test alternative 3D printed Alumina connectors and channels. These might solve the open questions on the potential use of micro-channel cooling in inner pixel layers.

- ➢ 3D printed ceramic could be used to fabricate staves!

If this works it might make micro-channel cooling a possible option by the time of the PH2 since fabrication time (and tests) could be faster