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Recent results with HV-CMOS and planar sensors for the CLIC vertex detector

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The physics aims at a future multi-TeV CLIC linear e+e- collider impose high precision requirements on the vertex detector. The detector also has to match the experimental conditions, such as the time structure of the collisions and the presence of beam-induced backgrounds. The principal challenges are: a point resolution of 3 micron, 10 ns time stamping capabilities, ultra-low mass (0.2% X0 per layer), very low power dissipation (compatible with air-flow cooling) and pulsed power operation. The R&D for the pixel detector follows an integrated approach addressing simultaneously the physics requirements and the engineering constraints. Two types of hybrid pixel detectors with ultra-small pitch (25*25 micron) and analogue readout are explored. Both make use of a dedicated readout ASIC (CLICpix), developed in 65 nm technology. CLICpix is either bump bonded to ultra-thin planar silicon sensors (with and without active edges), or AC coupled through a thin layer of glue to active HV-CMOS sensors. Results of recent beam tests and laboratory calibrations of a variety of assemblies with different sensor thicknesses are presented. Detailed simulations based on Geant4 and TCAD validate the experimental results and serve to optimise the detector design. The R&D project also includes the development of through-silicon via (TSV) technology, as well as various engineering studies involving thin mechanical structures and full-scale air-cooling tests.

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