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A 65 nm CMOS analog processor with zero dead time for future pixel detectors

Next generation pixel chips at the High-Luminosity (HL) LHC will be exposed to extremely high levels of radiation and particle rates. In the so-called Phase II upgrade, ATLAS and CMS will need a completely new tracker detector, complying with the very demanding operating conditions and the delivered luminosity (up to $5 \times 10^{34}\mathrm{cm}^{-2}\mathrm{s}^{-1}$ in the next decade).
This work is concerned with the design of a synchronous analog processor with zero dead time developed in a 65 nm CMOS technology, conceived for pixel detectors at the HL-LHC experiment upgrades. It includes a low noise, fast charge sensitive amplifier featuring a detector leakage compensation circuit, and a compact single ended comparator that guarantees very good performance in terms of channel-to-channel dispersion of threshold without needing any pixel-level trimming. A 3-bit Flash ADC is exploited for digital conversion immediately after the preamplifier.
The conference paper will provide a thorough discussion on the design of the different blocks making up the analog front-end channel.

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