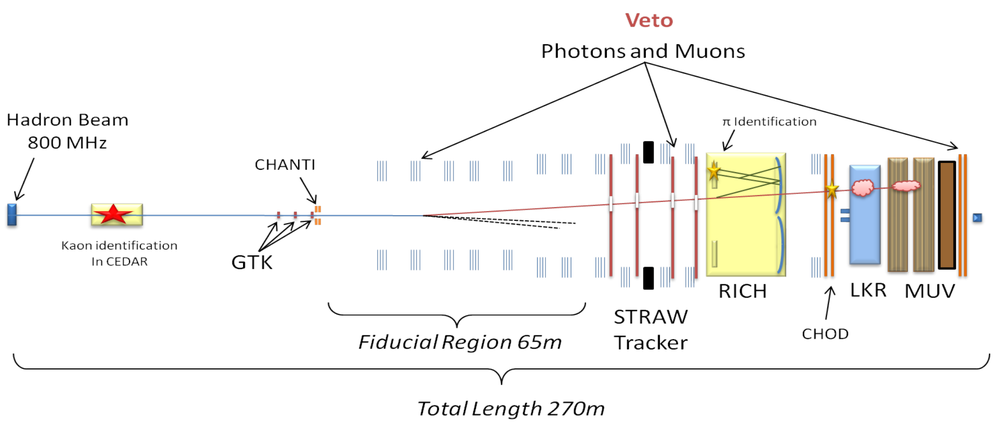
Vienna Conference
on Instrumentation

The Level 0 Trigger Processor - NA62 Experiment

Dario Soldi - INFN, University of Turin (Italy)



The main purpose of the experiment NA62 at CERN - SPS is to measure the branching ratio of the (ultra) rare decay

$$K^+ \to \pi^+ \nu\bar{\nu}$$

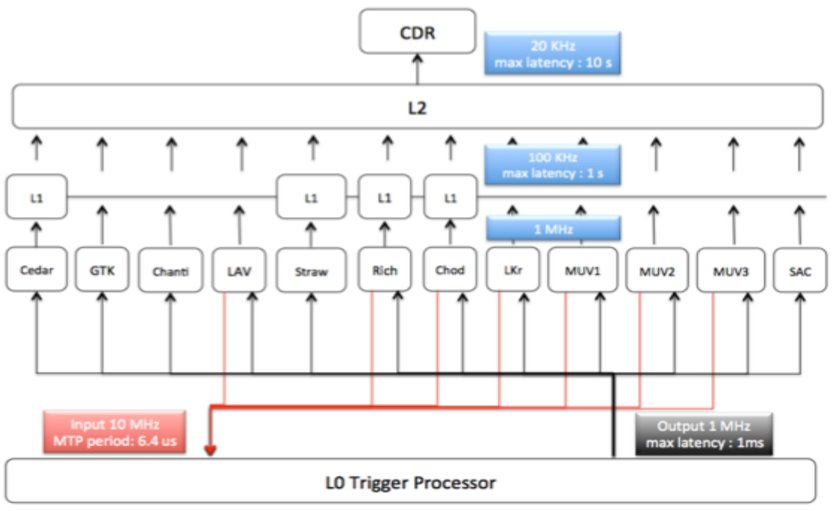
The expected value, according to the Standard Model, is of the order of 10^{-10} thus requiring a high intensity kaon beam. The intense flux of particles requires a high-performance trigger and data acquisition system. **The Level 0 (L0) trigger** permits to introduce simply cuts to select particular event types and should be flexible to allow for emerging requirements in later stages of the experiment.

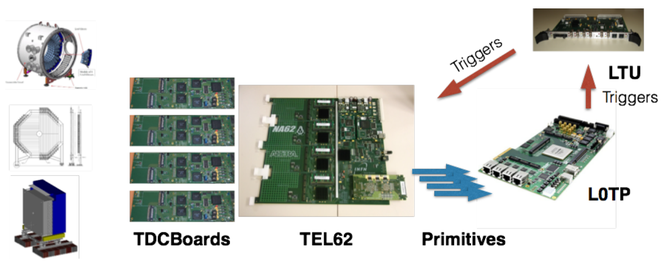
NA62 Trigger Levels:

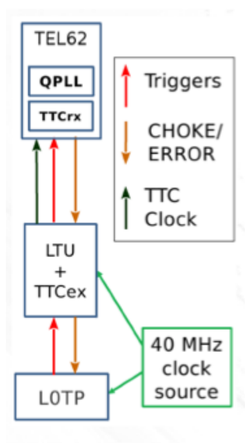
- L0: Hardware synchronous level. 10 MHz to 1 MHz. Max latency: 1 ms.
- L1: Software level. "Single detector". 1 MHz to 100 kHz. Max latency: O(1 s).
- L2: Software level. "Complete information". 100 kHz to O(kHz). Max latency: spill period O(10 s) .

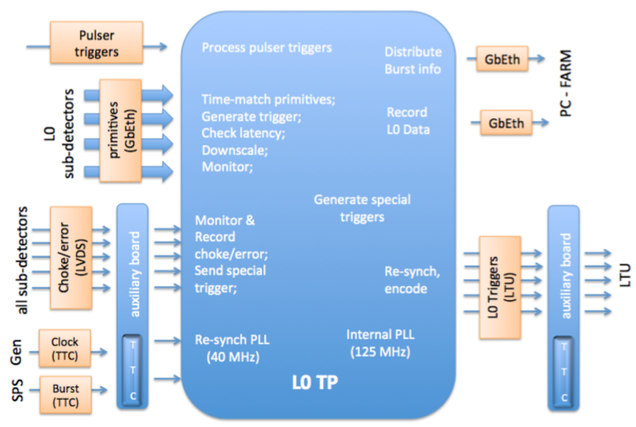
L0TP Features:

- Data not sorted in time are sent from detector to L0TP via Ethernet using UDP protocol (primitives) every 6.4 us.
- Primitives form different sources (max 7) are realigned the L0TP
- Primitives are compared with pre-selected masks.
- Triggers are sent to the Timing Trigger and Control (TTC) system with fixed latency.



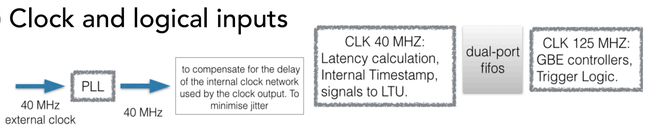


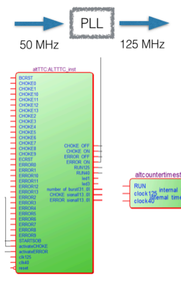




L0 Trigger Processor

1) Clock and logical inputs

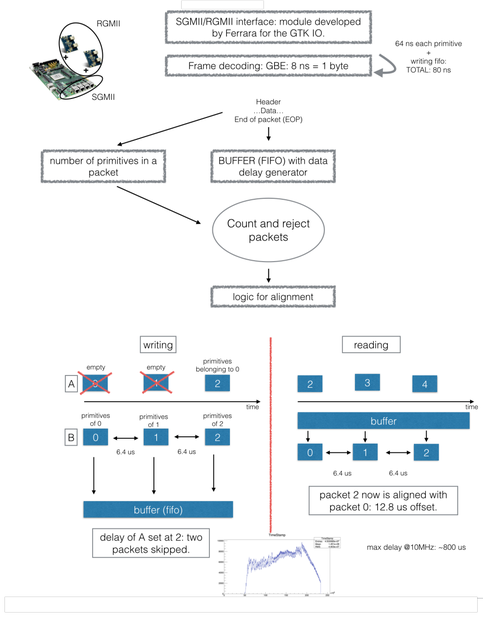




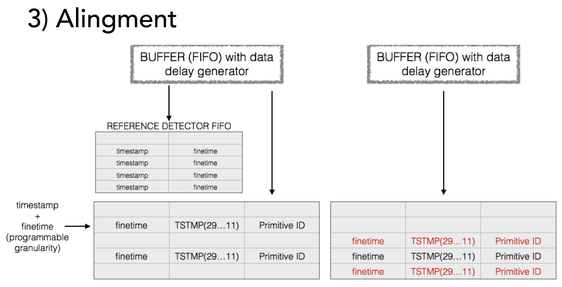
All pins are registered.
The Synchronisation is done with a two-stage shift-register that is clocked by the target domain's clock.

```
process(clk40, reset) is
begin
  if(rising_edge(clk40)) then
    if(reset = '1') then
      ERROR_s1 <= (others=>'0');
      ERROR_s2 <= (others=>'0');
    else
      ERROR_s1 <= ERROR;
      ERROR_s2 <= ERROR_s1;
    end if;
  end if;
end process;
```

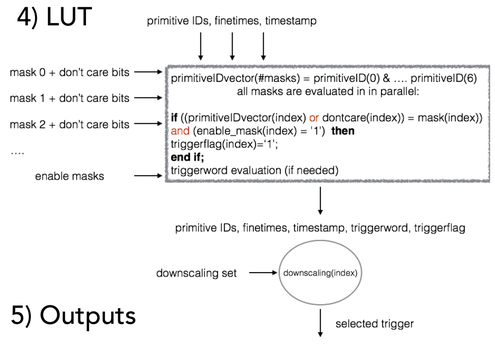
2) Ethernet interface



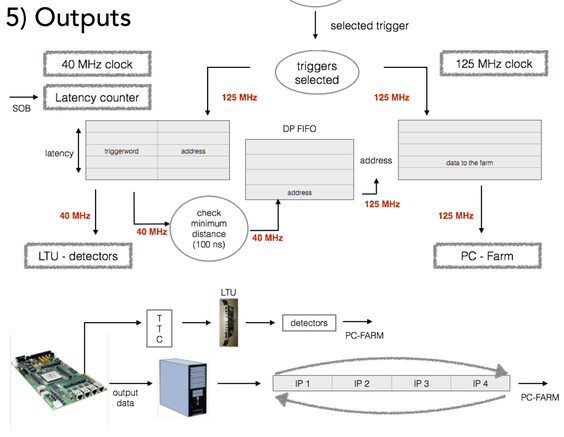
3) Alingment

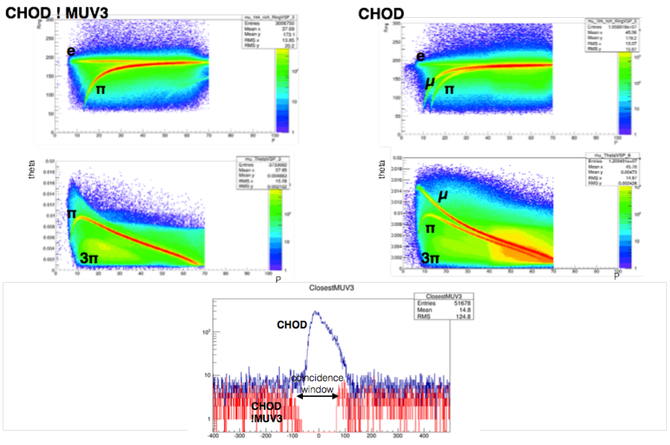


4) LUT

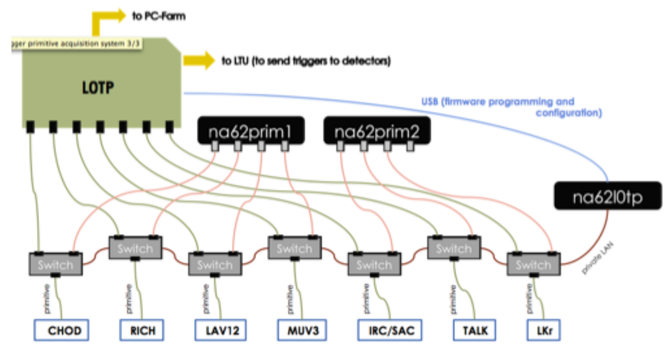


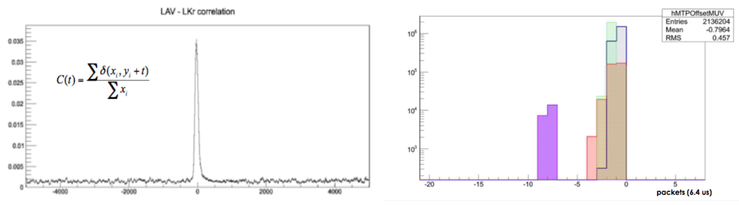
5) Outputs





Detector alignment





Development platform

Received Triggers are sampled with an internal clock and labeled with the internal timestamp and sent to a computer via ethernet.

Trigger In

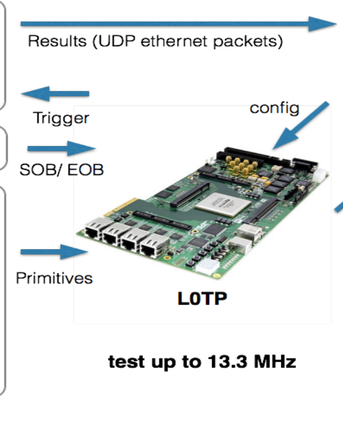
Clock 40 MHz, SOB/EOB, CHOKE/ERROR generator

Ram With Primitives

MTP packet generator: Primitive packets every 6.4 us.

Due to the maximum size of the ram, the primitives are read in loop modifying the time.

Three sources available.



test up to 13.3 MHz