



Low Energy Proton Detector for the PENeLOPE Experiment



D. Gaisbauer^a,

F. J. Hartmann^a, I. Konorov^a, S. Paul^a,

R. Picker^b, W. Schreyer^a, D. Steffen^c, R. Stoepfer^a, C. Tietze^a

(a) Technische Universität München, Germany

(b) TRIUMF, Vancouver, Canada

(c) CERN, Genève, Switzerland



Project Description

Ultra-Cold Neutrons (UCN)

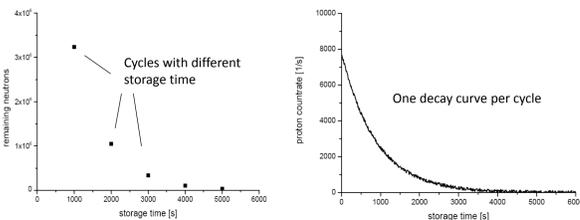
- kinetic energy below 300 neV

PENeLOPE

- Precision Experiment on Neutron Lifetime Operating with Proton Extraction
- lossless storage of UCN in magneto-gravitational trap
- neutron lifetime derived from neutron and proton counting
- aspired precision 0.1 s

Proton Detection

- charged decay particle extraction and detection
- extraction efficiency 69% (protons) and 37% (electrons)



Detector Requirements

Energy of Protons

- 30 keV

High Voltage Environment

- detector and electronics on -30 kV

Magnetic Field Environment

- 0.6 T

Low Temperature

- 77 Kelvin
- low heat input

Vacuum Compatibility

- 10⁻⁸ mbar
- low outgassing

Large Area

- 0.23 m²

Frontend Communication

Switched Enabling Protocol (SEP)

- time-division multiplexing transport layer protocol
- star like optical network (1:n) or point to point connection (1:1)
- readout in Round-Robin manner
- determined latency for time critical messages
- 98% link utilization efficiency for PENeLOPE

Higher level protocols

- data transmission
- IPBus (control of complete DAQ electronics)
- time distribution
- JTAG interface

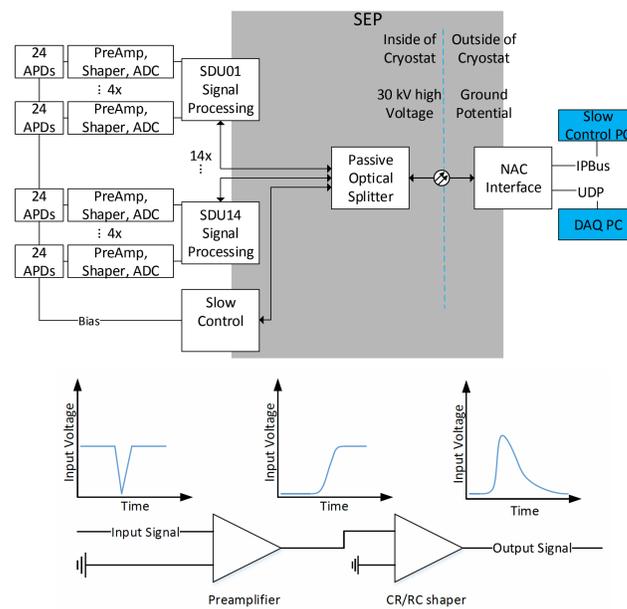
Transmission Time [μs]	Efficiency [%]
25000	99,93
10000	99,84
1000	98,42
500	96,90
100	86,20

Total link utilization efficiency of SEP for different times a slave can transmit data

PENeLOPE Proton Detector Readout

Complete Readout Scheme

- 14 SDU blocks with each 96 channels
- 1:16 passive optical splitter
- slow control card controlling the bias of the APDs
- all electronics inside the cryostat on -30 kV
- Network Access Controller (NAC) outside of cryostat to further process data and establish connection to PCs



Avalanche Photodiodes

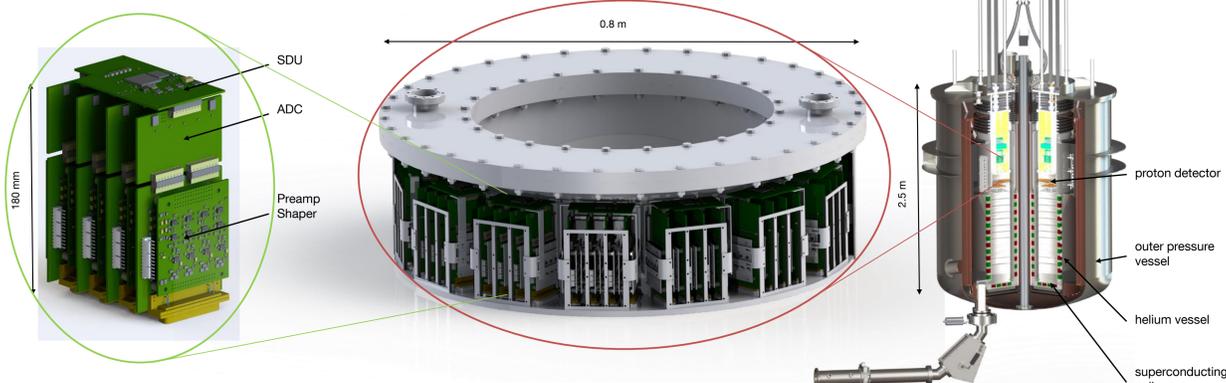
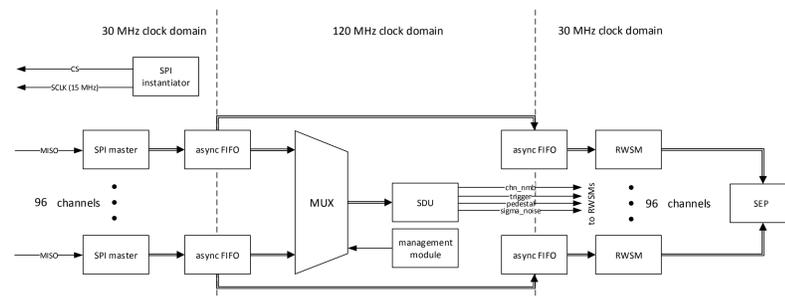
- Hamamatsu S11048
- 6.8 x 14 mm² active area
- 9 x 18 mm² size
- terminal capacitance of 220 pF
- no epoxy cover
- operational voltage of 240 to 270 V
- liquid nitrogen cooled to 77 K

Preamplifier, Shaper and ADC

- CR/RC shaper architecture with 1 μs time constant
- long time constant possible due to low trigger rate
- ADC card for 24 channels each using a 12 bit SAR ADC

Signal Detection Unit (SDU)

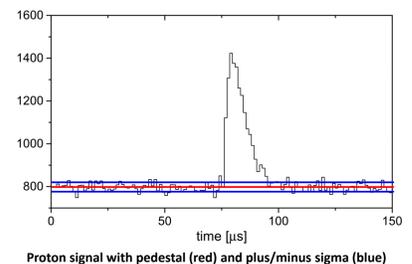
- 1 MHz sampling rate
- Xilinx Spartan 6 LX150T
- detects events and formats the signals provided by the ADCs



Trigger Algorithm

FPGA Signal Detection Algorithm

- "Real-time" pedestal calculation: Averaging over N_{avg} samples
- calculating sigma noise over N_{avg} samples: calculating quadratic deviation from mean value
- signal detection: If n_s consecutive samples $> pedestal + x_f \cdot \sigma$
- trigger threshold configurable to exactly defined signal/noise ratio
- each channel is treated by itself



Test Results

Beam results

- proton beam test at the paff accelerator
- 1.29 keV energy resolution at 300 K
- usable with proton energies down to about 15 keV

