



Improved Process Technologies in the SOI Pixel Detectors

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<http://rd.kek.jp/project/soi/>

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Outline

I. Introduction

II. Recent Progress

***Layout Shrinking with NMOS-PMOS merge**

***Double SOI Wafer & Process**

***Higher Dose LDD**

***Compensation with Tunneling**

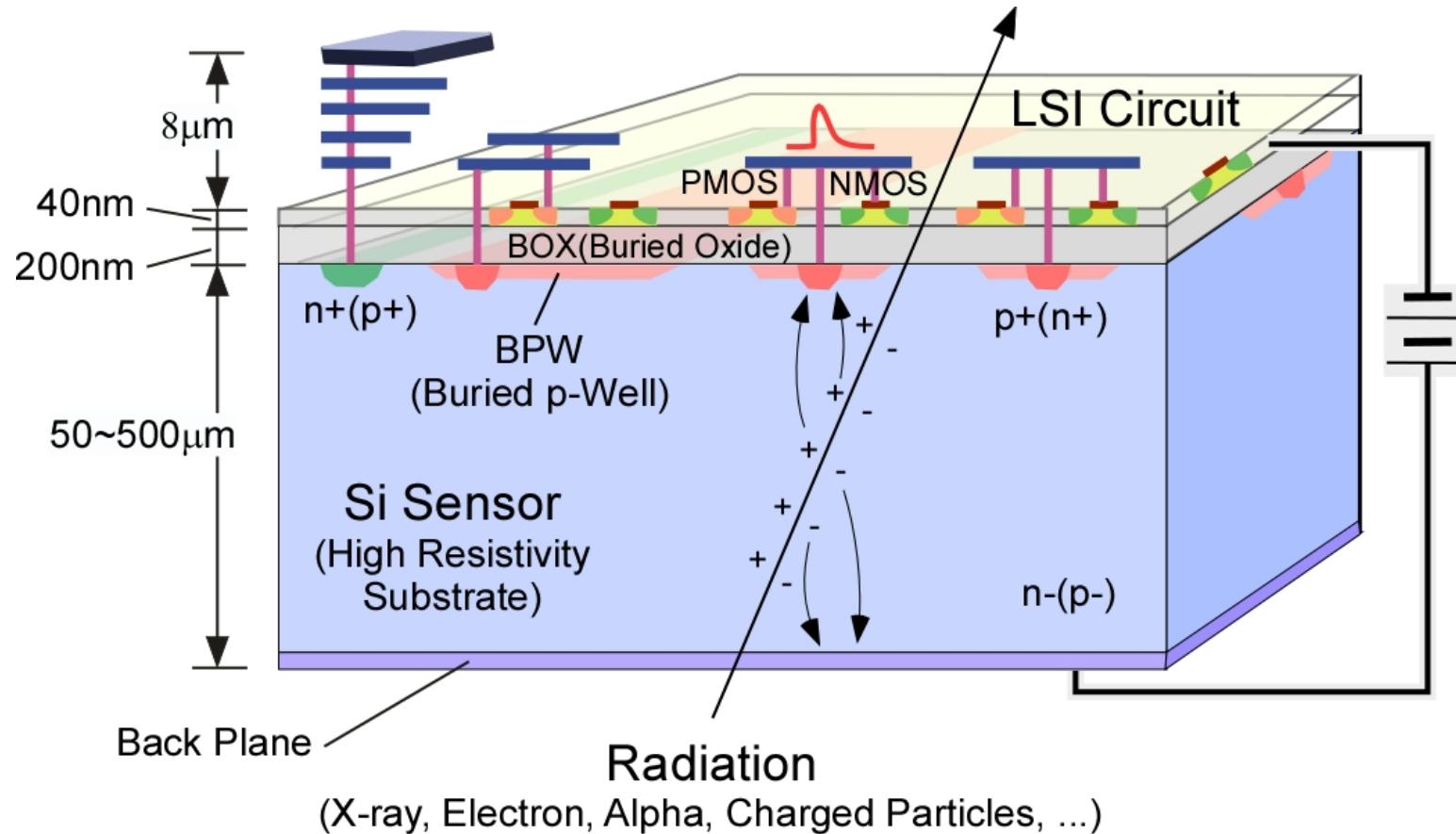
III. Summary

SOIPIX Poster Presentations

- ‘Development of a pixel sensor with fine space-time resolution based on SOI technology for the ILC vertex detector’, S. Ono, et al.
- ‘Development of an Event-driven SOI Pixel Detector for X-ray Astronomy - Improvement of an Intra-chip Readout Circuit for Low Noise Performance’, A. Takeda, et al.

I. Introduction

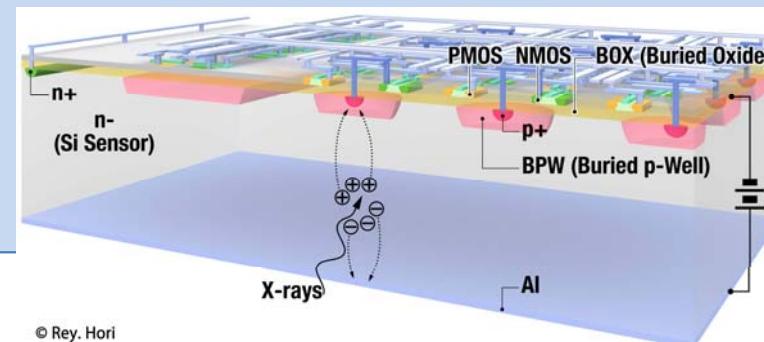
Silicon-On-Insulator Pixel Detector (SOIPIX)



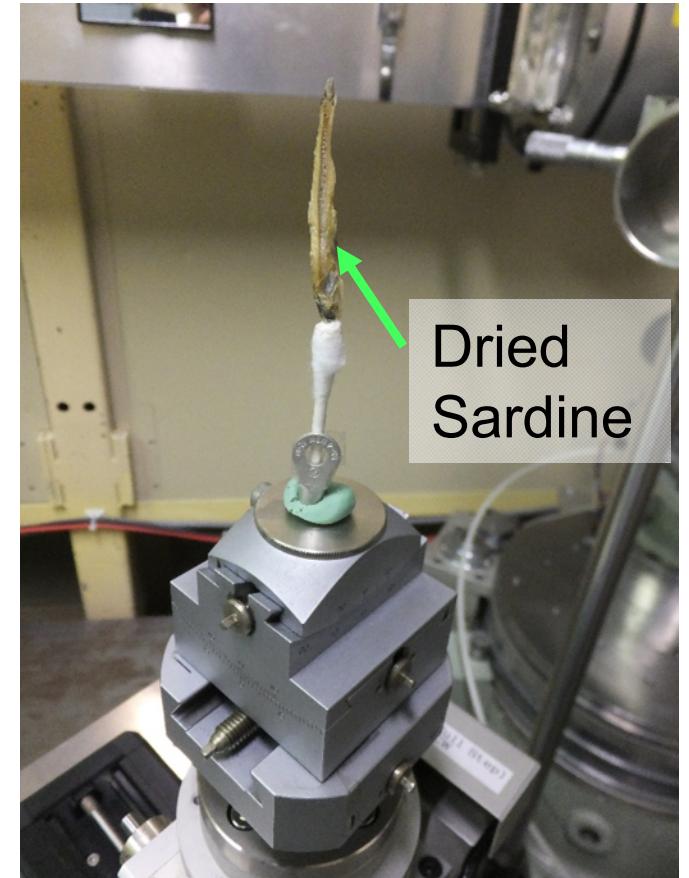
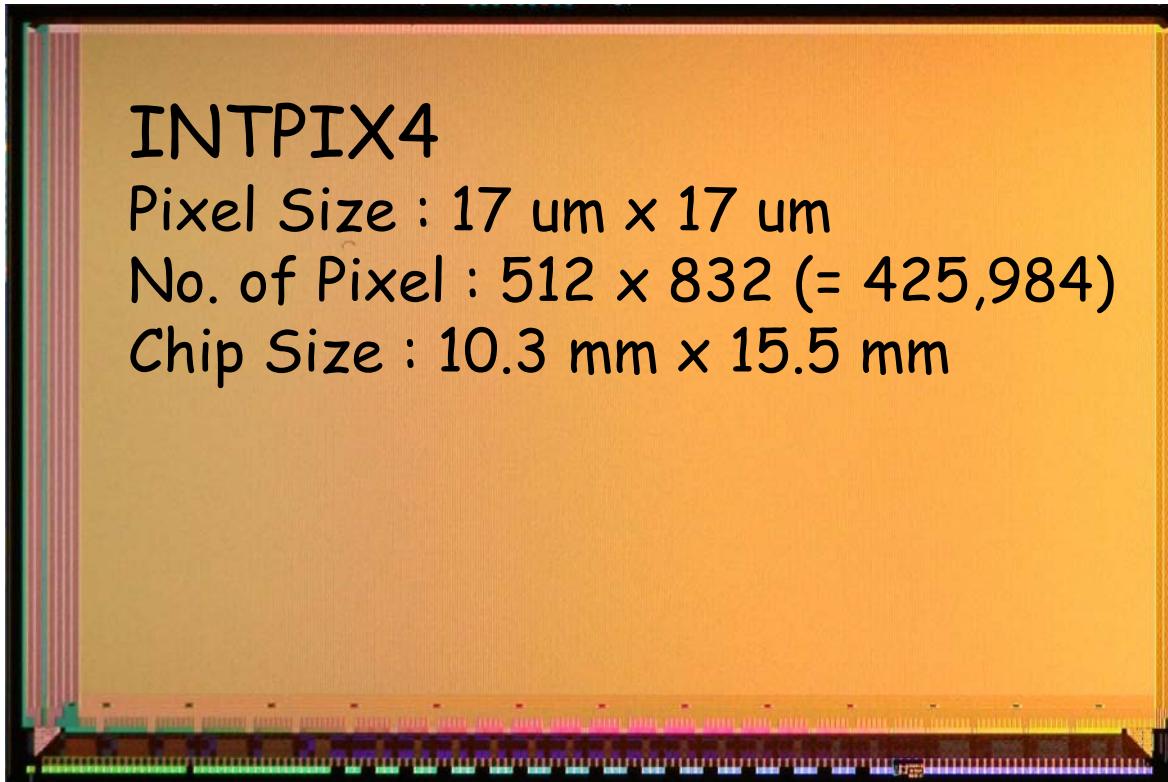
Monolithic Detector having fine resolution of silicon process and high functionality of CMOS LSI by using a SOI Pixel Technology.

Features of SOI Pixel Detector

- Monolithic device. No mechanical bonding.
- Fabricated with semiconductor process only, so high reliability and low cost are expected.
- High Resistivity fully depleted thick sensing region with Low sense node capacitance.
- On Pixel processing with CMOS transistors.
- No Latch up and Low single event cross section.
- 100% Fill-Factor with Back Illumination.
- Can be operated in wide temperature (1K-570K) range.
- Based on Industry Standard Technology.

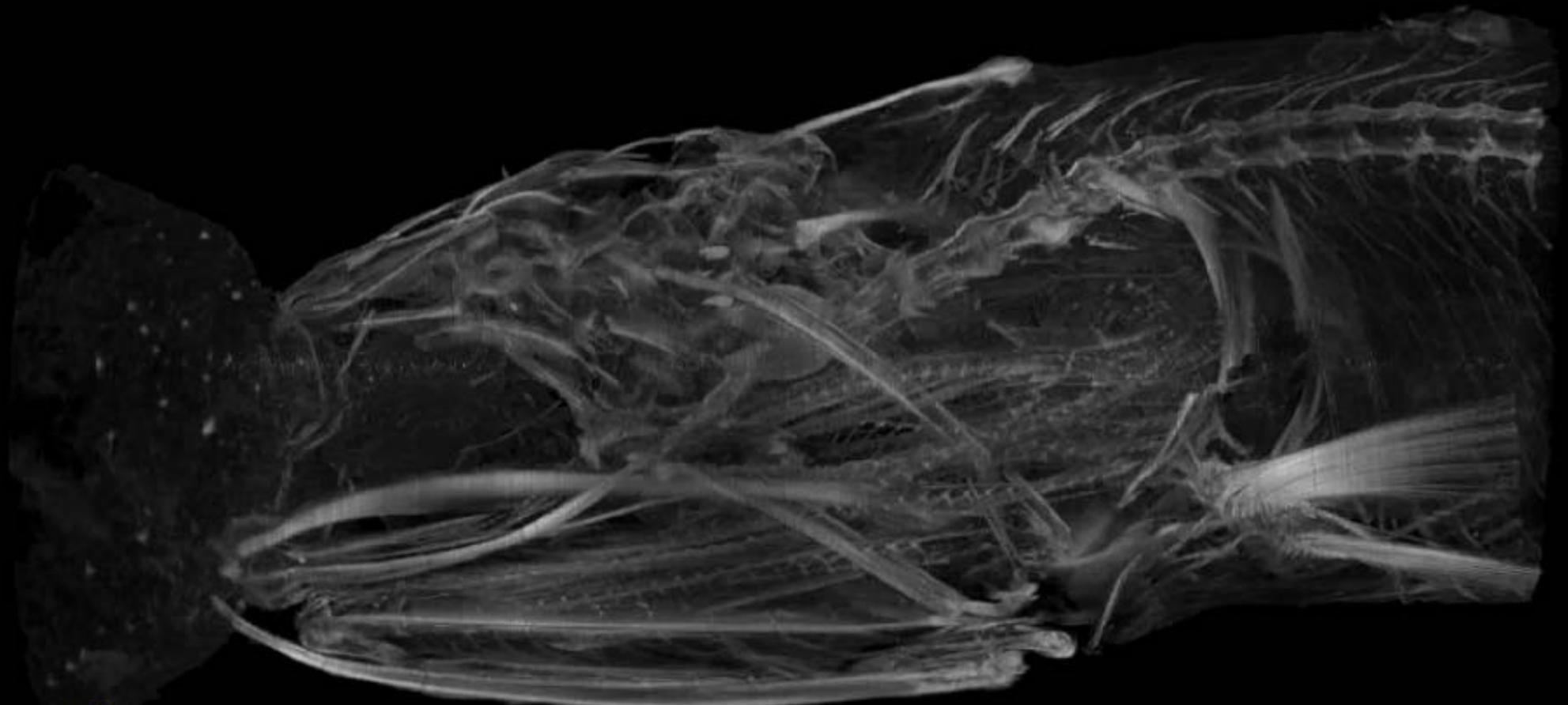


3D Tomographi with Syncrotron X-ray



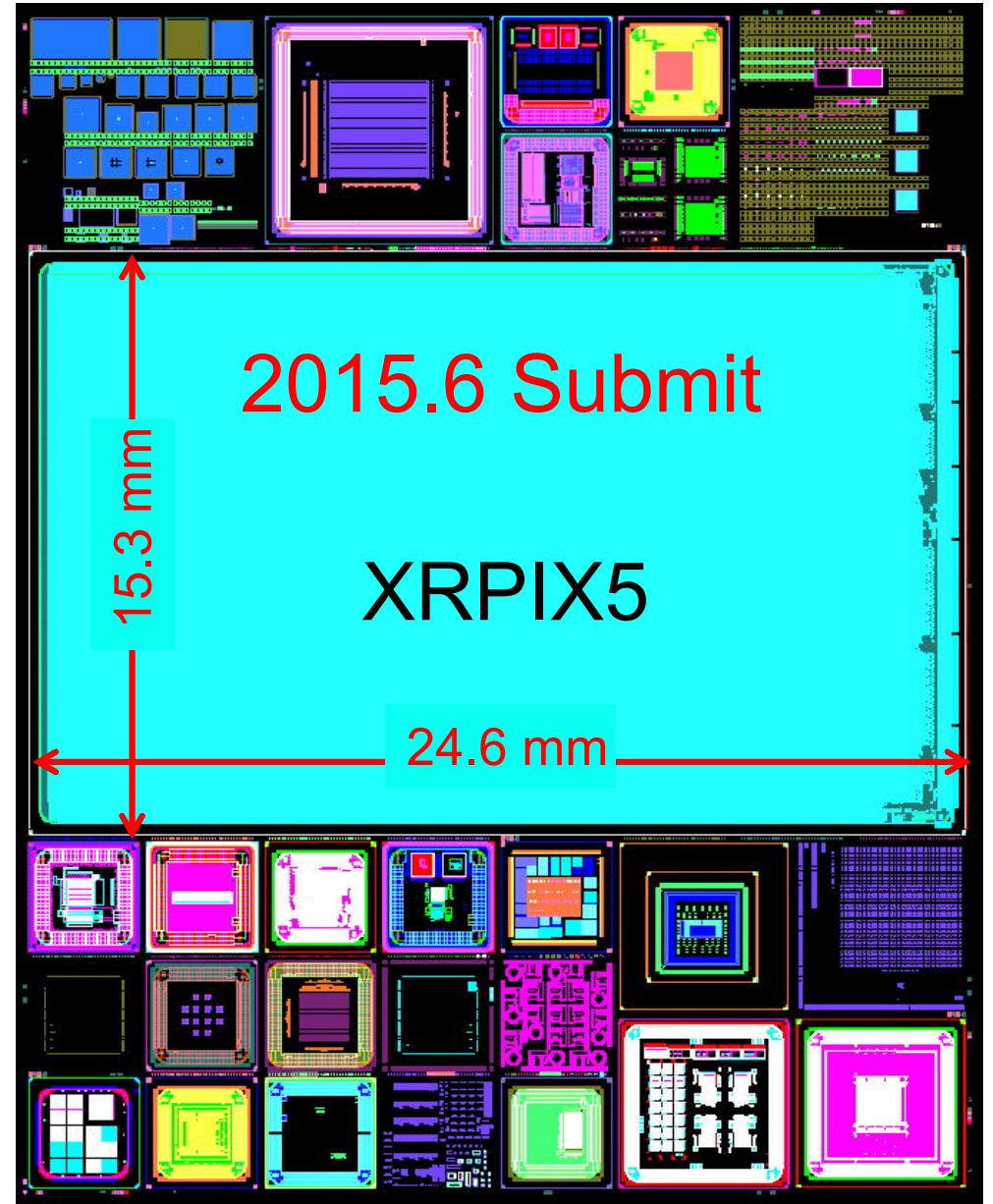
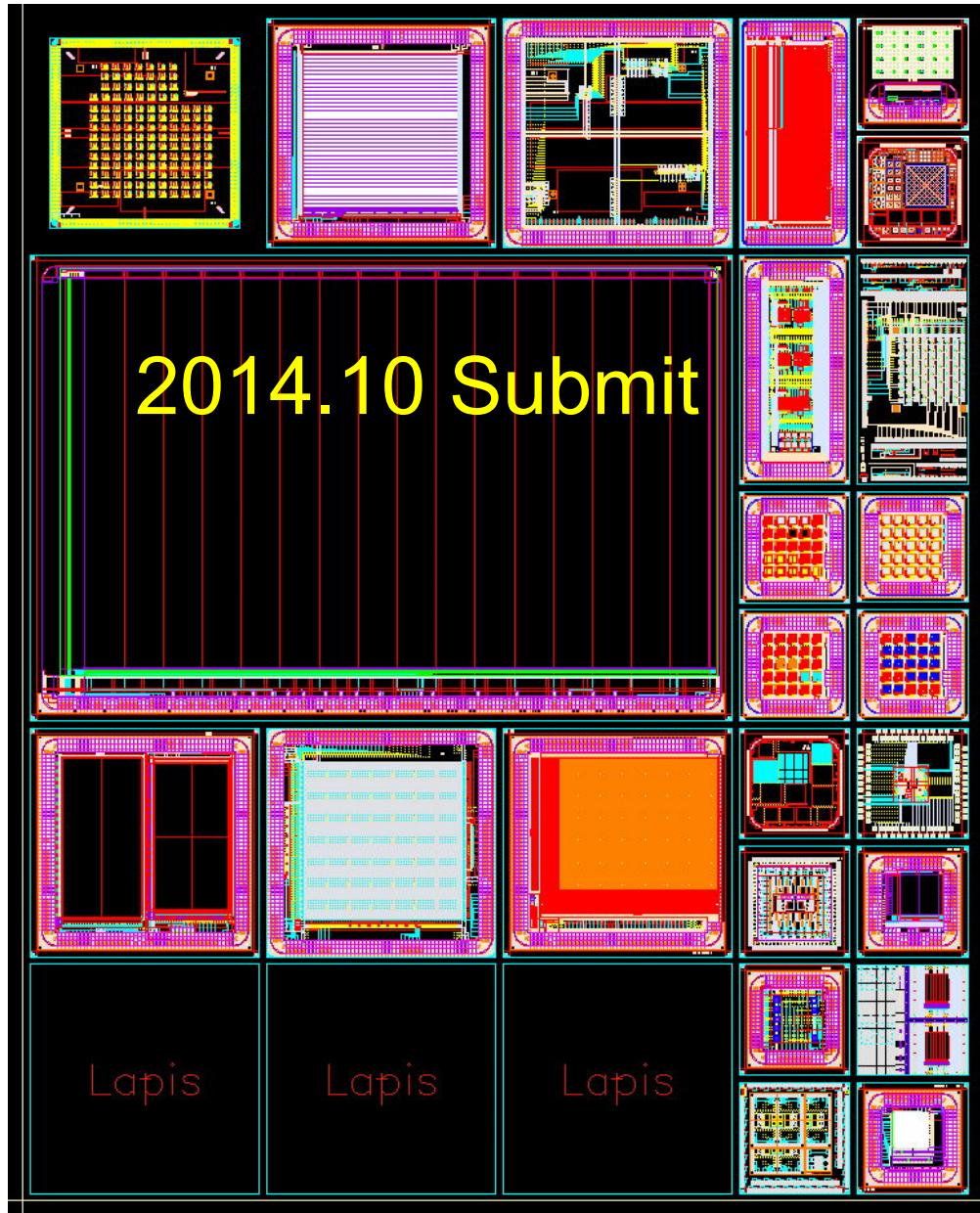
- Sensor : INTPIX4 FZn, Backside Illumination
- HV : 200V, Integration Time : 1ms, ScanTime : 320ns/pix, 1000frame/event
- KEK PF, X-ray Energy : 9.5keV
- Took images for 0° ~ 180° at every 1 degree.

INTPIX4: Computed Tomography with Syncrotron X-ray



3mm

Multi-Project Wafer (MPW) run.
(1~2 runs/year)

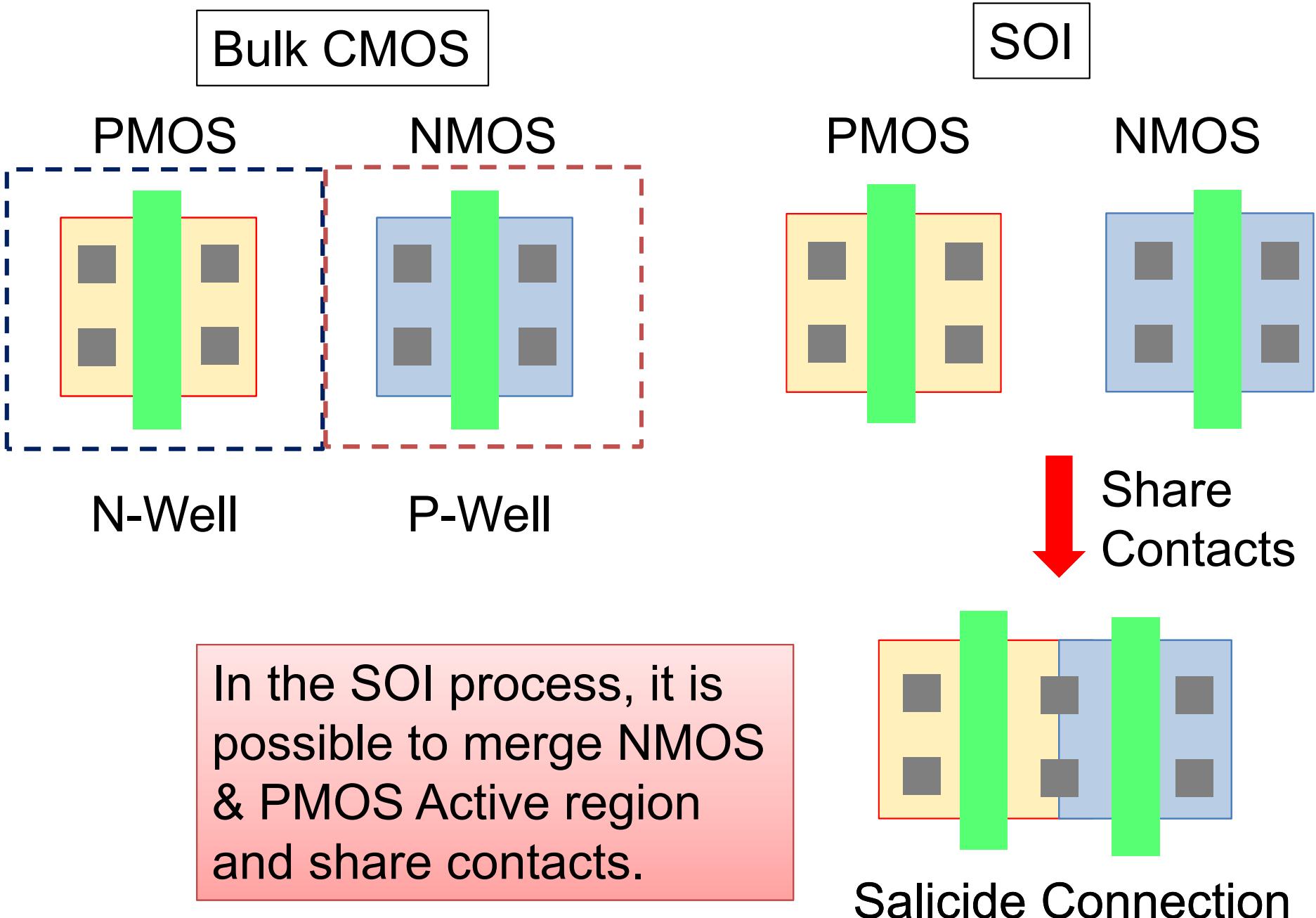


~25 Designes/Mask

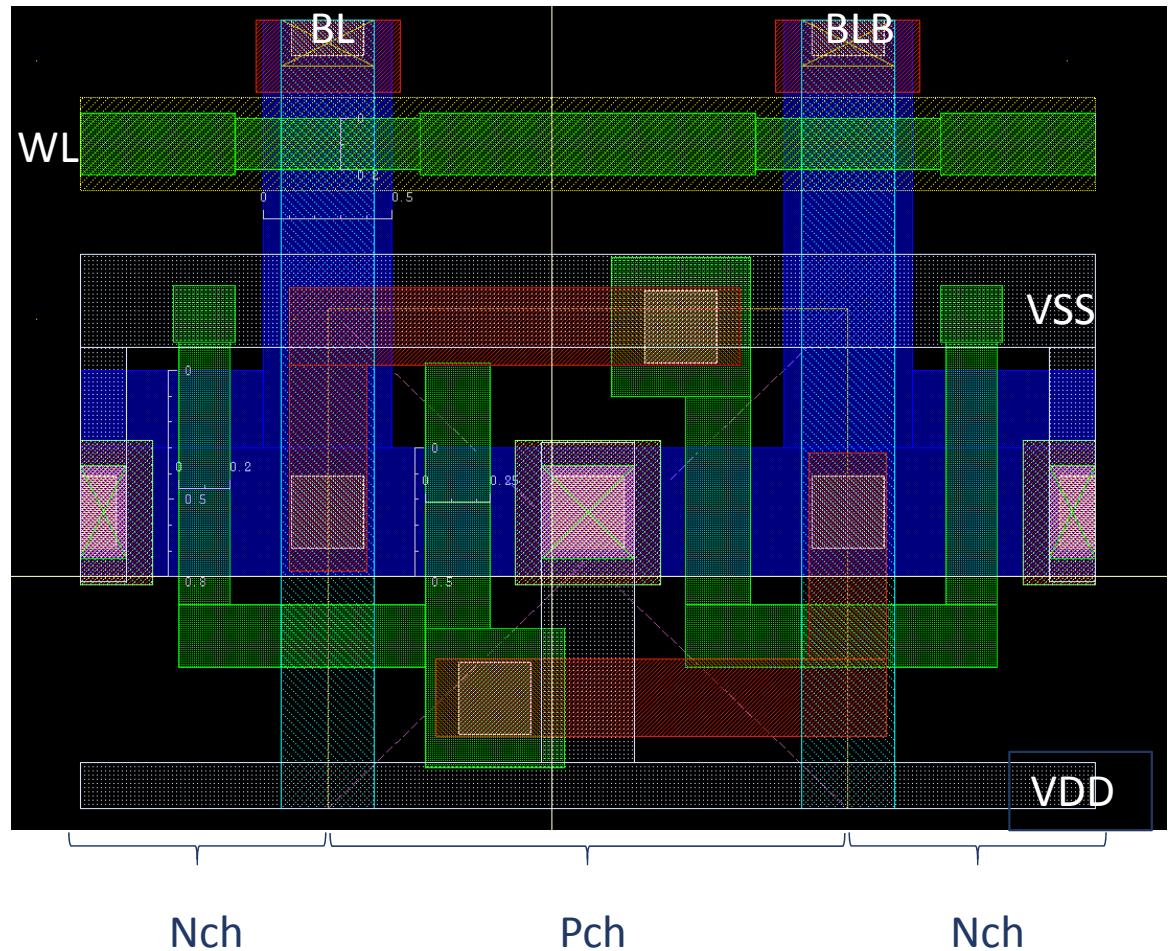
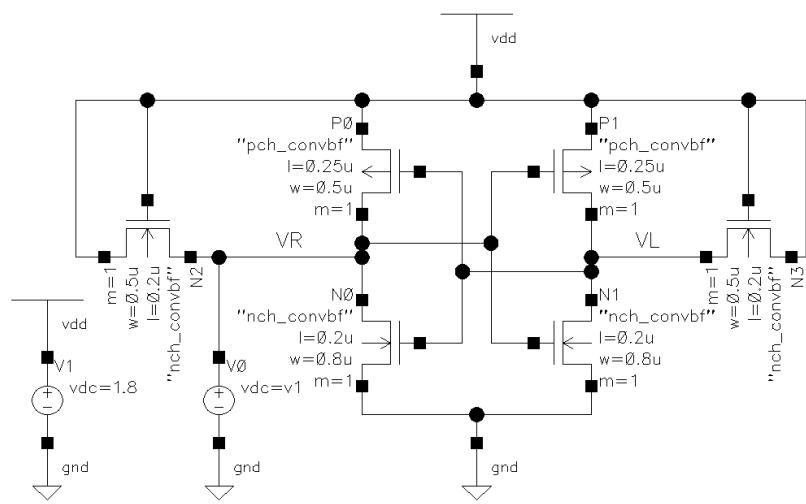
II. Recent Progress

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- *Double SOI Wafer & Process**
- *Higher Dose LDD**
- *Compensation with Tunneling**

Layout Shrink (Active Merge)

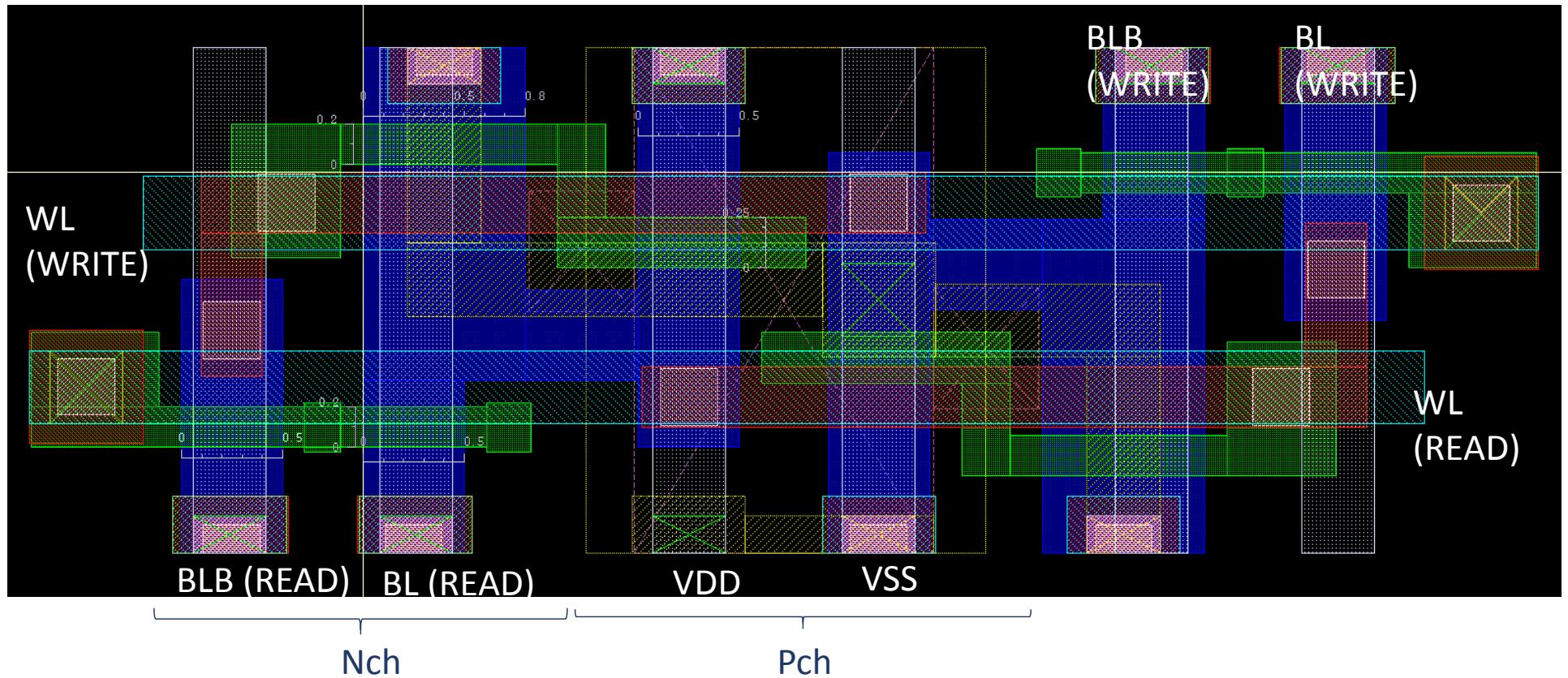


Single Port SRAM Bit Cell



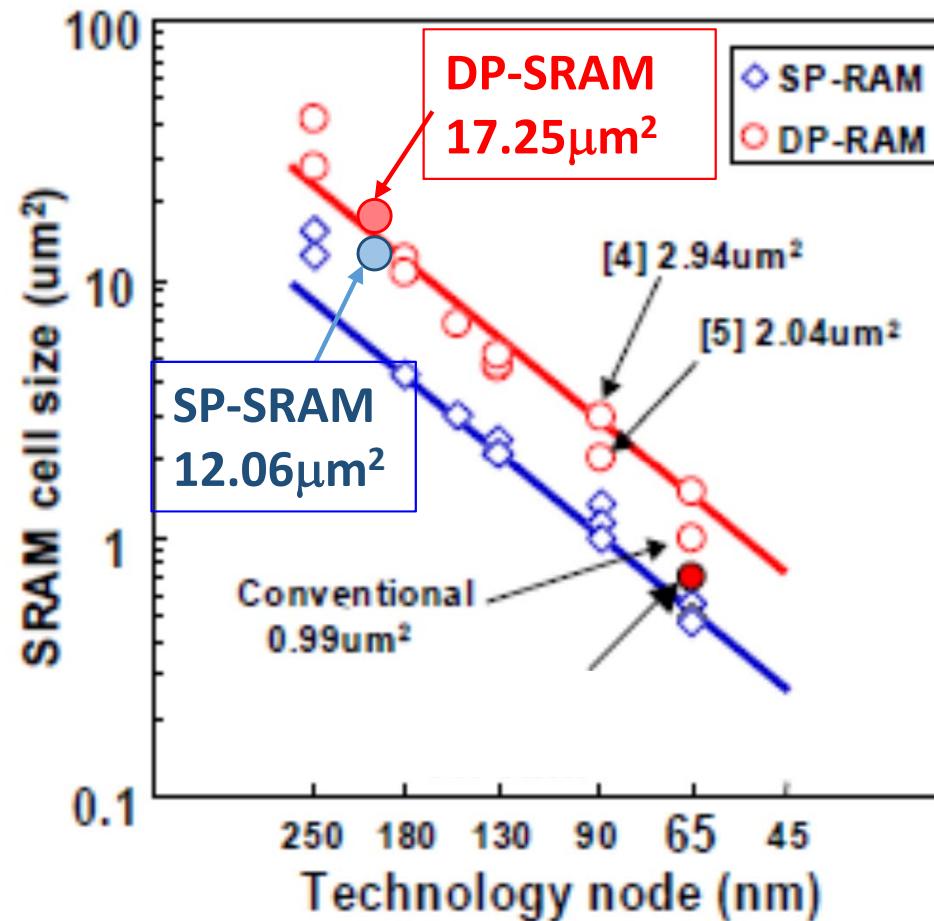
Cell Size : $3.94\mu\text{m} \times 3.06\mu\text{m} = 12.06\mu\text{m}^2$

Dual Port SRAM Bit Cell



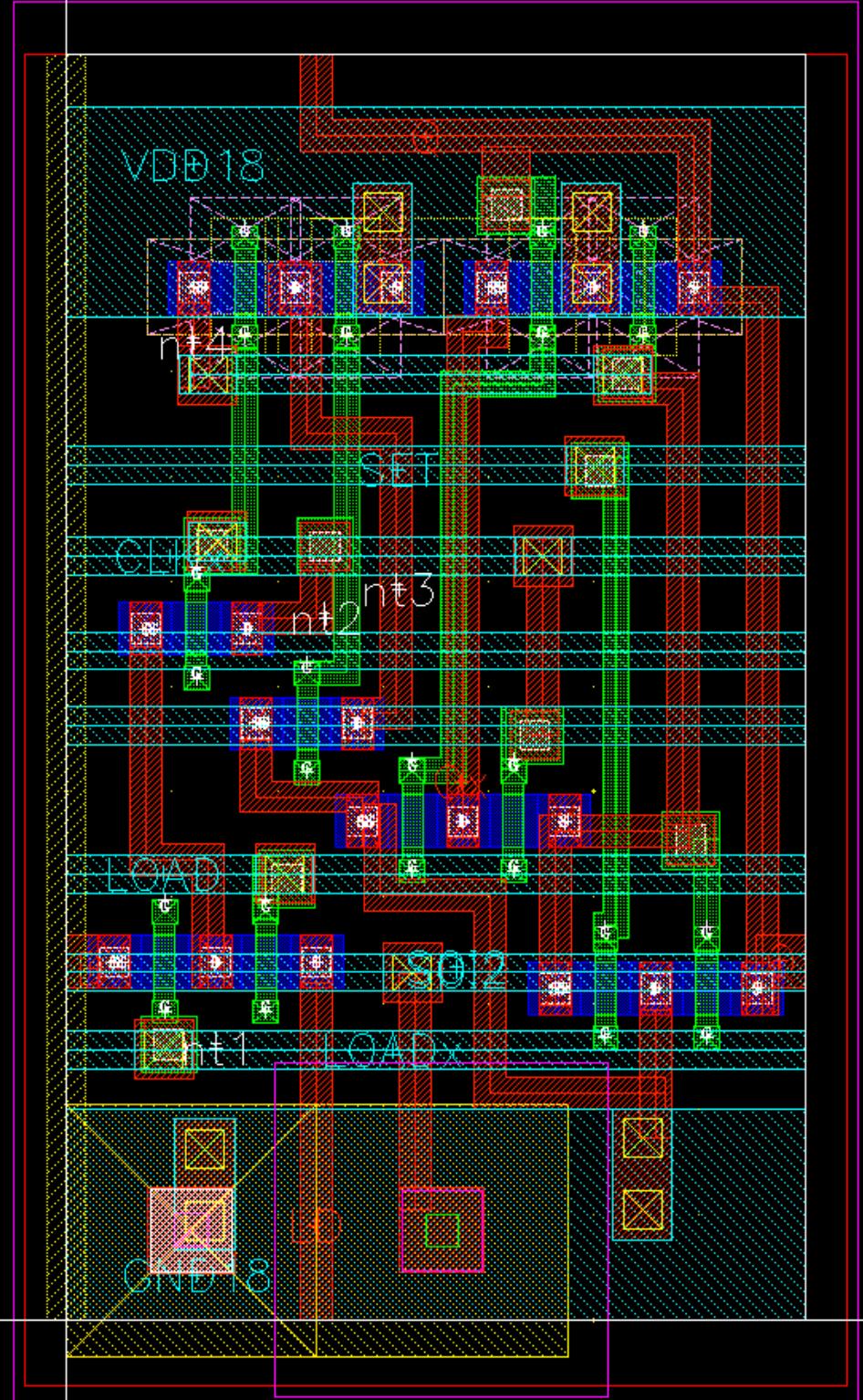
Cell Size : $6.90\mu\text{m} \times 2.50\mu\text{m} = 17.25\mu\text{m}^2$

SRAM Cell Size Comparison



K. Nii, et al., Symp. VLSI Circuit Digst., PP. 130-131, 2006

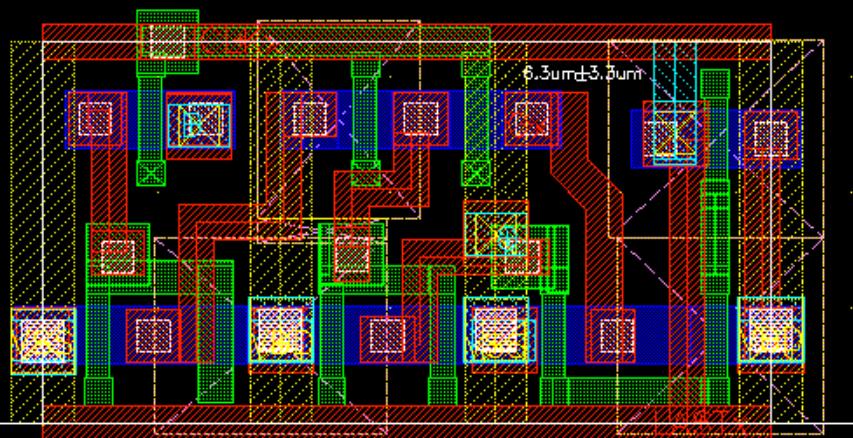
Cell size of the SP- and the DP-SRAM is almost comparable to that of advanced commercial products.



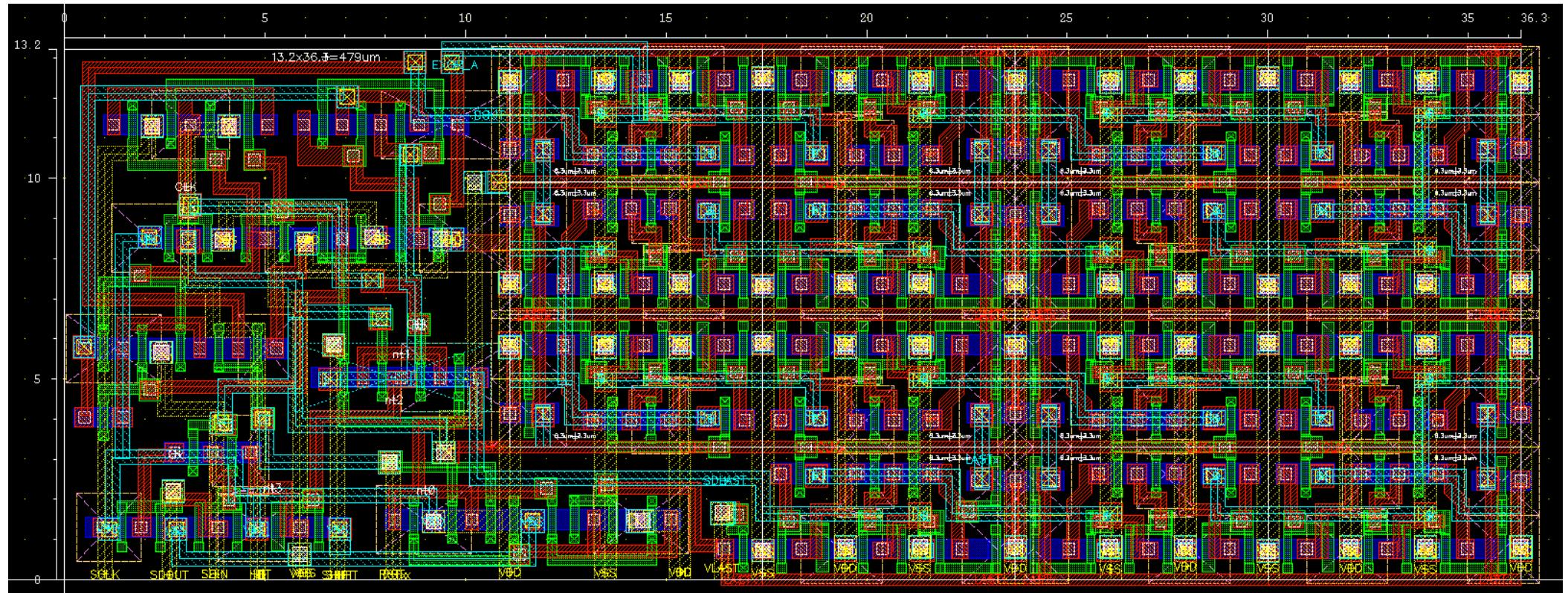
$12 \times 7 = 84 \mu\text{m}^2$

New D Flip-Flop
25% of Previous Cell

$3.3 \times 6.3 = 20.79 \mu\text{m}^2$



15bit Counter + Overflow bit with Serial I/O



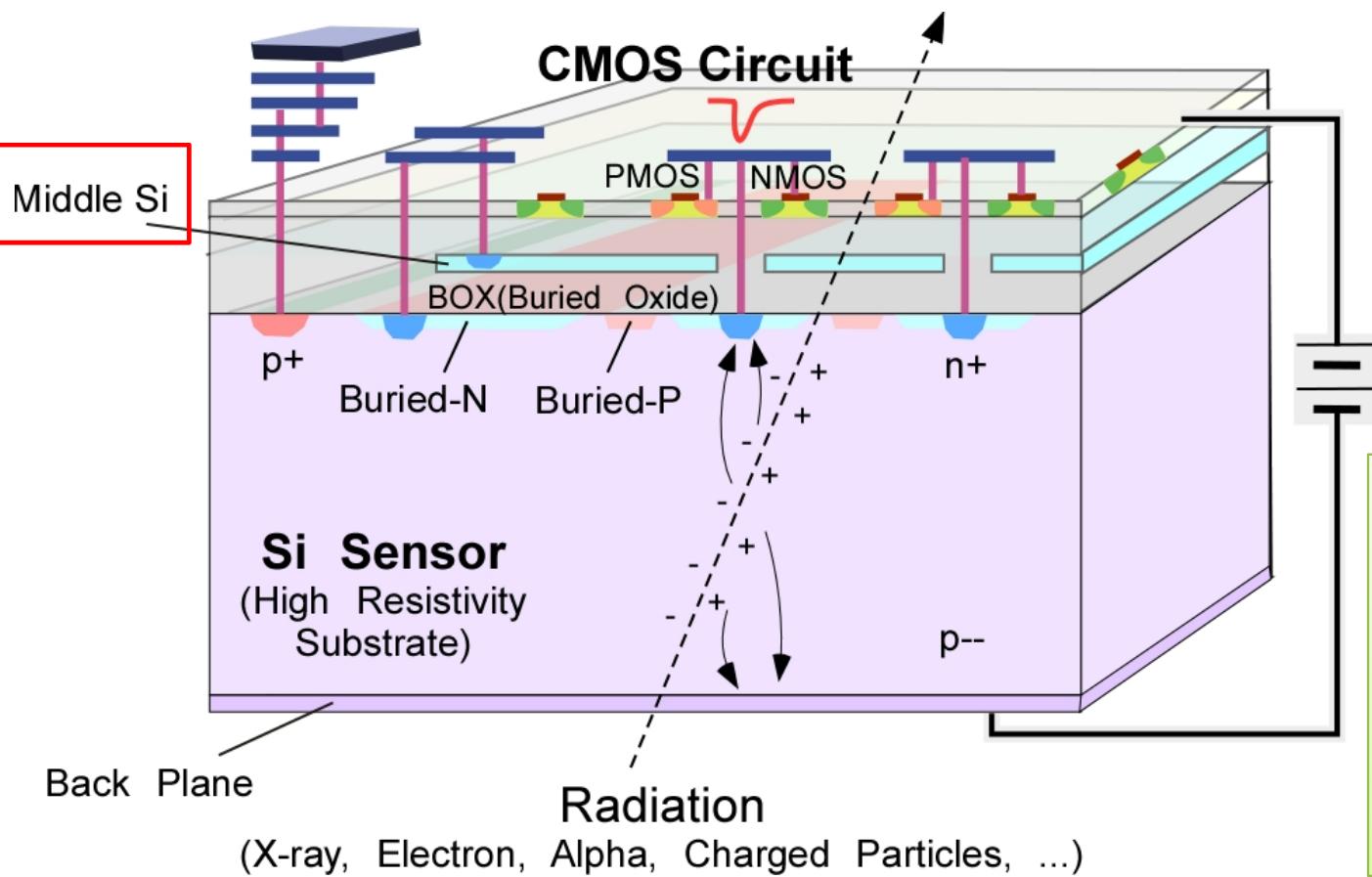
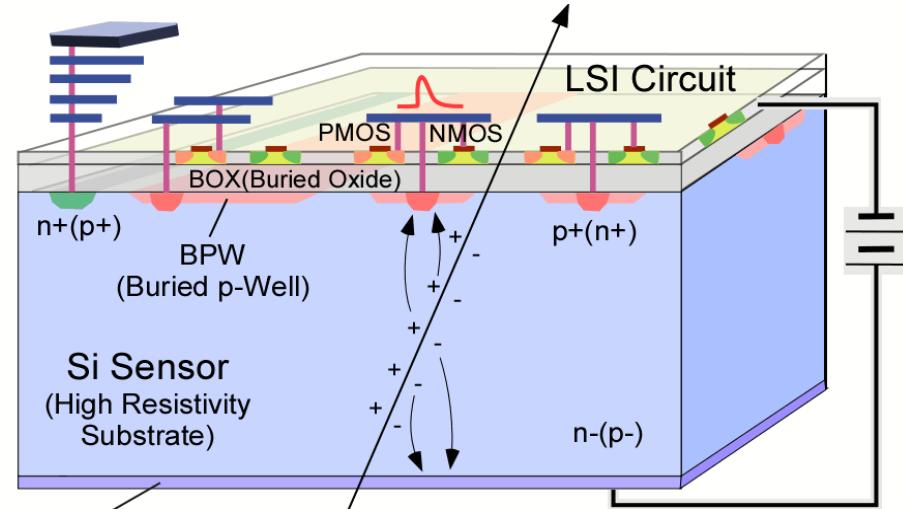
$$13.2\mu\text{m} \times 36.3 = 479 \mu\text{m}^2$$

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Single to Double SOI

Double SOI

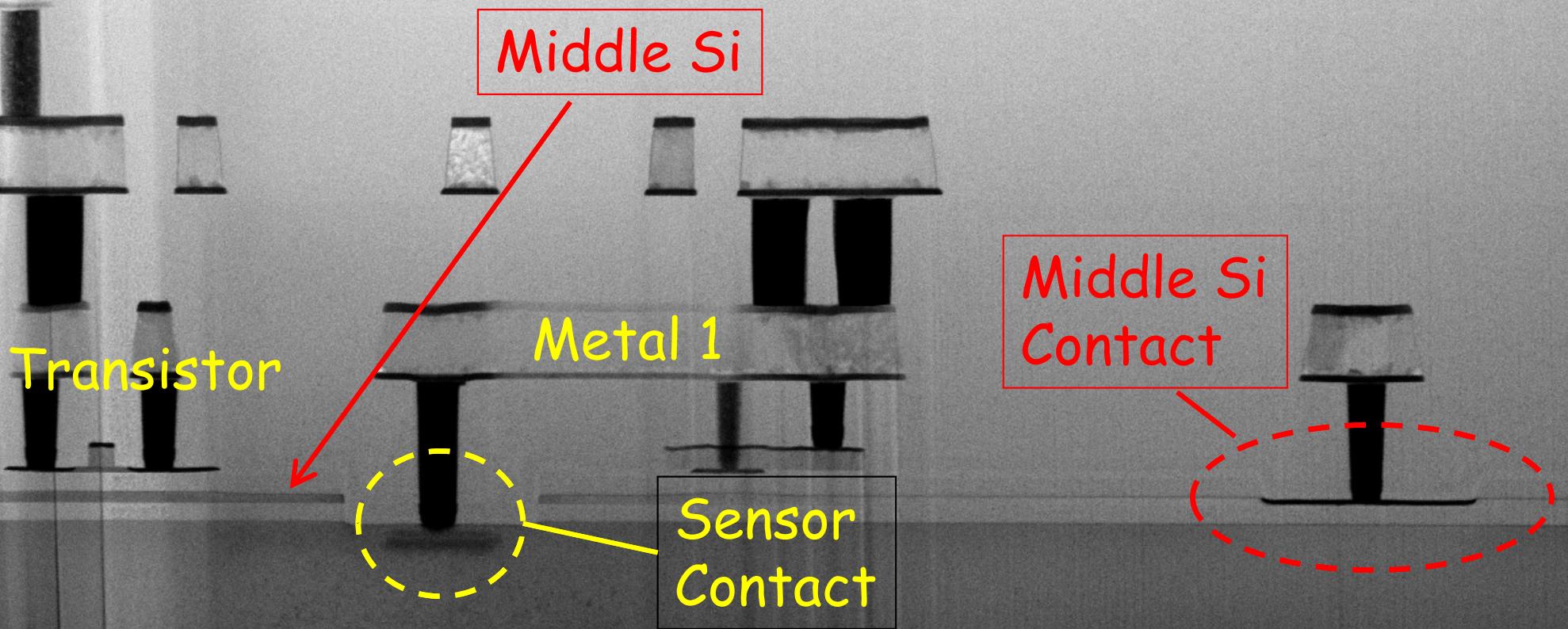


Single SOI

- Shield Sensor–Circuit Interference
- Compensate radiation induced oxide trap charge

Metal 5

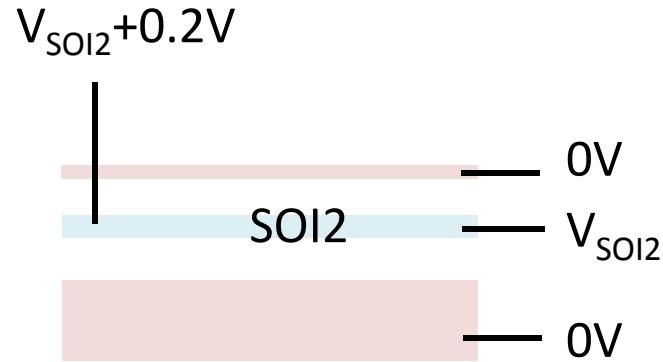
Cross section of the Double SOI Pixel



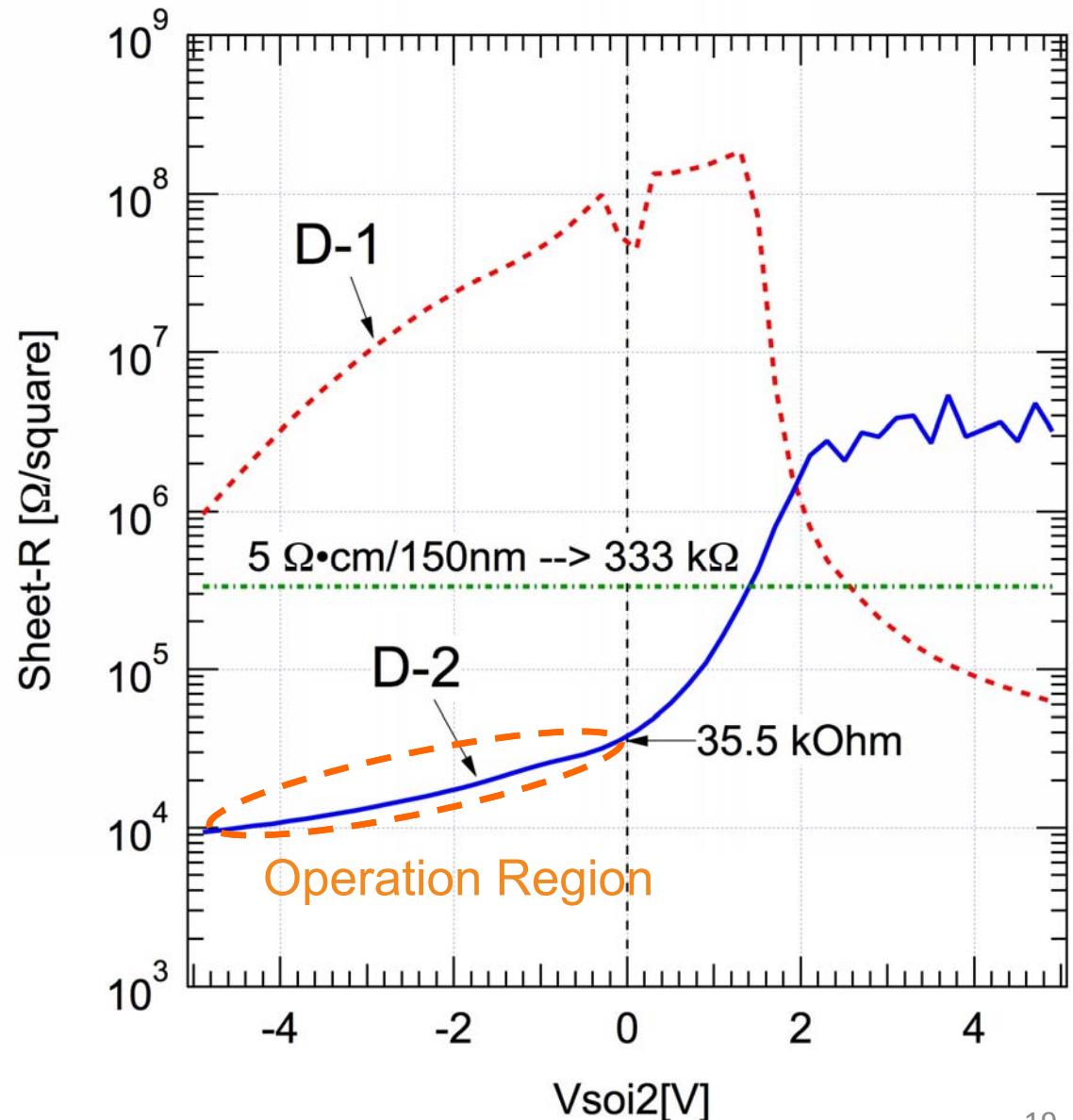
Structure of 2 kinds of Double SOI wafer

Layer	D-1	D-2
SOI1	p-type 88 nm, $<10 \Omega \cdot \text{cm}$	p-type 88 nm, $<10 \Omega \cdot \text{cm}$
BOX1	145 nm	145 nm
SOI2	p-type 88 nm, $<10 \Omega \cdot \text{cm}$	n-type 150 nm, $<10 \Omega \cdot \text{cm}$
BOX2	145 nm	145 nm
Substrate	n-type CZ, 725um, $>700 \Omega \cdot \text{cm}$	p-type Low Oxygen CZ, 725um, $>1.0 \text{ k} \Omega \cdot \text{cm}$

Sheet Resistance of the Middle Si (SOI2)

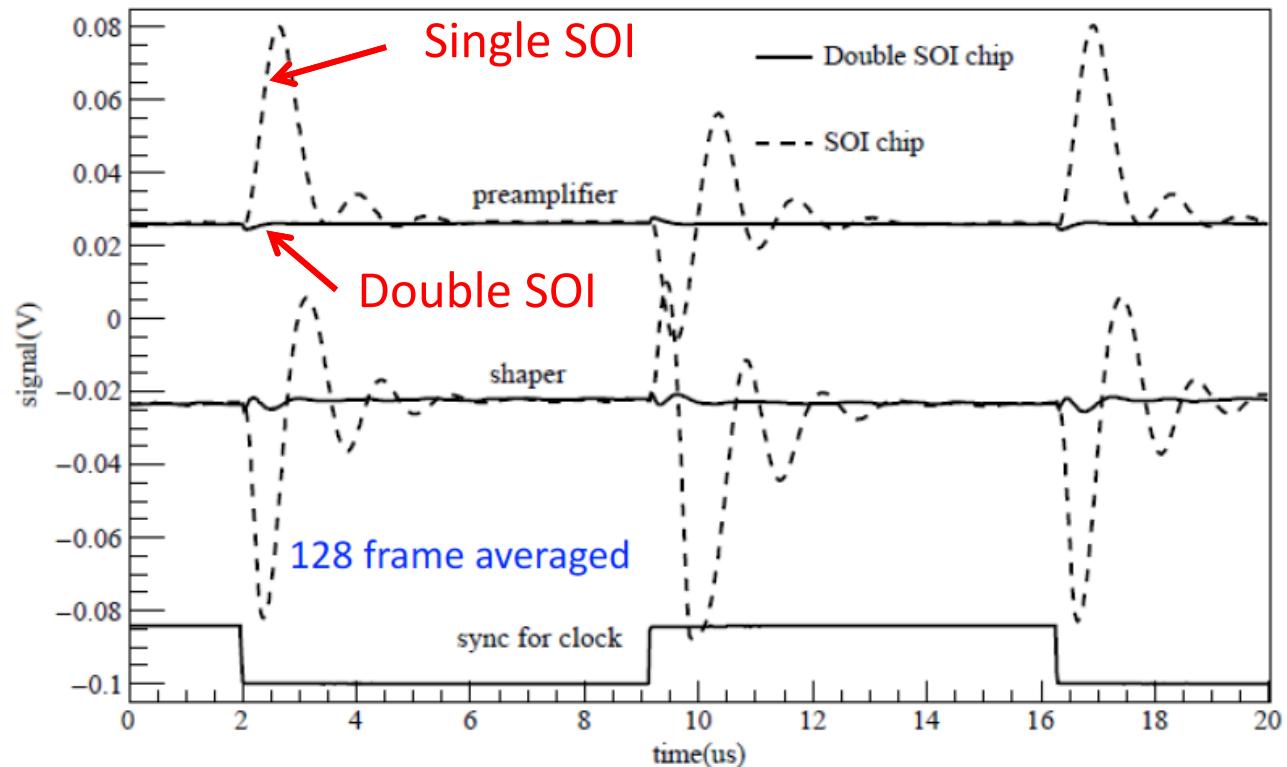


Sheet resistance of the middle Si changes depend on its potential.
D-2 wafer has lower resistance in operation region.



- Crosstalk from counter
 - 5mV @ shaper output for DSOI (74 e⁻ referred to input charge), negligible when superimposed with noise (ENC ~ 113e⁻)
 - 95mV for normal SOI (note the gain of shaper reduced)
 - **Compelling proof of shielding effectiveness**

By using Double SOI wafer, Cross Talk between Circuit and Sensor is reduced to 1/20.



	Double-SOI	Normal SOI
Preamp output(peak to peak)	3.7mV	60mV
Shaper output(peak to peak)	5mV	100mV

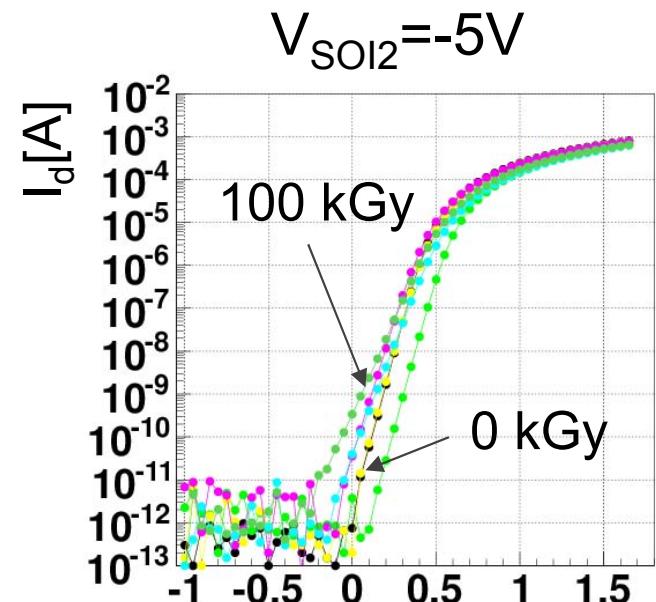
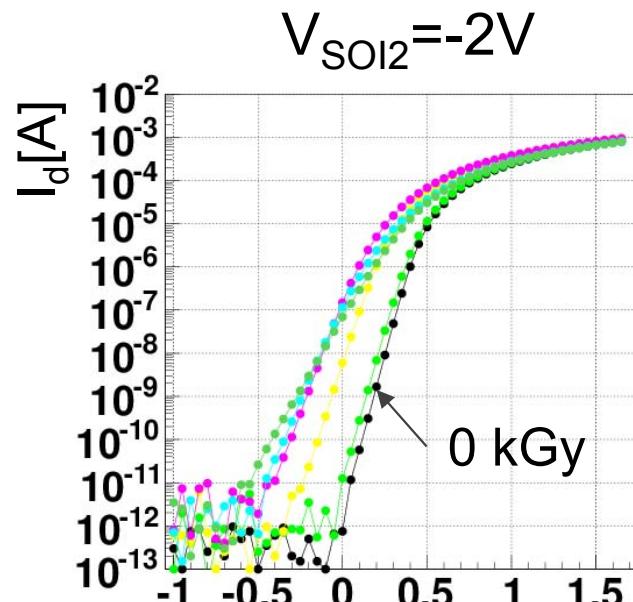
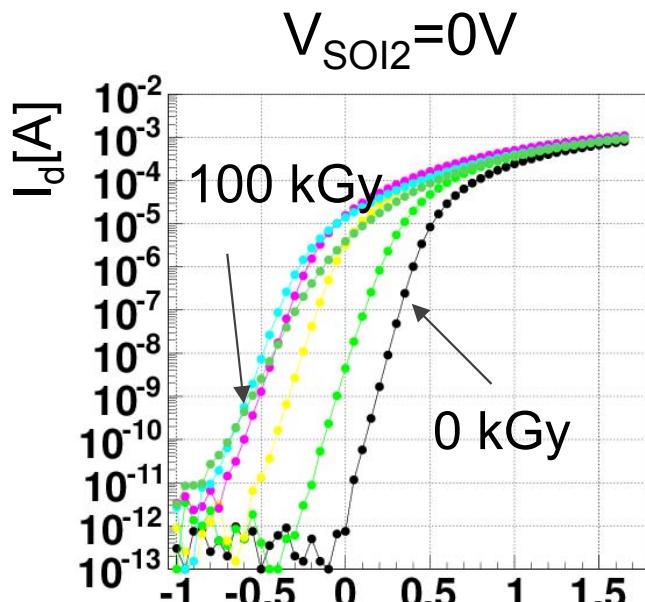
(by Lu Yunpeng (IHEP))

SOIPIX2015, June 2-6, 2015, Sendai

Gamma-ray Irradiation Test

(Id-Vg Characteristics v.s. SOI2 Potential)

NMOS



- 0kGy
- 0.5kGy
- 1kGy
- 2kGy
- 5kGy
- 10kGy
- 20kGy
- 100kGy

By setting $V_{SOI2} \sim -5V$, Id-Vg curve returned
nearly to pre-irradiation value at 100 kGy(Si)

(by U. of Tsukuba)

I/O normal Vth
Source-Tie Tr.
 $L/W = 0.35\mu m/5\mu m$

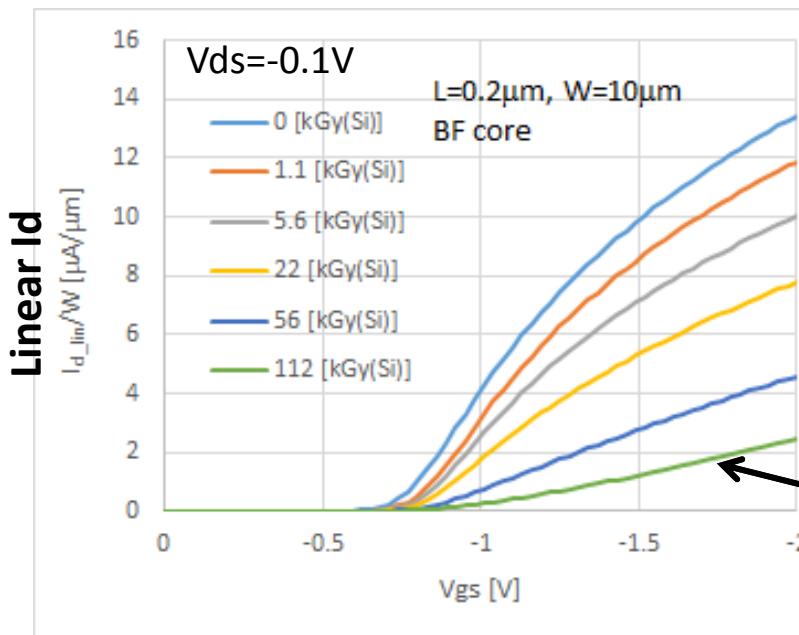
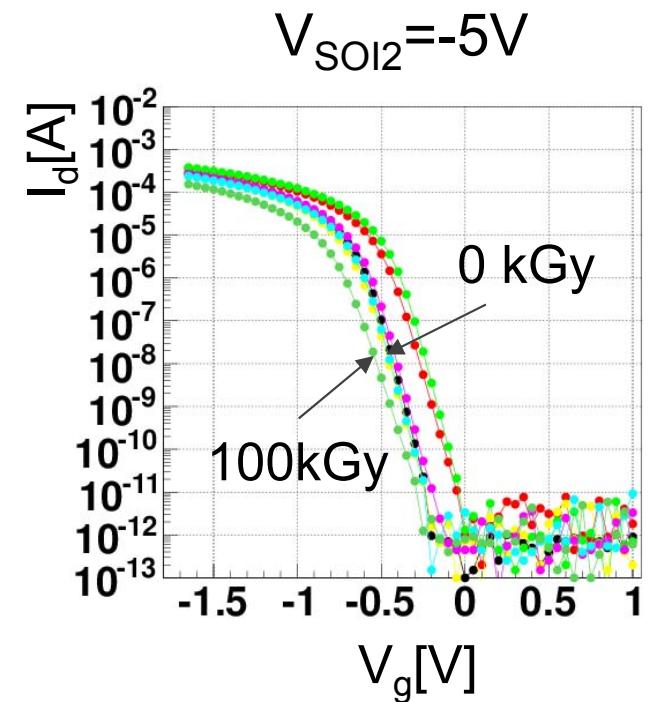
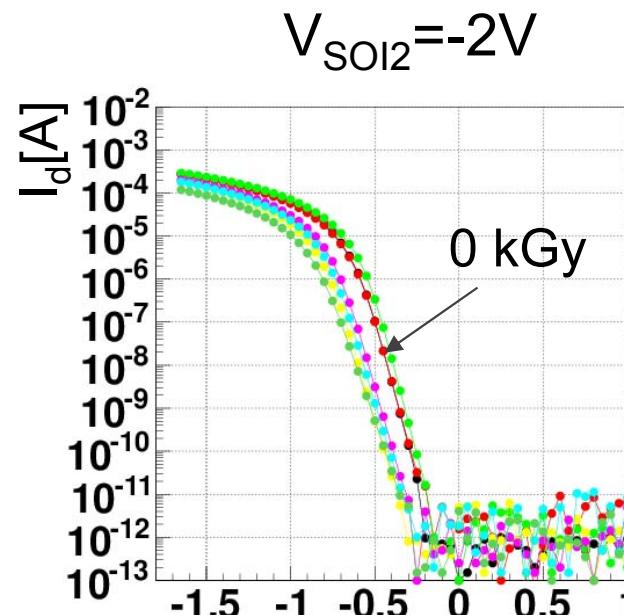
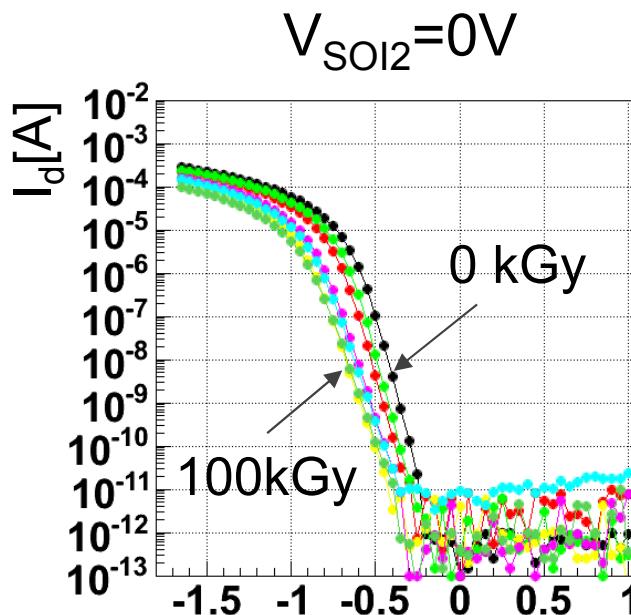
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Variation of Id-Vg Characteristics and Effect of SOI2 Potential

PMOS

I/O Normal Vt
Source-Tie
L/W = 0.35um/5um



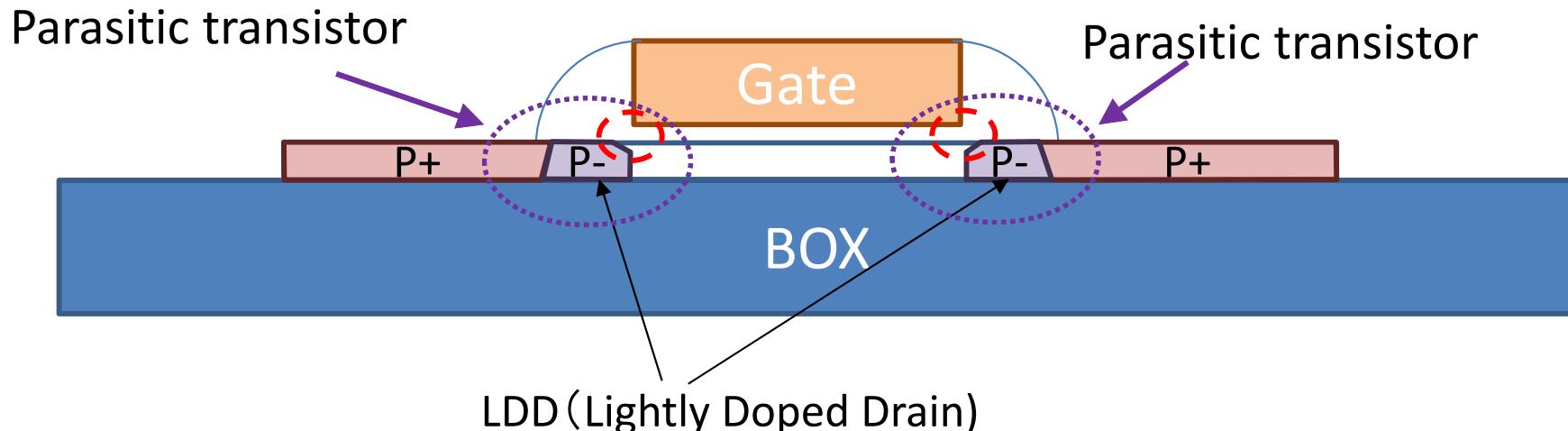
-80%

112 kGy

Threshold voltage shift is not so large in PMOS, but Drain Current decreases much .

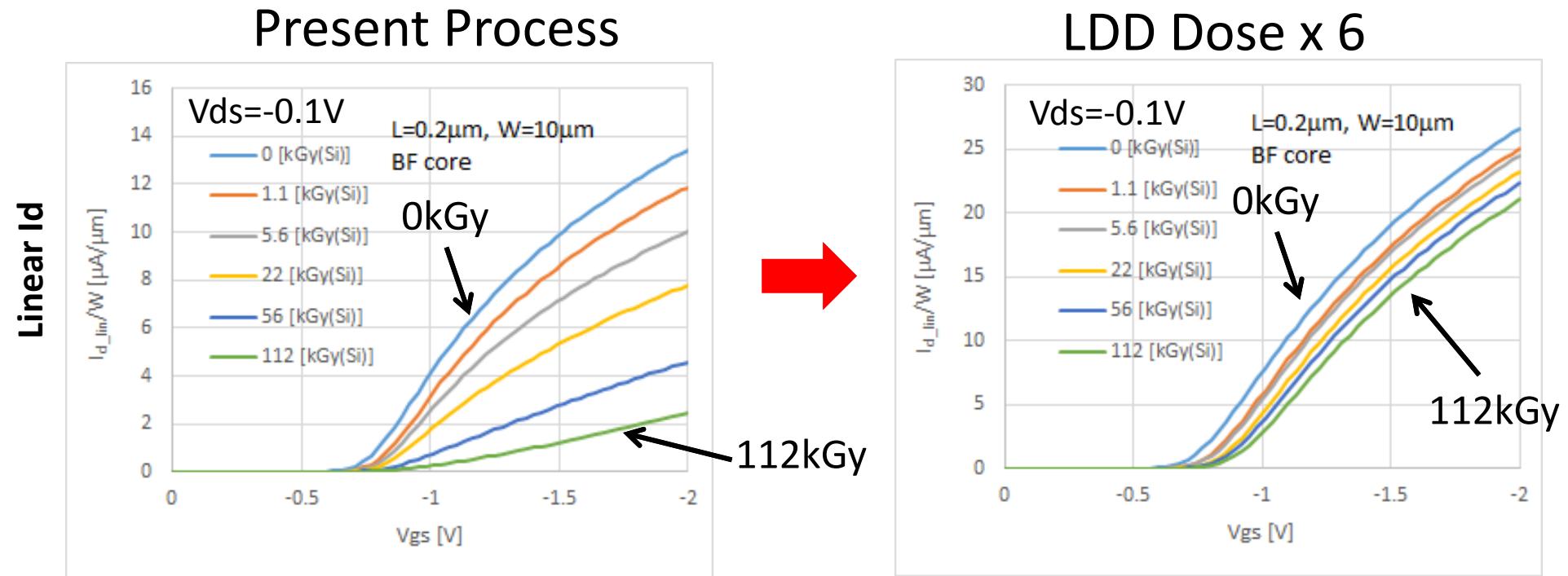
Dose Increase in Lightly Doped Drain (LDD) Region

- Major cause of the drain current degradation by radiation is V_t increase at gate edge due to positive charge generation in spacer.
- Charge in spacer control the V_t of the parasitic transistor.
- To reduce this effect, lightly doped drain (LDD) dose should be increased.
- Present process has rather low dose in LDD region to aiming lower power.



(by I. Kurachi)

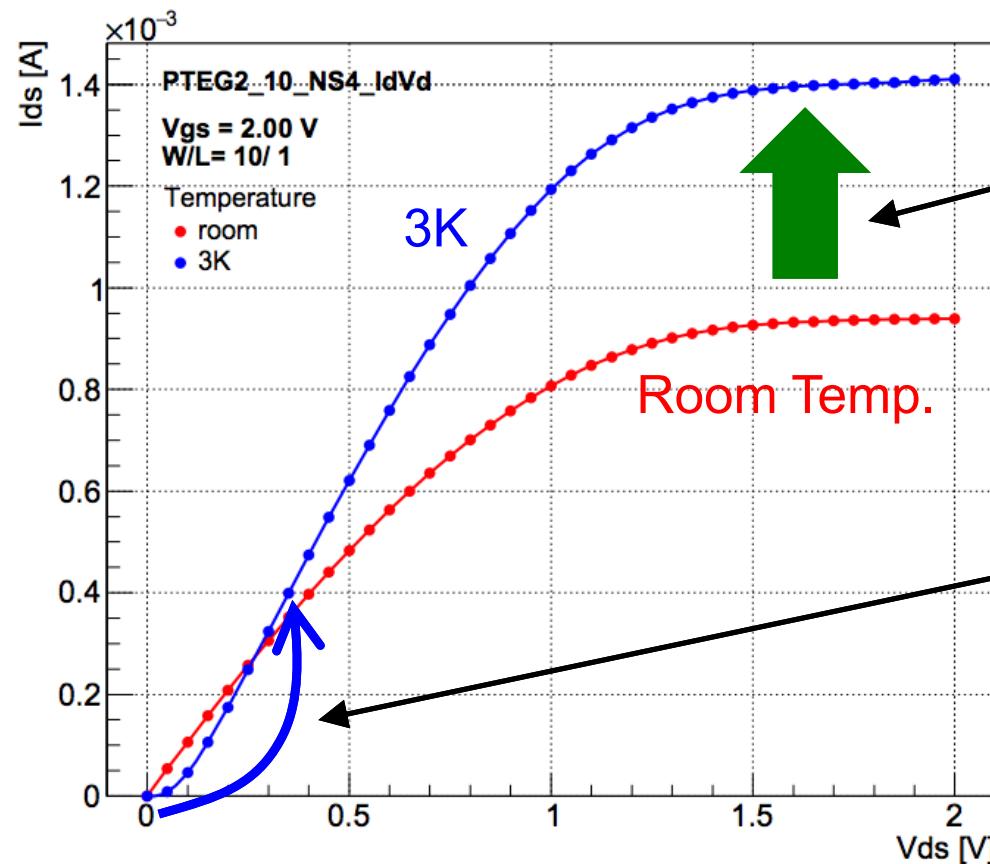
Id-Vg Characteristics in Triode Region



With increasing Implantation dose of PLDD region 6 times higher than present value, the degradation is reduced from 80% to 20% at 112 krad(Si).

Ultra-Low Temperature Operation

One of the feature in SOI transistor is operation capability in ultra-low temperature.

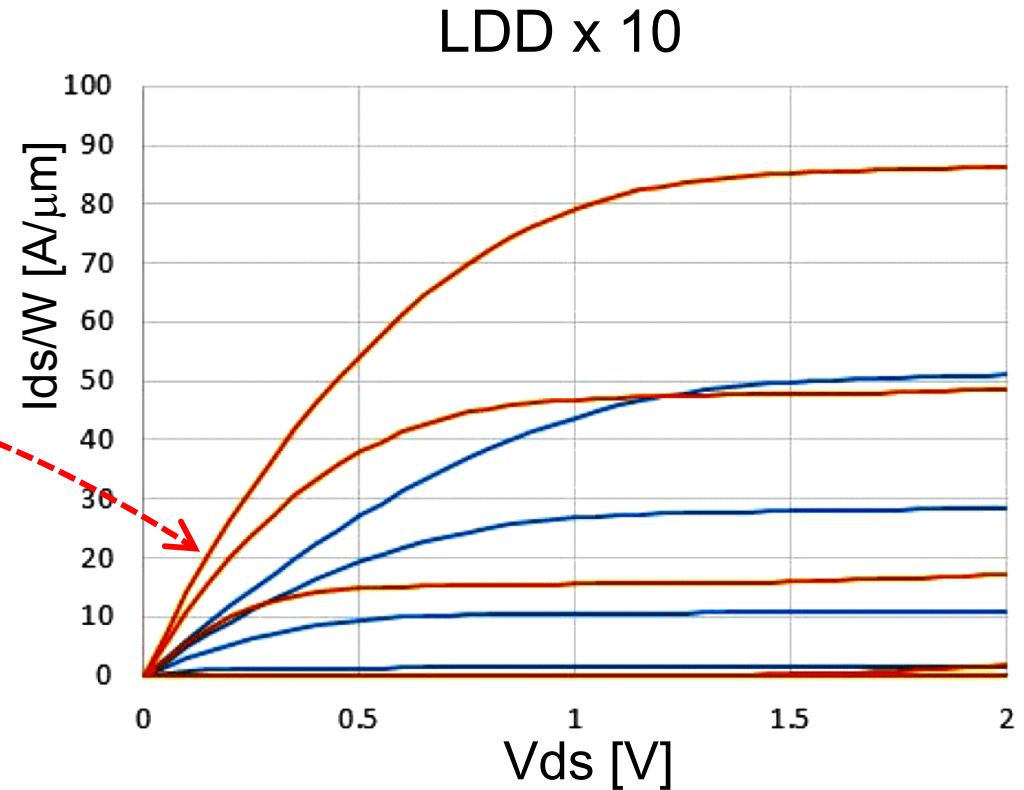
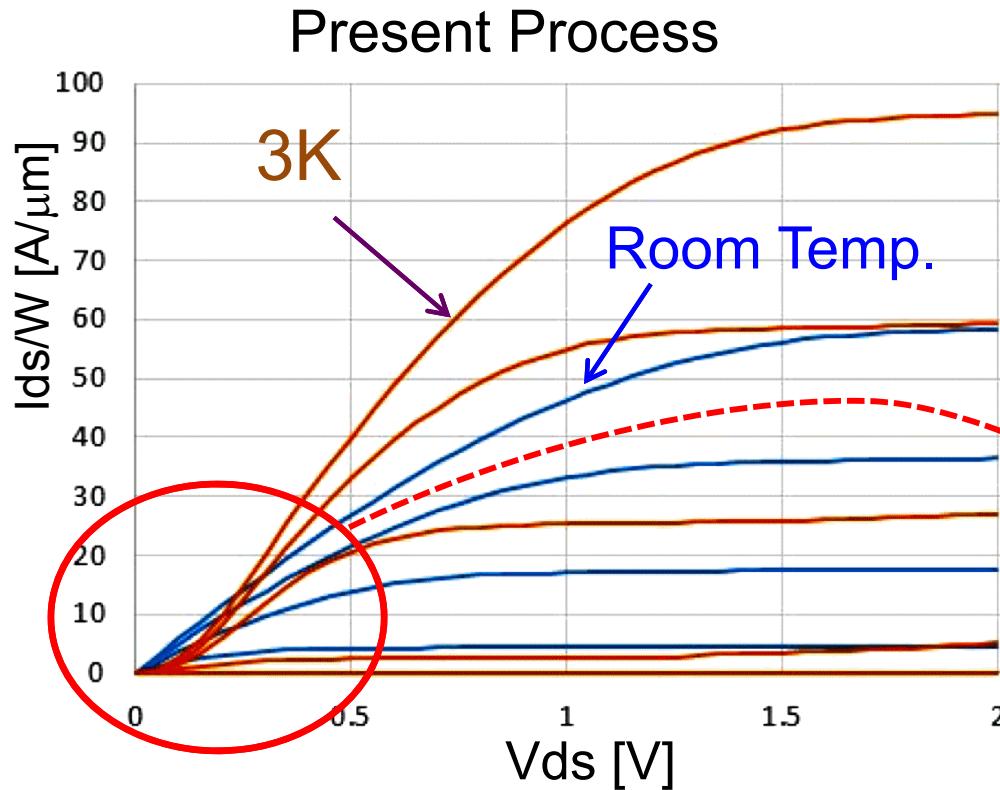


Drain Current Increase due to increase of carrier mobility

Slow rise in low V_{ds} region!

Improvement in Ultra-Low Temperature

Pch Transistor
Source-Tie type 2
 $L=1\mu m$, $W=10\mu m$

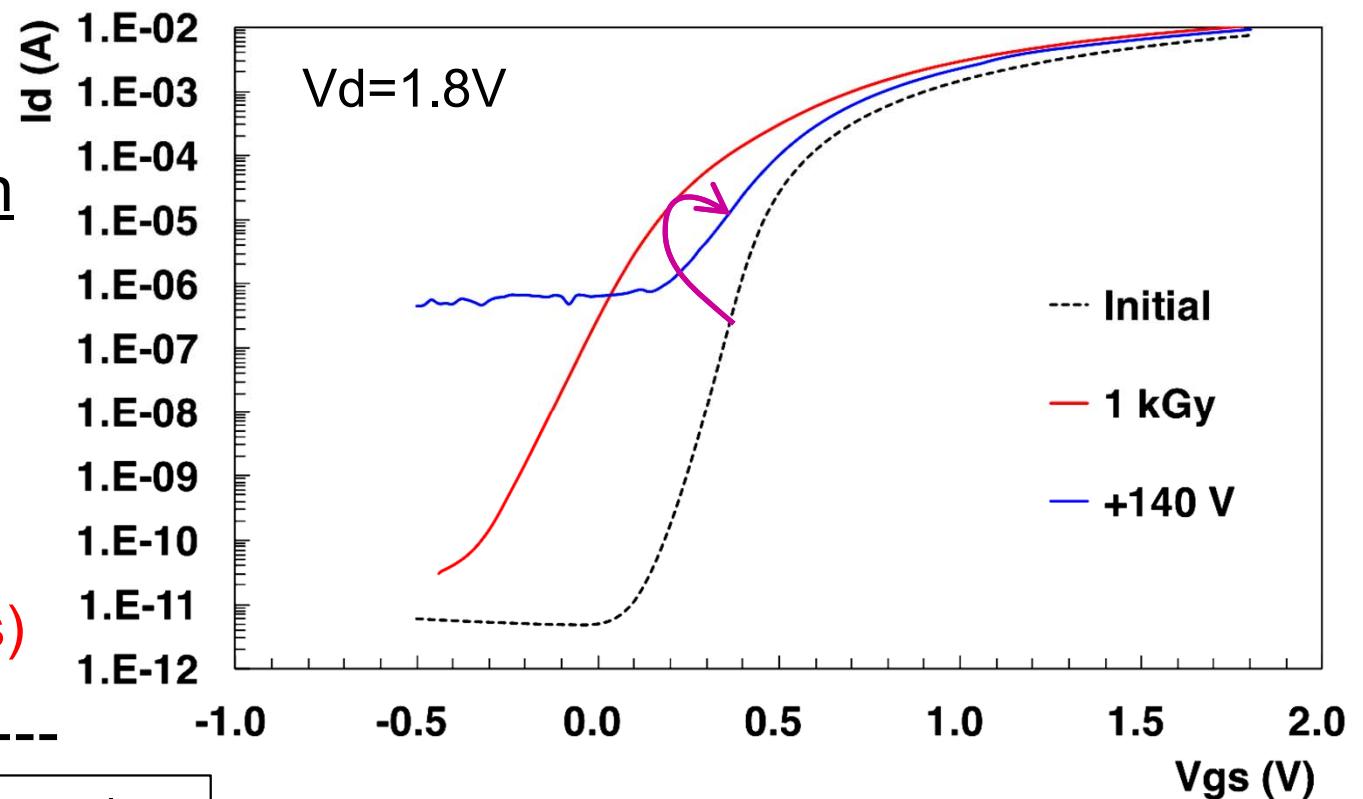
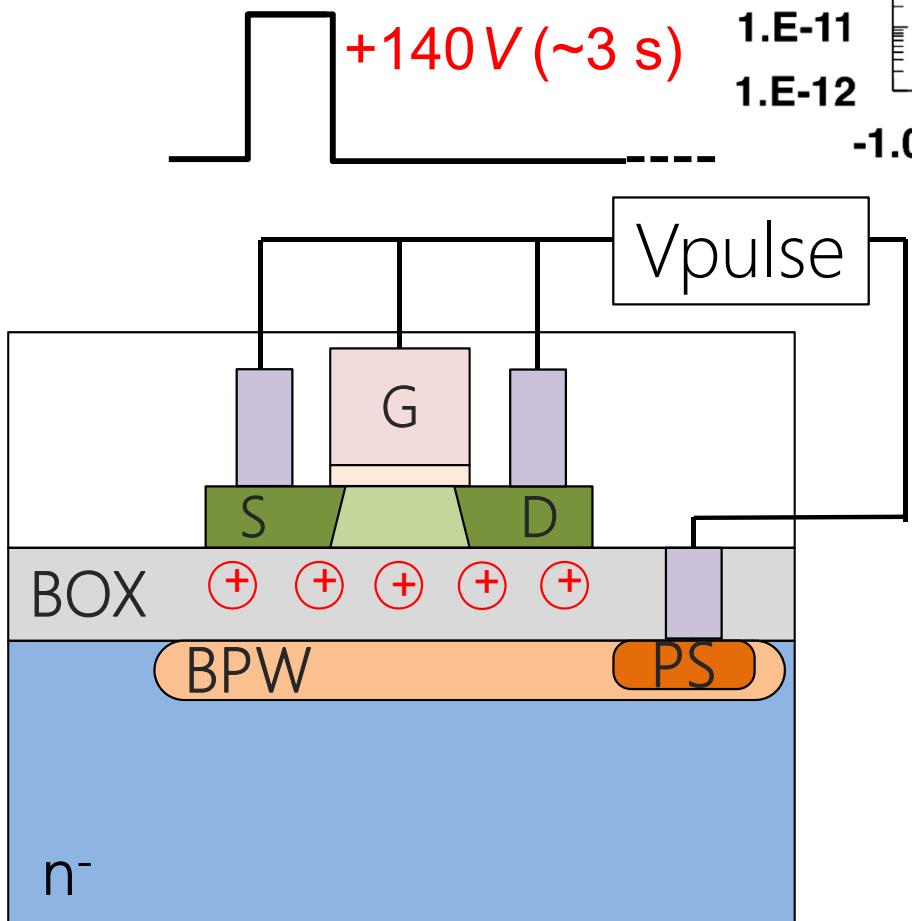


By increasing the LDD dose 6~10 times, characteristic of the transistors becomes smooth in Ultra-Low Temperature.

II. Recent Progress

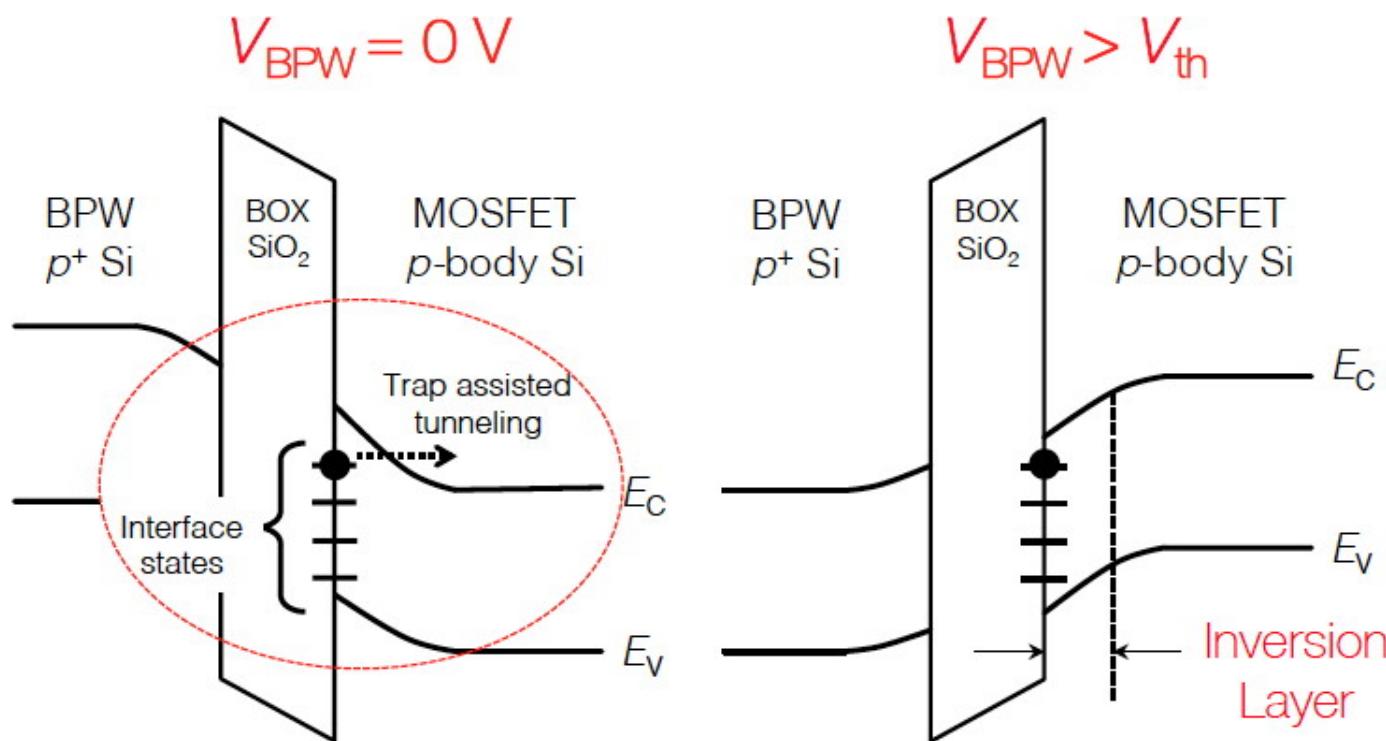
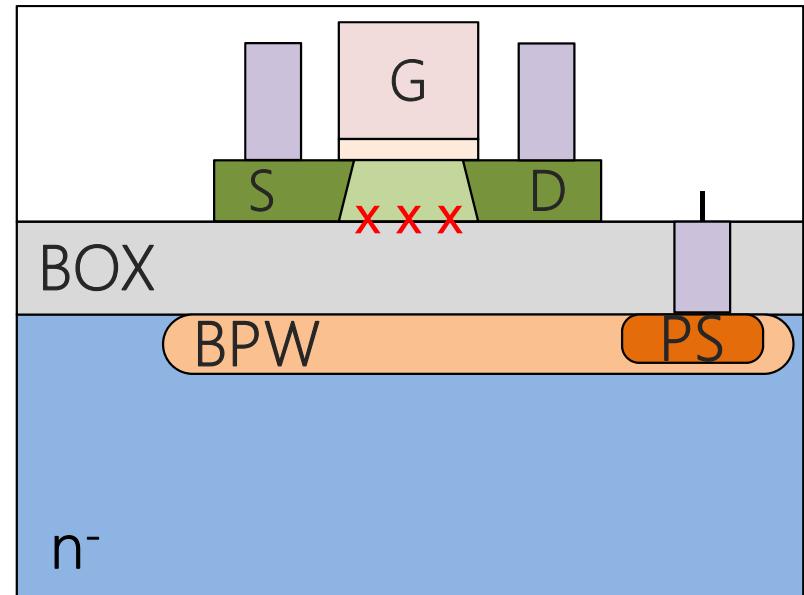
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HV Impulse Application

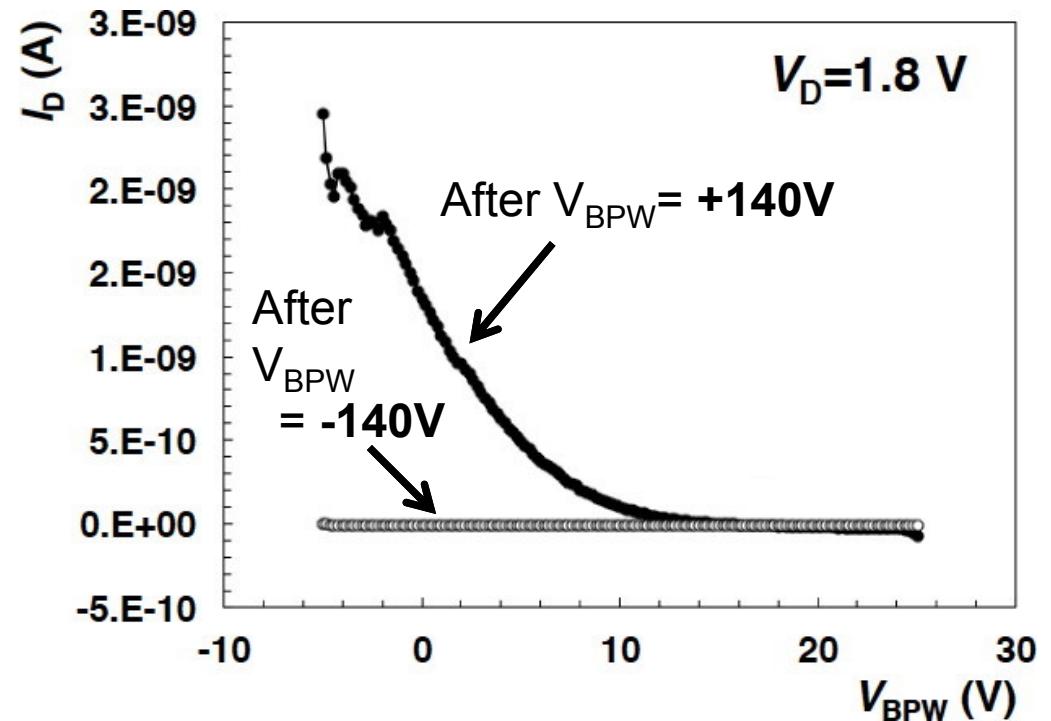
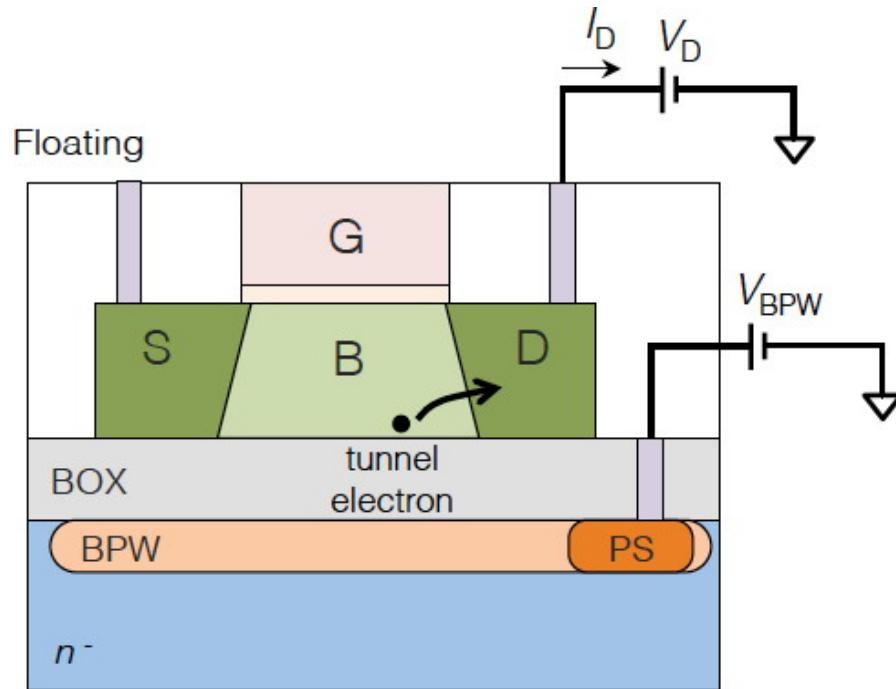


Threshold shift with radiation is recovered by applying a HV pulse to under-layer (SOI2 or BPW) of transistor.
However, Leakage current was increased.

We assumed the origin of the leakage current is **Trap Assisted Tunneling**.
 If so, the leakage current should disappear when an inversion layer is generated at the bottom of the transistor.

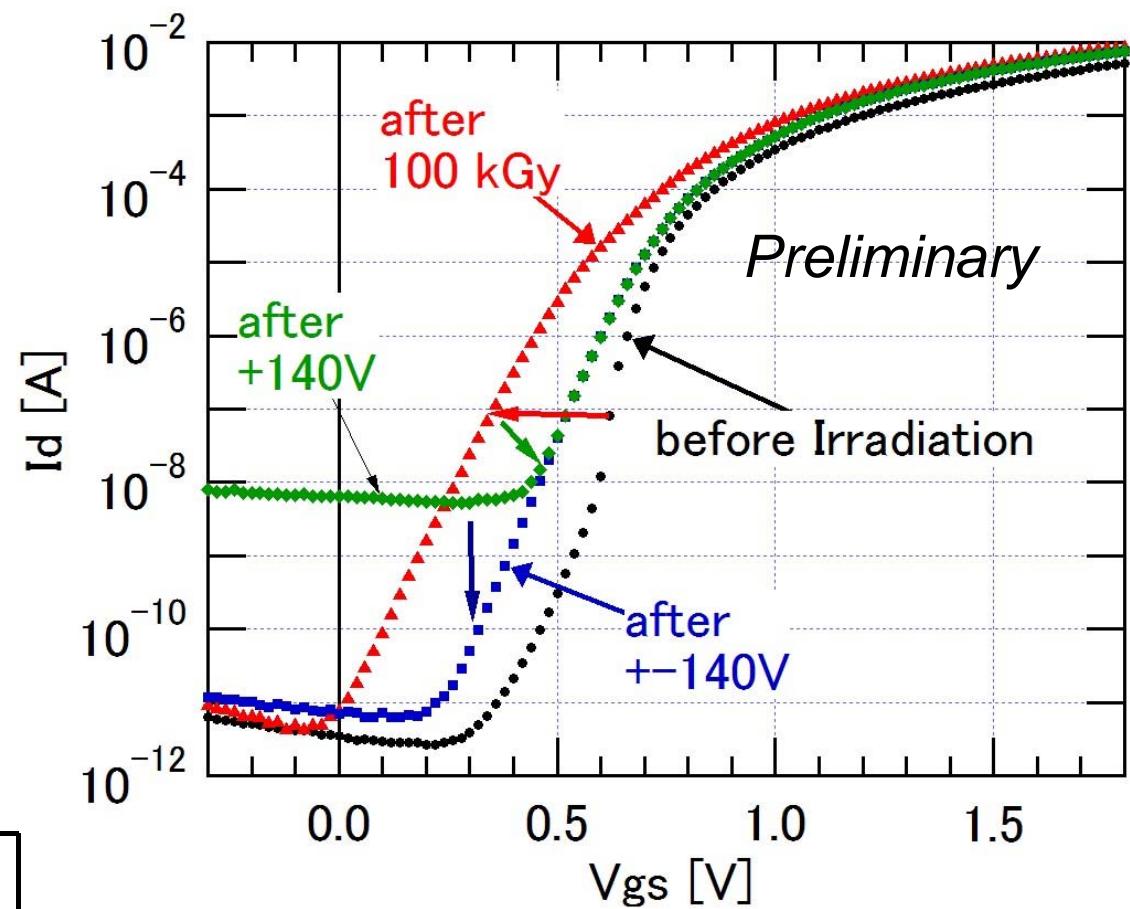
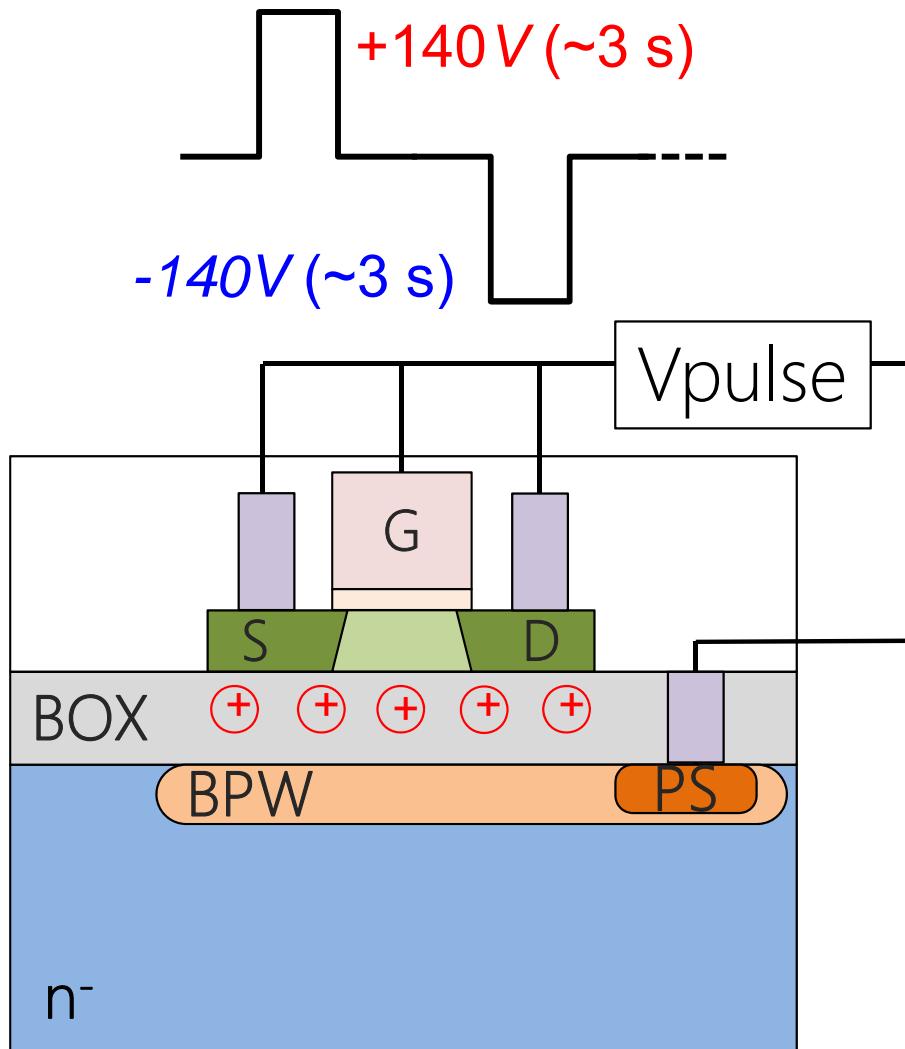


Confirmation of the Trap Assisted Tunneling



After generating an inversion layer at the bottom of the transistor by applying negative pulse to the BPW layer, drain current become insensitive to the back gate (BPW) voltage.

Removing Radiation Induced Oxide Charge with FN Tunneling



Radiation damage is recovered by applying Plus-Minus HV pulses to under-layer of transistor.

Summary of Solutions in SOI pixel detector

	Back Gate Effect	Sensor Circuit Interference	Vt Shift by radiation	Un-isotropic damage by radiation	Id degradation by radiation	Id slow rise @Low Temp.
Buried Well	○	X	△	△	-	-
Nested Well	○	△	△	△	-	-
Double SOI	○	○	○	△	-	-
Higher LDD Dose	-	-	-	-	○	○
FN Tunneling	-	-	○	○	-	-

III. Summary

- We have been developing SOI pixel process/detectors, and operating MPW runs.
- NMOS-PMOS active merge reduces layout size very much. This is almost equivalent to go to finer process while keeping good analog properties of 0.2um process.
- Double SOI reduces interference between sensor and circuit very efficiently.
- Radiation tolerance is improved to more than 100 kGy by biasing middle Si of the DSOI and increasing the dose of LDD region.
- Radiation induced oxide trapped charge can be compensated with HV pulsing in under-layer of transistors.