Contribution ID: **301** Type: **Talk**

Improved Process Technologies in the SOI Pixel Detectors

Thursday 18 February 2016 16:55 (20 minutes)

A monolithic detector using Silicon-On-Insulator (SOI) technology is one of promising technologies for future pixel detectors in various kinds of applications. It fabricates both sensors and readout circuits in a semiconductor process. It is also known that the technology is immune to Single Event Effect (SEE).
Remaining issues in the SOI pixel technology are radiation tolerance for Total Ionization Dose (TID) and sensor crosstalk from circuit signals. We have solved these issues by introducing double SOI technology and modifying implantation dose of Lightly Doped Drain (LDD) region of transistors.
In the double SOI technology, an additional Si layer is inserted under transistor layer, so it shields the crosstalk. We confirmed the middle Si layer could suppress the crosstalk very efficiently. In addition, by applying bias voltage to the middle layer, it can compensate electric field created by oxide-trapped hole generated by irradiation. Thus the threshold shift caused by radiation can be adjusted to original value even in the device which is irradiated more than 10 Mrad(Si).
However, we observed drain current reduction after heavy irradiation. We found this is caused by parasitic transistors exist in the LDD region of transistors. By increasing the doping level of the LDD region, we confirmed such reduction could be avoided. We also found this doping level change improves Id-Vd characteristics of transistor in ultra-low temperature region (< 3K).

Primary authors: MIYOSHI, Toshinobu (KEK); ARAI, Yasuo (High Energy Accelerator Research Organization (KEK))

Co-authors: Prof. KURACHI, Ikuo (High Energy Accelerator Research Organization (KEK)); HARA, Kazuhiko (University of Tsukuba (JP)); TAUCHI, Kazuya (High Energy Accelerator Research Organization (KEK)); ASANO, Mari (University of Tsukuba (JP)); YAMADA, Miho (High Energy Accelerator Research Organization (KEK)); TOBITA, Naoshi (University of Tsukuba); HAMASAKI, Ryutaro (The Graduate University of Advanced Studies (KEK)); NISHIMURA, Ryutaro (The Graduate University for Advanced Studies (KEK)); HONDA, Shunsuke (University of Tsukuba (JP)); TSUBOYAMA, Toru (High Energy Accelerator Research Organization (KEK)); IKEGAMI, Yoichi (High Energy Accelerator Research Organization (KEK)); FUJITA, Yowichi (High Energy Accelerator Research Organization (KEK))

Presenter: ARAI, Yasuo (High Energy Accelerator Research Organization (KEK))

Session Classification: Semiconductor Detectors

Track Classification: Semiconductor Detectors