14th Vienna Conference on Instrumentation

Wien February 15-19, 2016

Recent Developments in Silicon Detectors

particle

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University of Bonn

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SI LAB
Silizium Labor Bonn

Looking back at 4 years of the LHC (25 /fb + 5 /fb)

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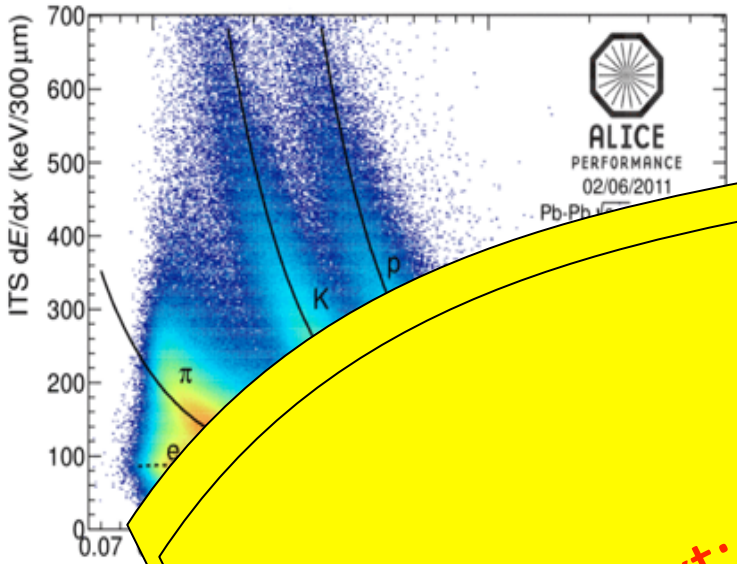
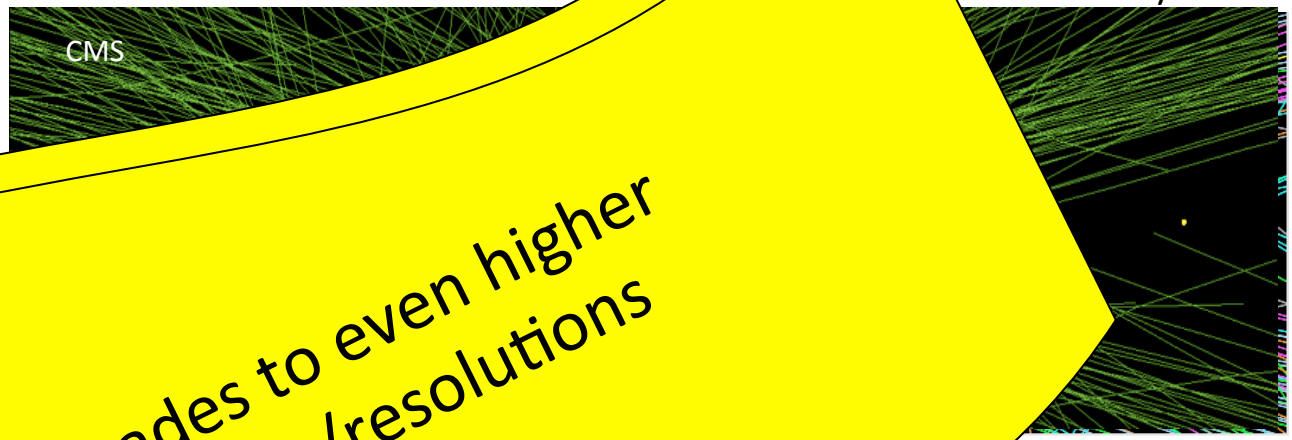
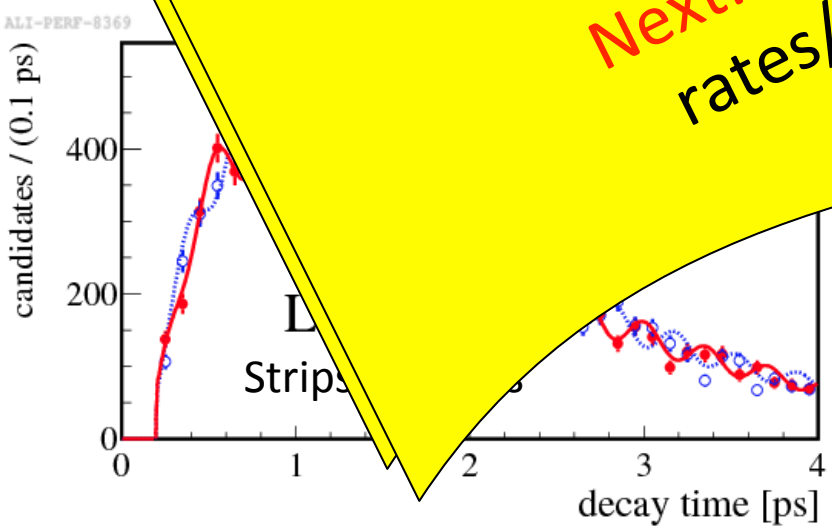
- This is a definitively a success story !

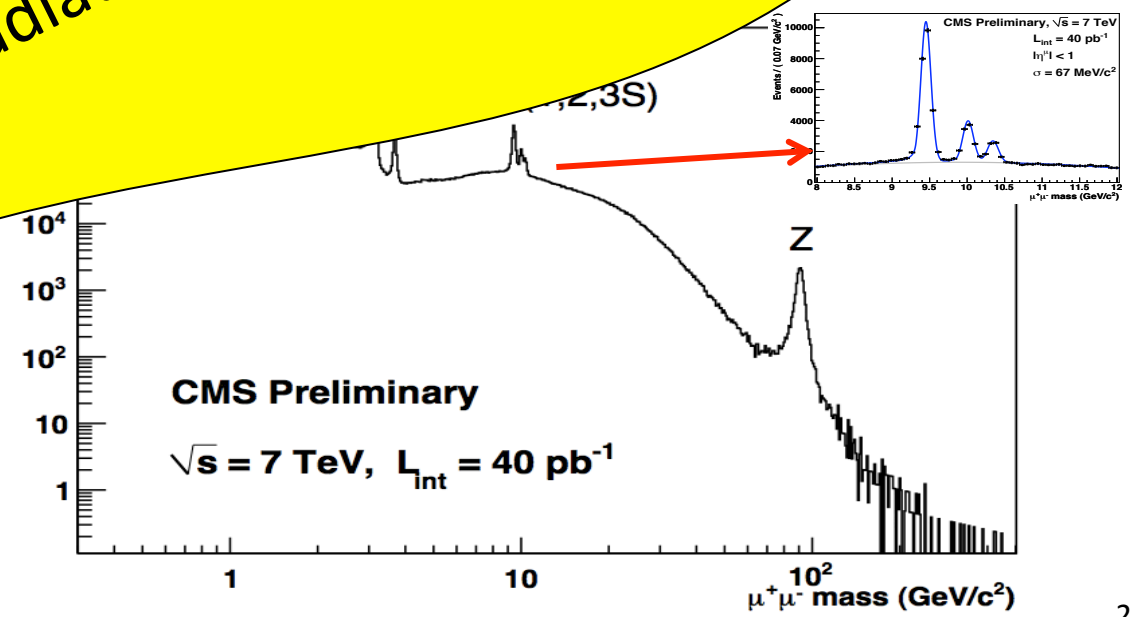




interaction /BX

Next: Upgrades to even higher rates/radiation/resolutions





Huge plans with silicon within HL-LHC Upgrade ...

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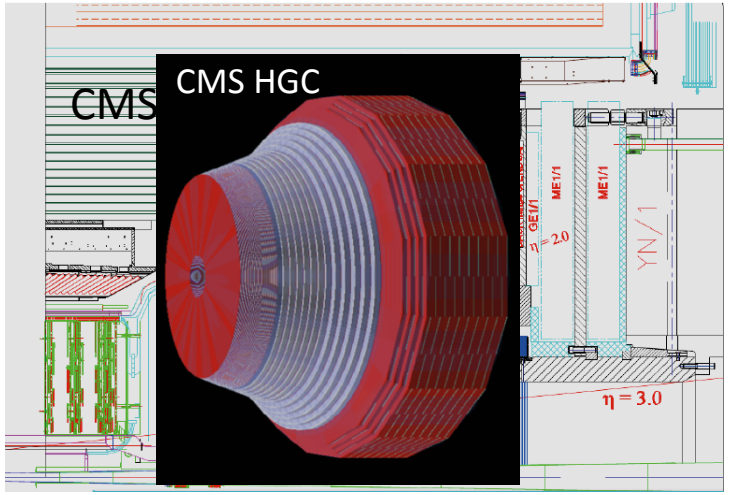
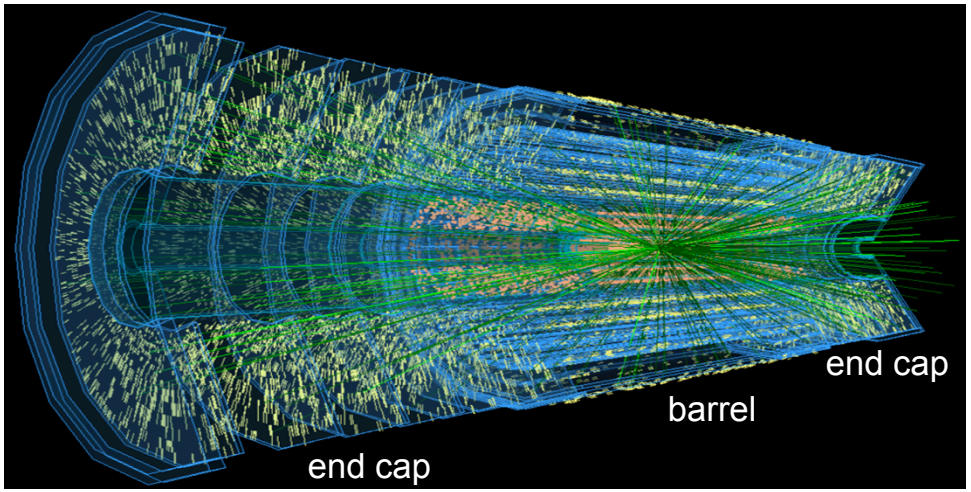
- ... largest is CMS HGC (Forward Calorimeter) — 780 m^2 silicon (pads)
- ... HL-LHC trackers of ATLAS and CMS — ~200 m^2 silicon (strips & pixels)



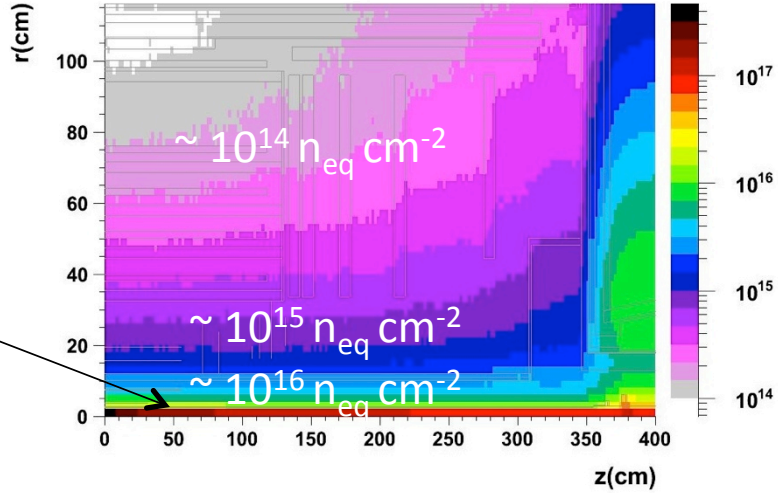


- Radiation hardness and rate performance must increase compared to LHC Run I by ...
  - phase 0 (2015) ≈ × 5
  - phase 1 (2018) ≈ × 5-10
  - phase 2 (>2025) ≈ × 10-30

- Increased luminosity (@ large area) thus demands ...
  - higher hit-rate capability
  - increased granularity
  - higher radiation tolerance
  - lighter detectors
  - cheaper price tag !!

> 10^{16} n_{eq} cm^{-2}

TID: > 1 Grad



Outline

- Silicon detectors under extreme particle rates and radiation
  - Current understandings
  - Strip/pixel developments for large systems
- Non-Hybrid detectors
- 4D developments

Apologies for having to make a selection

Rate and Radiation Levels

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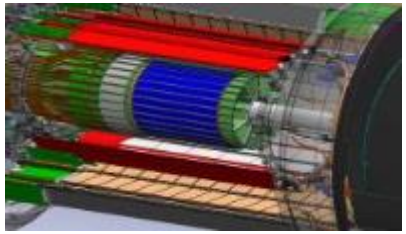
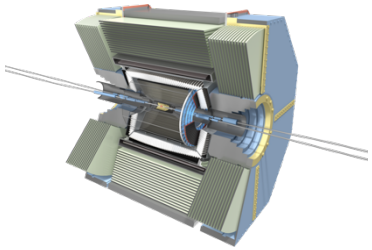
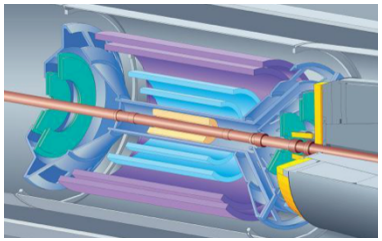
STAR



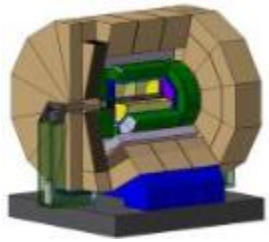
Belle II



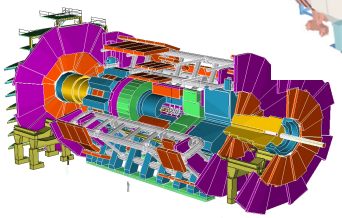
ALICE-(HL)-LHC

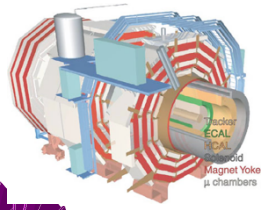


ILC



ATLAS





CMS

Numbers for innermost layers (r ≈ 5cm,) -> scale by 1/10 for typical strip layers (r > 25 cm)

	STAR	Belle II	ALICE-LHC heavy ion	ILC	LHC pp	HL-LHC-pp	
						Outer	Inner
BX-time (ns)	110	2	20 000	350	25	25	25
Particle Rate (kHz/mm^2)	4	400	10	250	1 000	1 000	10 000
Φ (n_{eq}/cm^2)	few 10^{12}	3 x 10^{12}	> 10^{13}	10^{12}	2x10^{15}	10^{15}	2x10^{16}
TID (Mrad)*	0.2	20	0.7	0.4	80	50	> 1000

*per (assumed) liftetime
LHC, HL-LHC: 7 years
ILC: 10 years
others: 5 years

in need for
- much less material
- higher resolution
- thinner strips & monolithic pixels

state of the art
- large area strips
- hybrid pixels

- even larger area
- radhard sensors
- higher rates R/O
- R&D of new types

Radiation

- From defect investigation -> defect engineering (example: oxygen enrichment)

make VO happen more likely than VP

↑

phosphorus = donor

Recipe

- Readout at n^+ electrodes (e^- collection)
- Operate at high bias voltages
- Carefully plan the annealing scenario
- Provide proper electrode design
- Use p-substrates (rather than n)

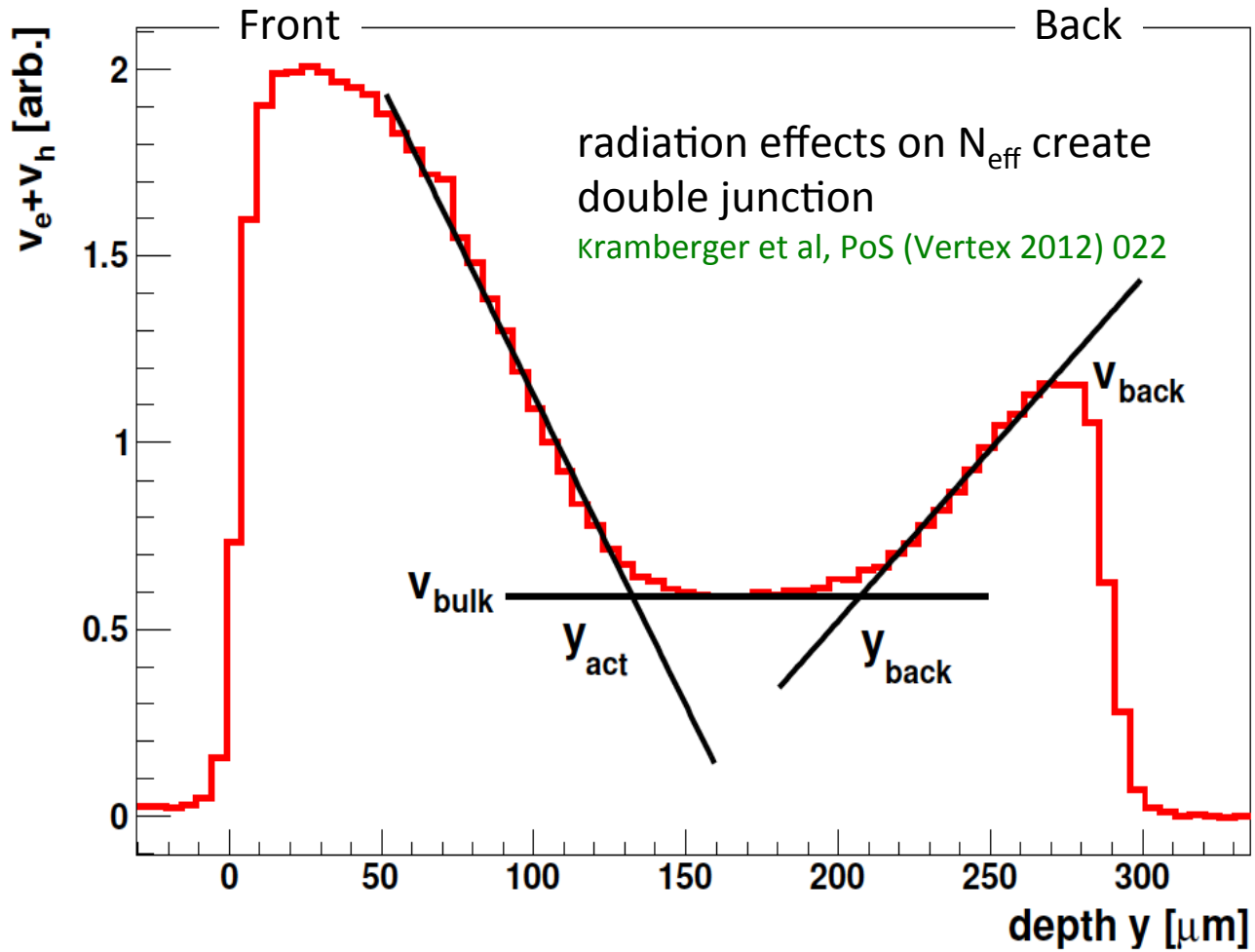
What we are used to ...

- change in I_{leak}

⇒ increased noise
⇒ increased power
⇒ thermal runaway
⇒ increased cooling
⇒ increased material

- change in N_{eff}

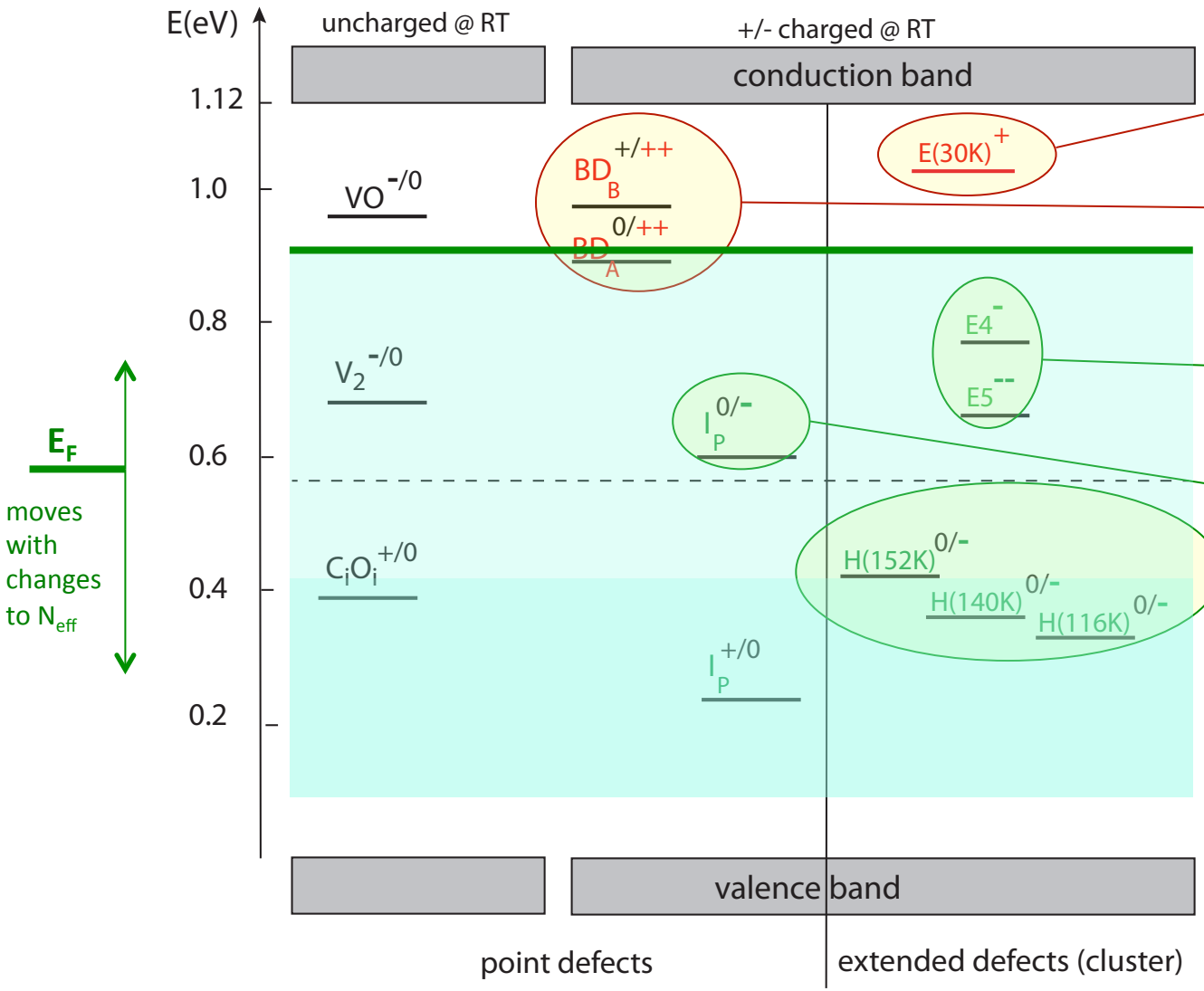
⇒ "type inversion"
⇒ "reverse annealing"
⇒ need higher V_{bias}
⇒ op. in partial depletion



- for $\Phi > 10^{15}\ n_{eq}/cm^2$ → charge trapping important: $Q_{tc} \cong Q_0 \exp(-t_c/\tau_{tr}),\ 1/\tau_{tr} = \beta\Phi.$

CCD becomes smaller than detector thickness (low Q) => need low noise @ high leakage current

Much progress in understanding radiated Si-sensors



e- trap
positive space charge
higher conc. after proton than neutron irradiation
depends on oxygen content

BD=bistable donor (e- trap)
positive space charge
strongly produced in oxygen rich DOFZ material

triple vacancy, small cluster
negative space charge
-> **high leakage current**

V_2O complex (?)
negative space charge
causes **leakage current**,
strongly produced in oxygen lean STFZ

extended acceptor defects produced equally by n,p
negative space charge
-> **reverse annealing**

- most defects show linear fluence dependence
- cooling helps to keep I_{leak} and rev. annealing smaller
- N_{eff} changes

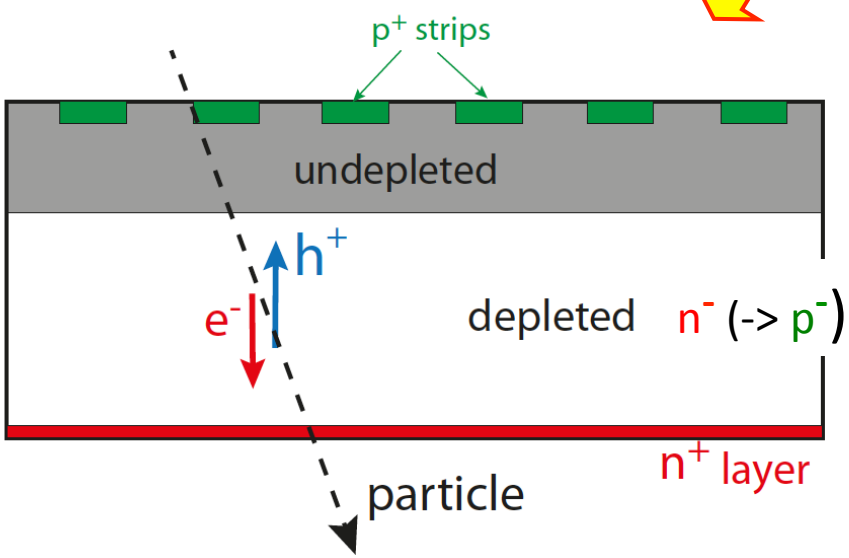
Radu et al., J. Appl. Phys. 117, 164503 (2015)
RD50, M. Moll et al., PoS (Vertex 2013) (2013) 026

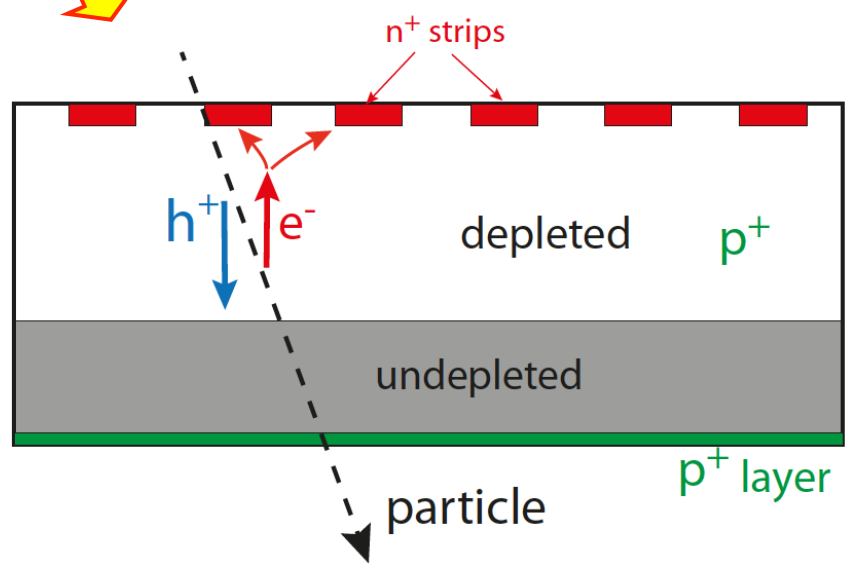
- most studies with n-type material

For upgrades: p-type silicon substrates

- classic strip choice: **p^+ in n**
- for HL upgrade: **n^+ in p** or **n^+ in n (-> p)**

after high irradiation





consequences:

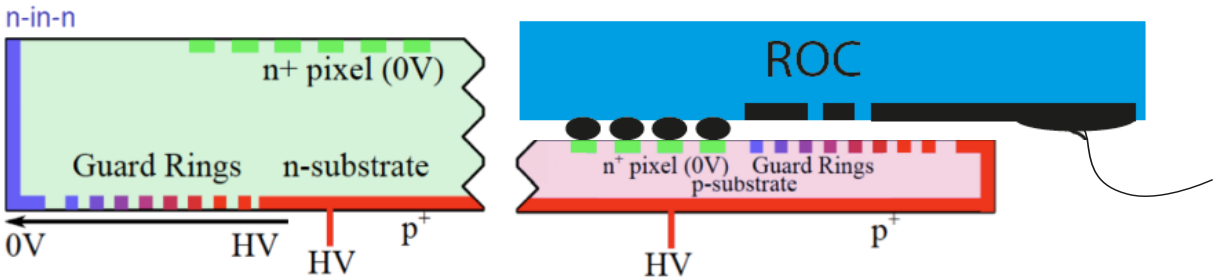
- signal loss
- resolution degradation (Q spreading)

advantages:

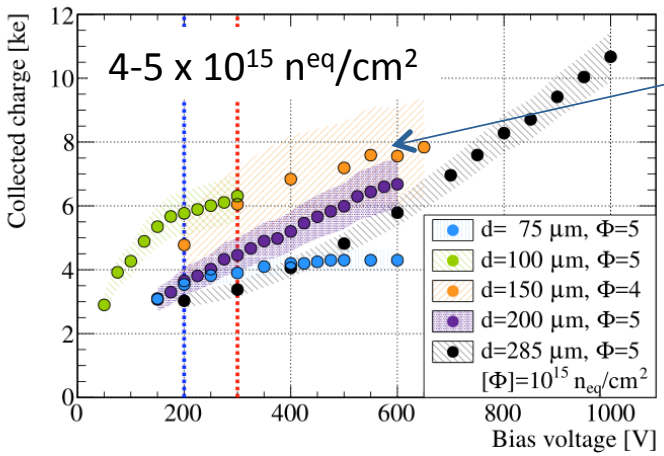
- faster charge collection (electrons)
- signal and CCE degradation less&smoother

p – type substrates favoured for strips and pixels

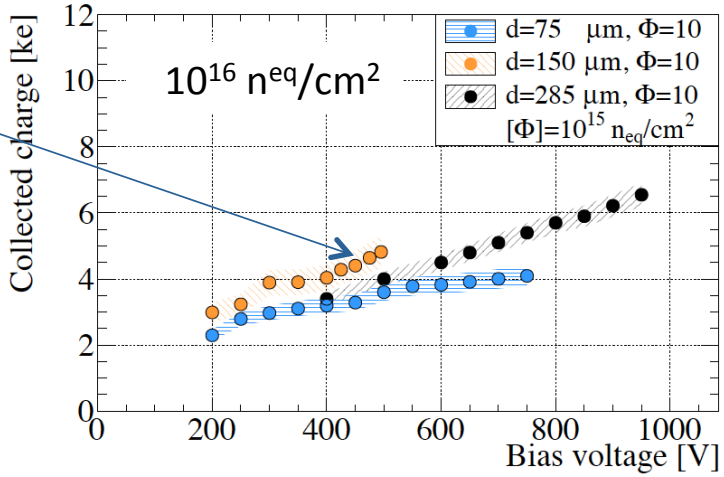
For very high fluences -> thin planar (pixel) sensors



- thin n^+ in p sensors after high fluences (neutrons)

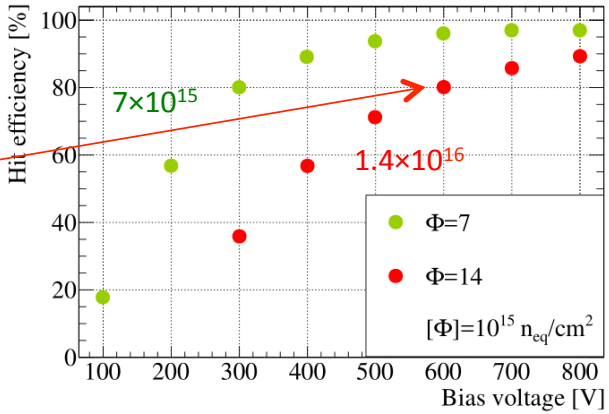


best (150 µm)



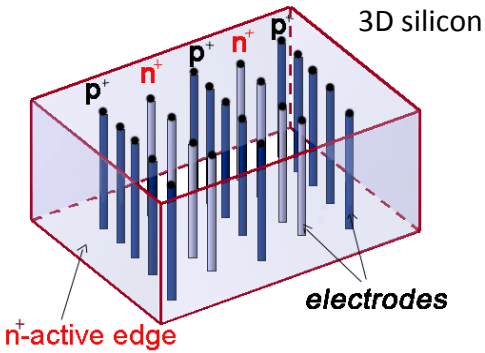
- **6000 – 7000 e-**
  for 100 - 200 µm sensors @ 300 V – 600 V bias

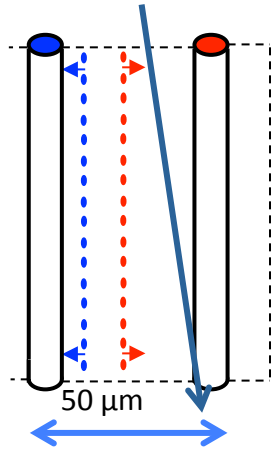
- hit efficiencies still reasonable at $\Phi > 10^{16}$



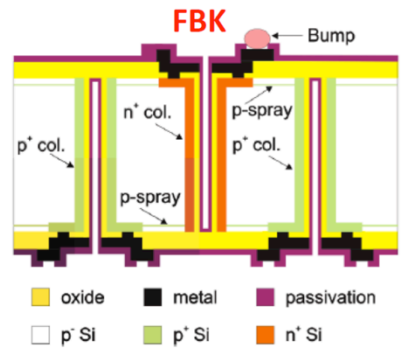
Terzo, Andricek, Macchiolo, Nisius et al, JINST 9 (2014) C05023

3D-Si sensors for the innermost pixel layer(s)

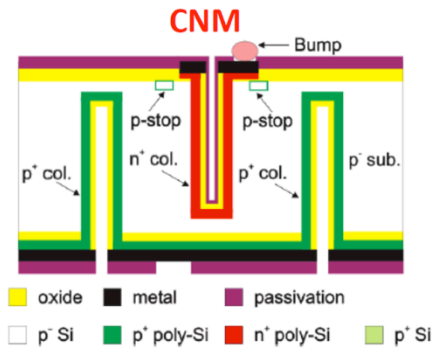




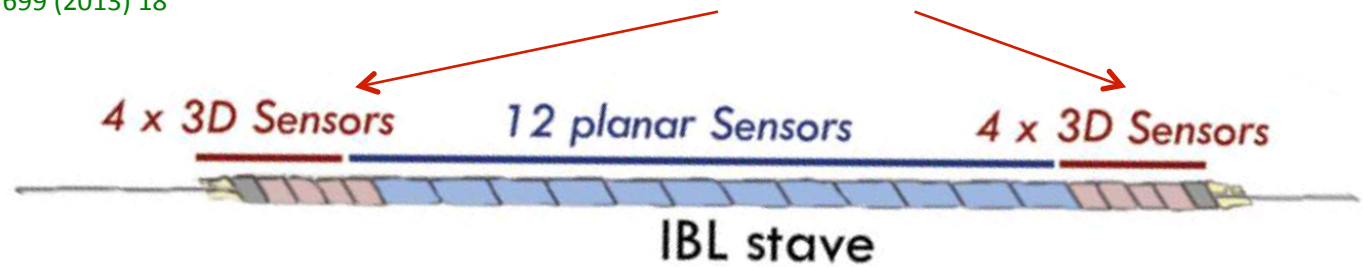
S. Parker, C. Kenney , J. Segal, ICFA Instrum.Bull. 14 (1997) 30-50
C. Da Via, et al., NIM A49 (2005) 122-125 and NIM A 699 (2013) 18



G.F. Della Betta et al.,
PoS Vertex2012 (2013) 014



G. Pellegrini et al..
NIM A731 (2013) 198-200



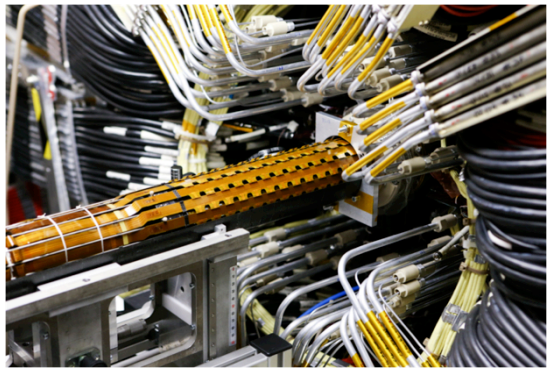
- ➢ particle path (signal) different from drift path
- ➢ high field w/ low voltage

-> radiation tolerance
-> Q still 50% @ 10^{16} cm^{-2}

- ➢ good for inclined tracks

- ▪ slightly larger C_{in} (noise)

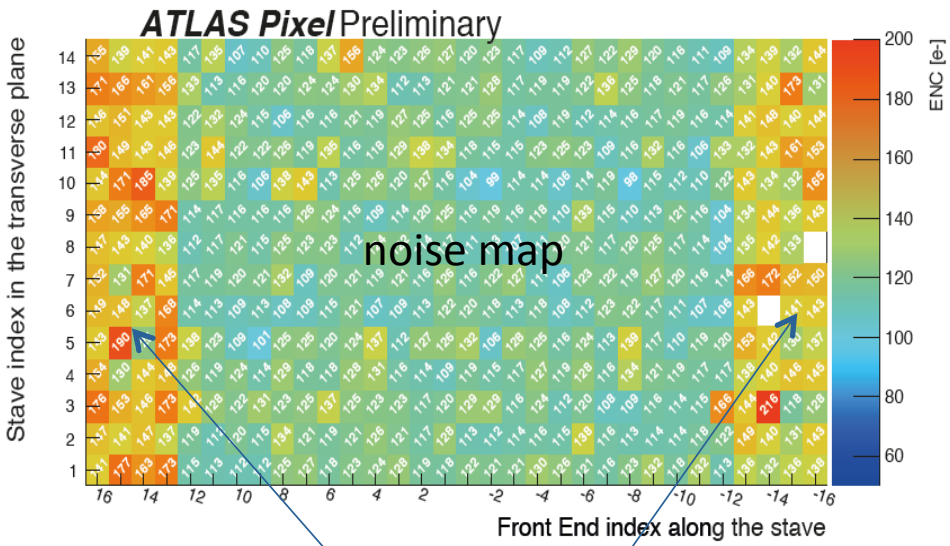
- ✧ now also in diamond, CdTe



- ▪ 3D sensors have been put to reality
- ▪ in ATLAS IBL for one year
- ▪ Let's see how they performed

see also dedicated talk by Didier Ferrere

3D-Si sensors in ATLAS at 13 TeV and 0.5×10^{34} cm^{-2} s^{-1}

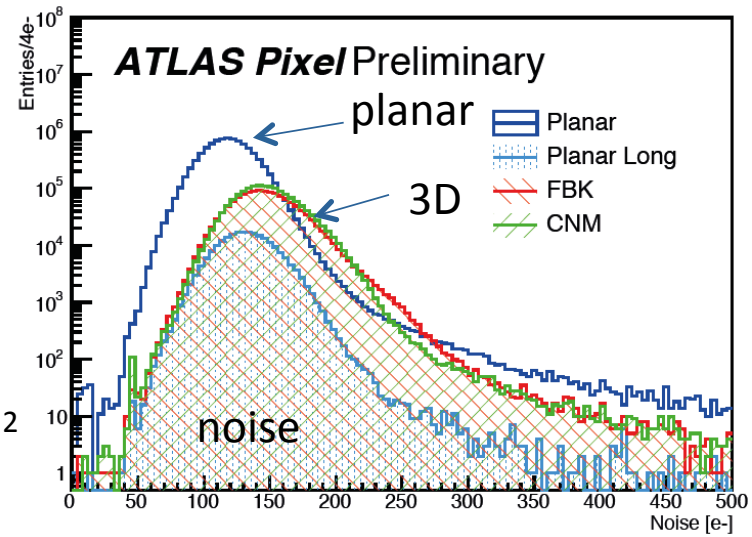


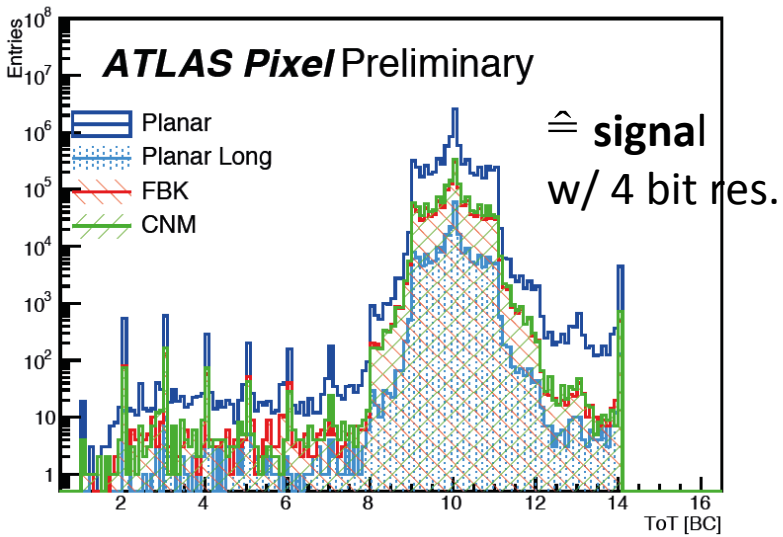
after 4.3 fb^{-1}

radiation

1.3 Mrad

2.5 10^{13} n_{eq}/cm^2



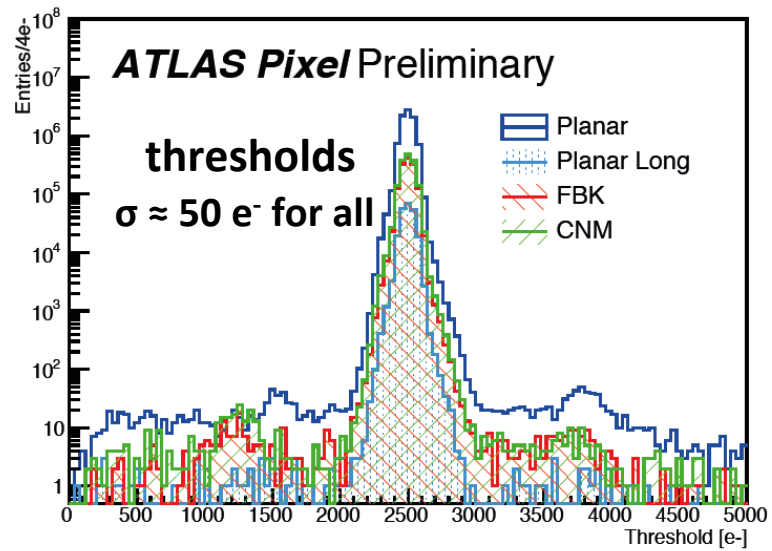


bias voltage

IBL 3D: 20 V

IBL planar: 80 V

B-layer: 250 V



Conclusion: 3D-Si sensors seem suited for inner pixel layer(s) @ HL-LHC

Pixel R/O-Chip for HL-LHC rates (and radiation)

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- effort and costs so large that joint approach (cross experiments) is needed -> **RD53** (20 Institutes)
- decide on technology w/ some probability of sustainability -> **65 nm TSMC**

FE-I3

< 100 MHz/cm^2
< 100 Mrad

250 nm technology

pixel size 400 × 50 µm^2

3.5 M. transistors

FE-I4

hit rate < 400 MHz/cm^2
1.8 mW/mm^2
rad hard: 5x10^{15}/cm^2
200 Mrad

130 nm technology

pixel size 250 × 50 µm^2

70 M transistors

FE-65

hit rate 2-3 GHz/cm^2
< 1 MHz trigger @12µs
3.5 mW/mm^2
rad hard: 2x10^{16}/cm^2
1 Grad

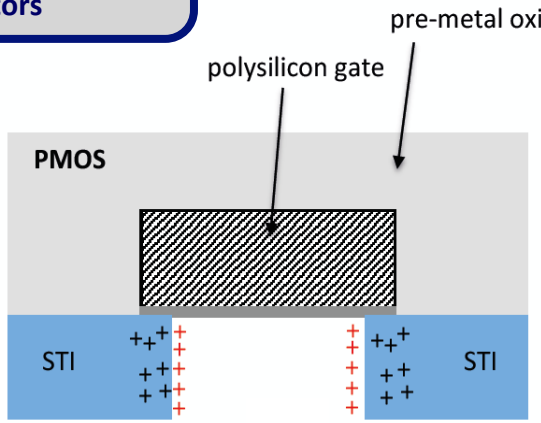
65 nm technology

pixel size 50 × 50 µm^2

~ 1000 M transistors

- FE-65 first full-size prototype -> spring 2016
- Deep submicron (250 nm & 130 nm) saved LHC pixel R/O chips
- 65 nm has its own – geometry induced – radiation effects to deal with
- Requires long and tedious study program ...

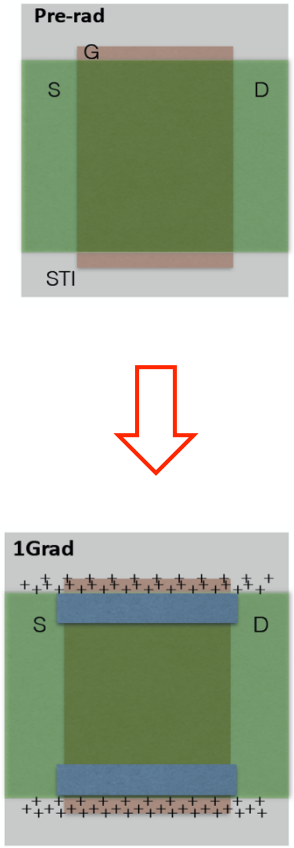
RINCE = Radiation Induced Narrow Channel Effects



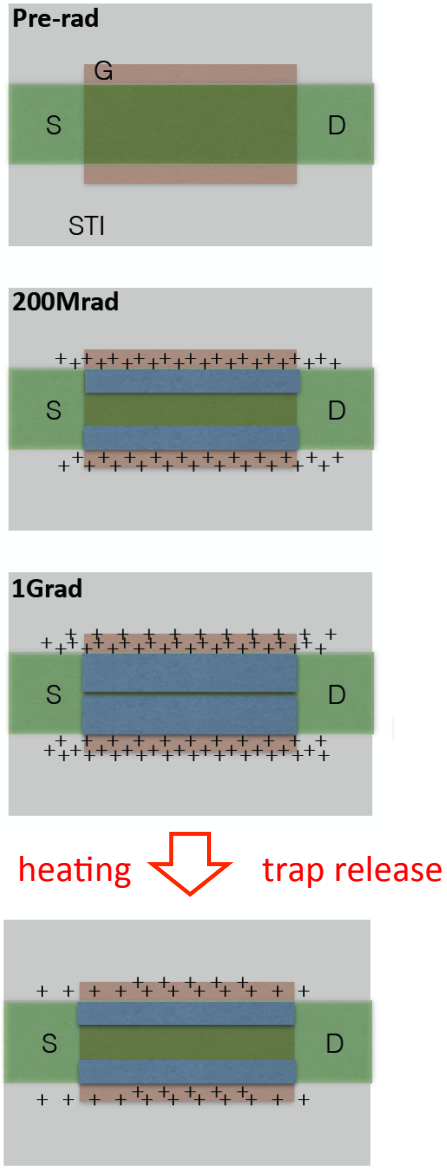
see F. Faccio, TWEPP 2015, Proceedings

Radiation effects in 65 nm CMOS small channel devices

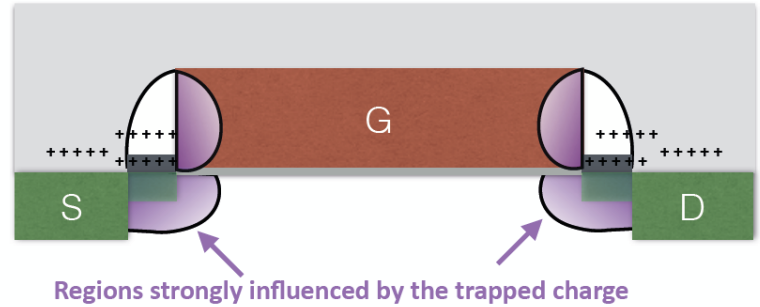
W = moderate size



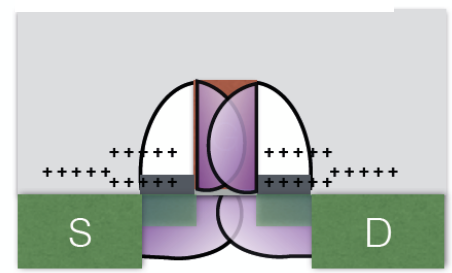
W = minimum size



L = moderate size



L = minimum size



cartoons: F. Faccio, TWEPP2015

Short channel 65 nm PMOS suffer more than NMOS

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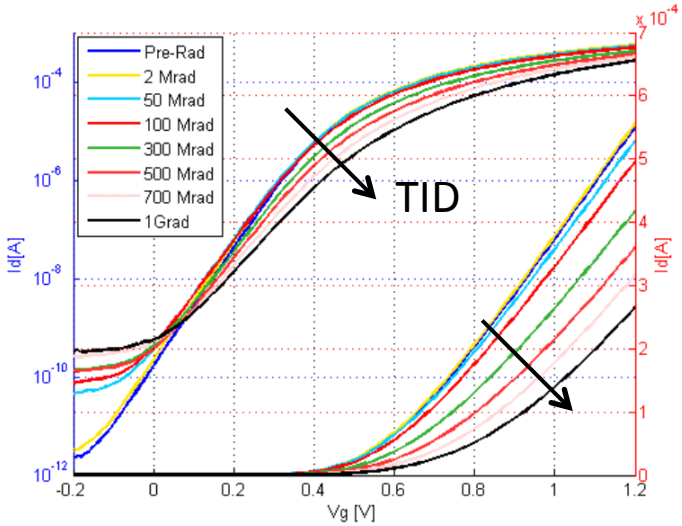
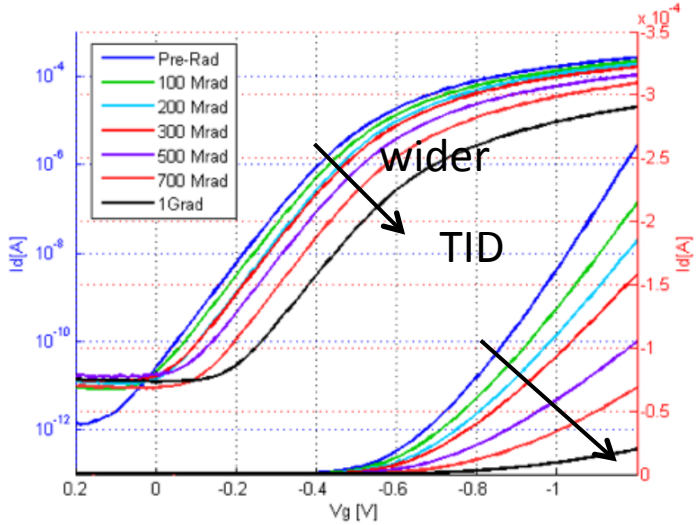
NMOS



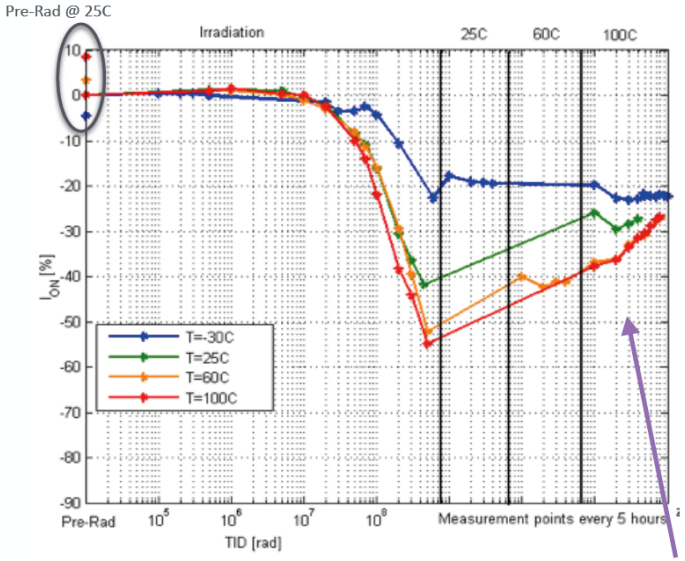
PMOS



Transistors' size: W=1um, L=60nm
Irradiation conditions:
T = 25C
Bias: |Vgs|=|Vds|=1.2V

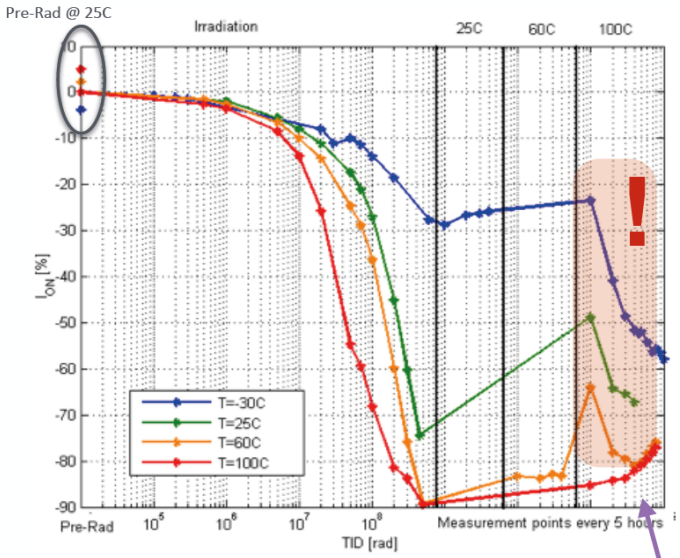
Transfer characteristic

NMOS



Some recovery at high T for the most damaged

PMOS



Relevant degradation at high T for the less damaged

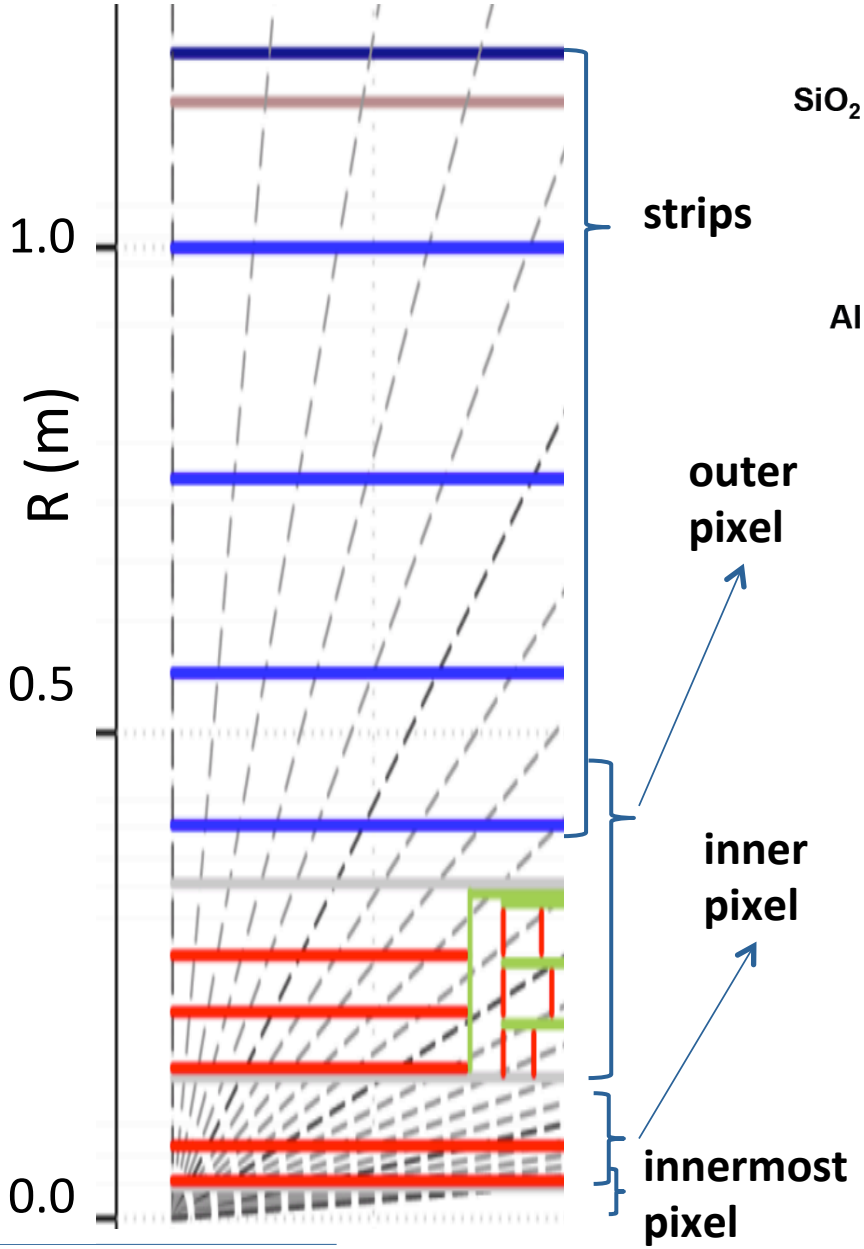
Temperature dependence of I_{ON}

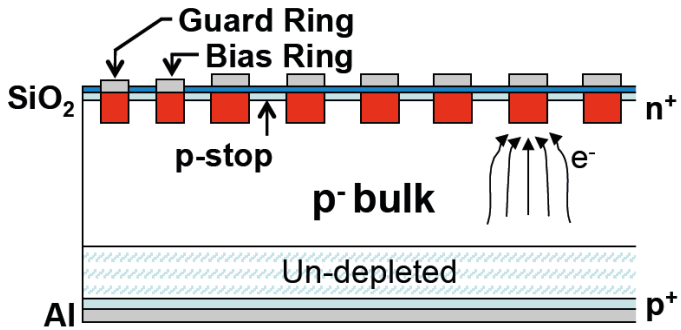
F. Faccio, TWEPP 2015, Proceedings

Transistors' size: W=0.6um, L=60nm

Large Systems

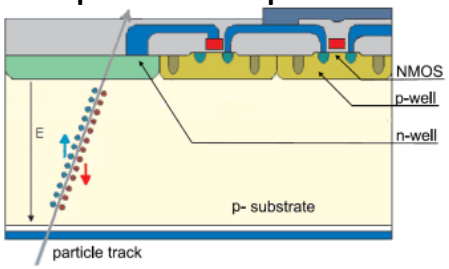
Typical pre-TDR favourite views ...

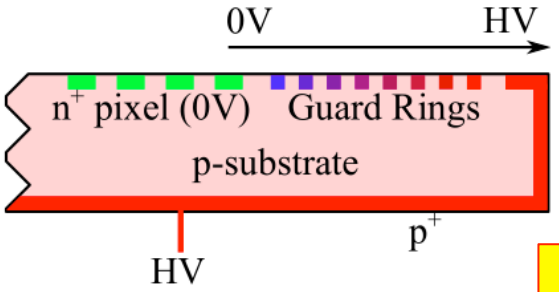




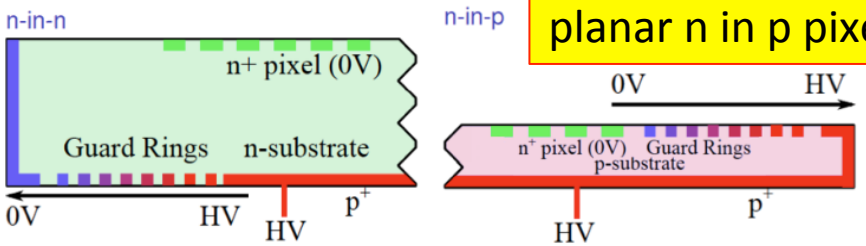
n in p
strip modules

depl. CMOS pixels

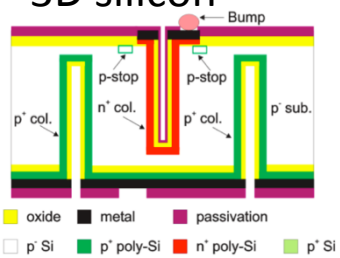




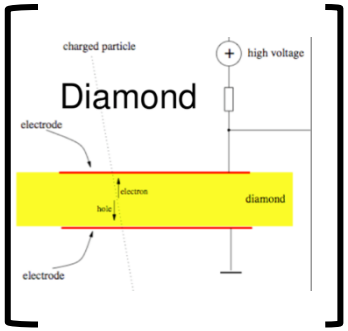
large modules
planar n in p pixels / CMOS?



3D silicon



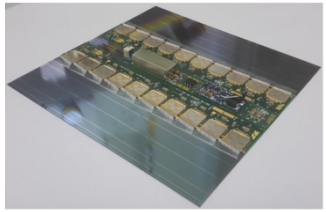
dedicated
rad.-hard
detectors



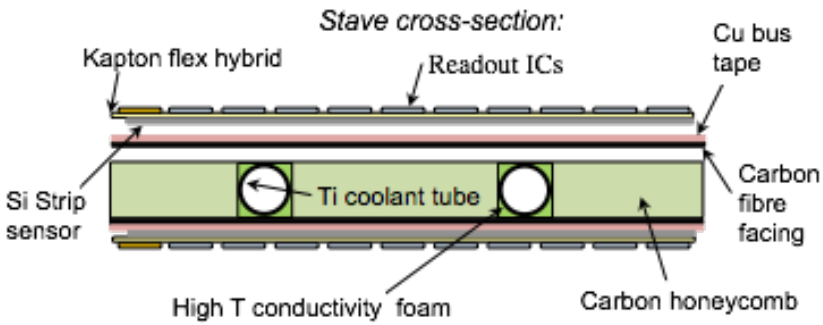
Large Area Strip Trackers of ATLAS and CMS

- "Large" meaning: 200 - 220 m^2 strips and 8 - 18 m^2 pixels

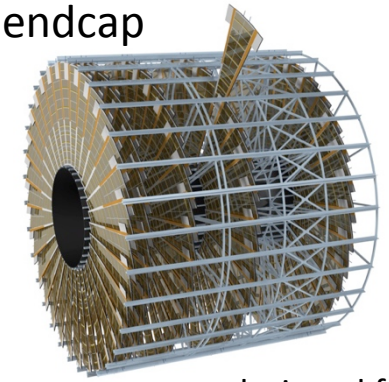
Main points
ATLAS
- affordable cost
- finer segmentation
- simplicity & robustness @ min. material

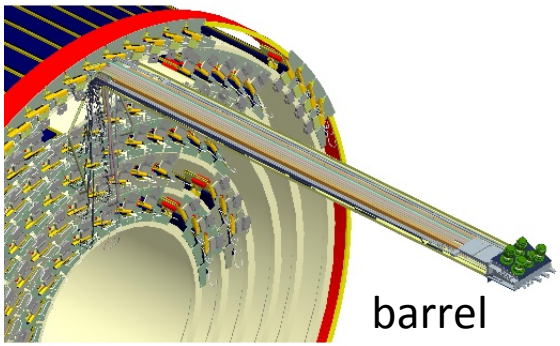


10x10 cm^2
2.5 cm strips
limit of strip geom?



endcap

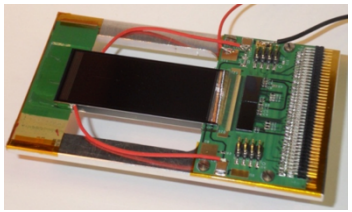


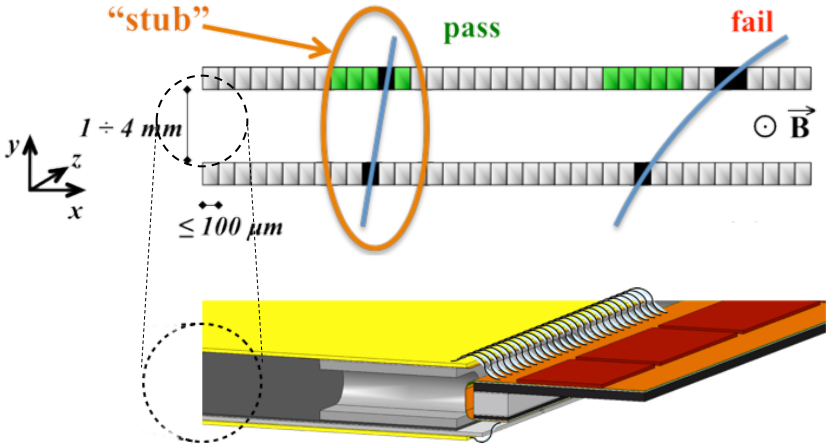


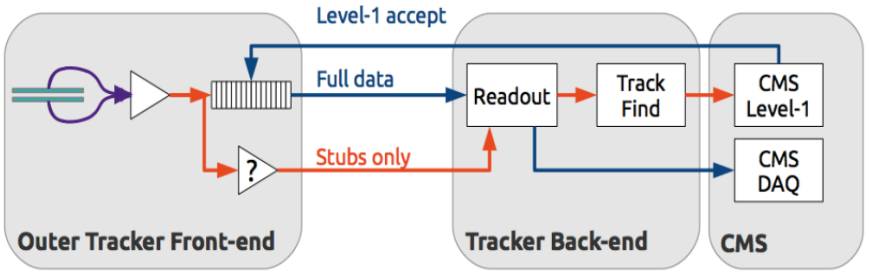
barrel

designed for end insertion

Main points
CMS
- same principle goals plus ...
- p_T module & tracks in trigger @ L1
- new industrial 8" (-> 12") sensors



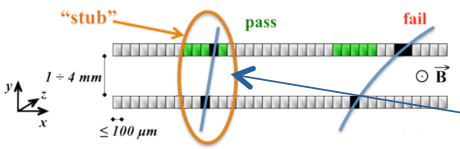


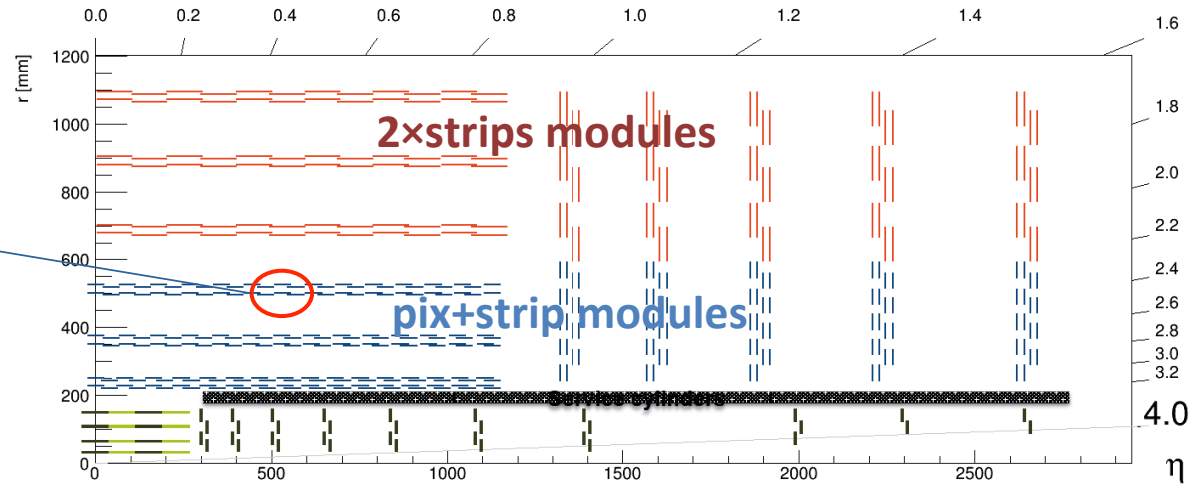


see e.g. T. Affolder, various talks

see e.g. D. Abbaneo, CERN PH seminar, F. Ravera 13th Pisa Meeting

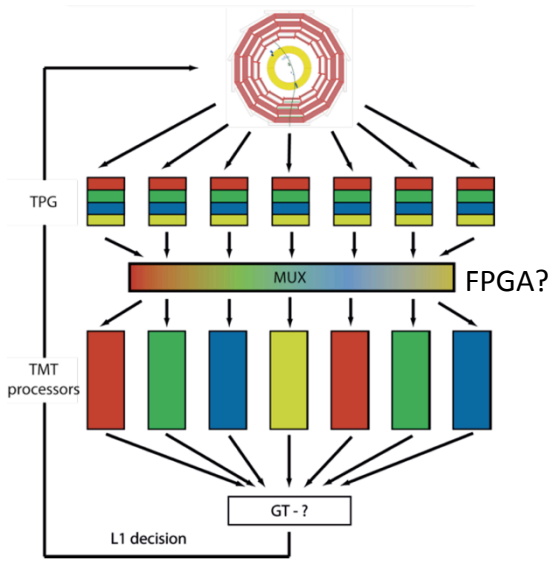
CMS Outer Tracker



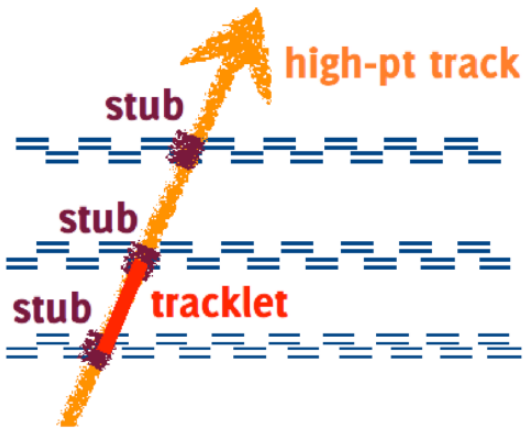


process stubs

use CAMs for fast pattern matching



use Time MUX Trigger to process complete event



get (high p_T) tracks seeded by stubs pairs

NEW ... introducing a large scale sensor producer

universitätbonn

SINTEF

VTT

MICRON SEMICONDUCTOR ltd

MPG HLL

FONDAZIONE BRUNO KESSLER

CiS Forschungsinstitut für Mikrosensorik und Photovoltaik GmbH

cnm Centre Nacional de Microelectrònica IMB

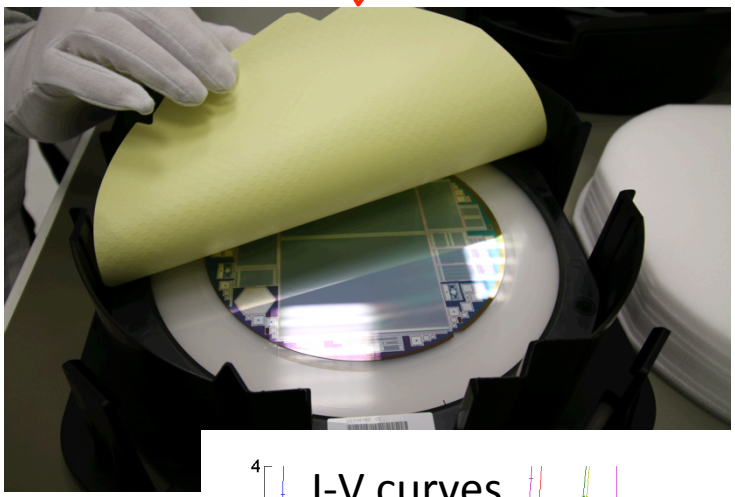
10 to some 100 wafers / year

HAMAMATSU PHOTONICS YOUR BUSINESS

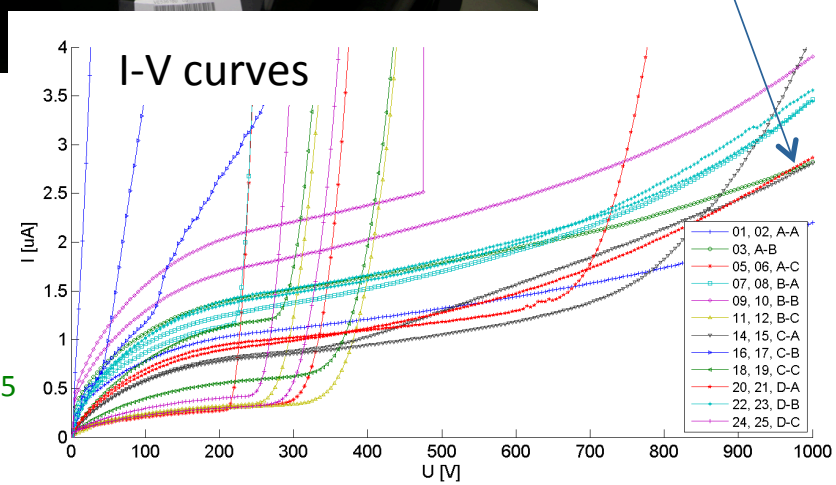
1000 – 10 000 / year

infineon

A possible VERY large scale producer:
- Wafer Output: 50.000 per week
- 8" wafers -> 12" wafers aimed for



many stable up to 1000 V

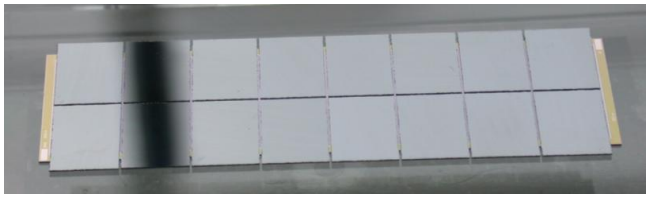


T. Bergauer et al., CMS tracker group, Hiroshima Conf. 2015
J. Hacker, Hiroshima Conference 2015

Large area pixel modules

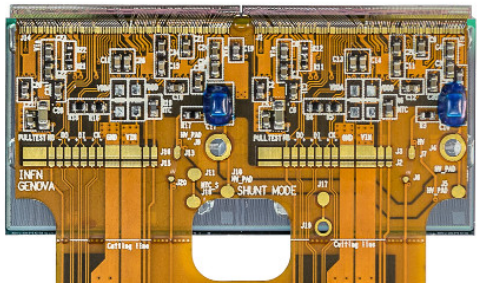
- Evolution of pixel modules

~2 × 5 cm²

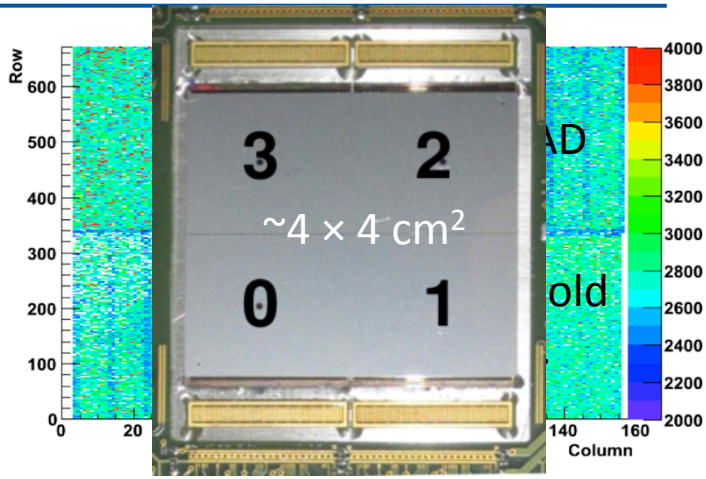


2009: ATLAS Pixel 16-chip module

~2 × 4 cm²



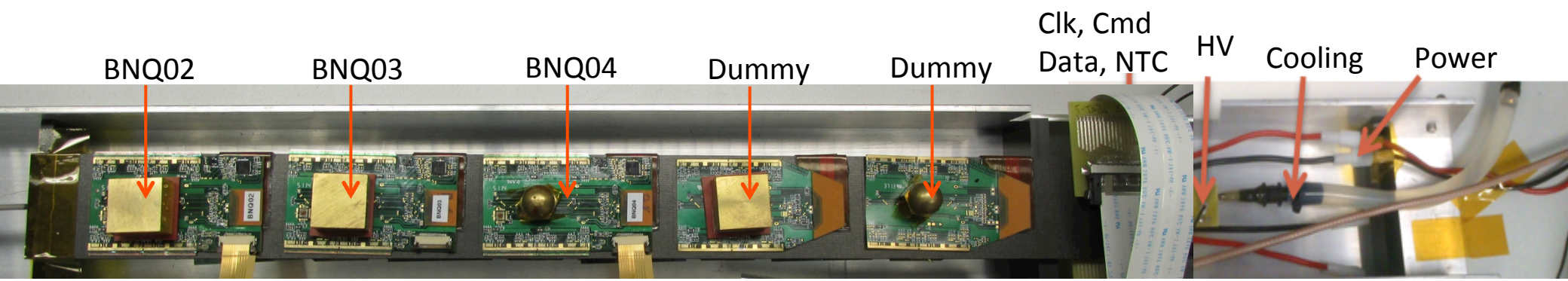
2014: IBL: 2-chip module



QUAD module (2x2 chips)
with ganged and "long" pixels
covering the interchip area

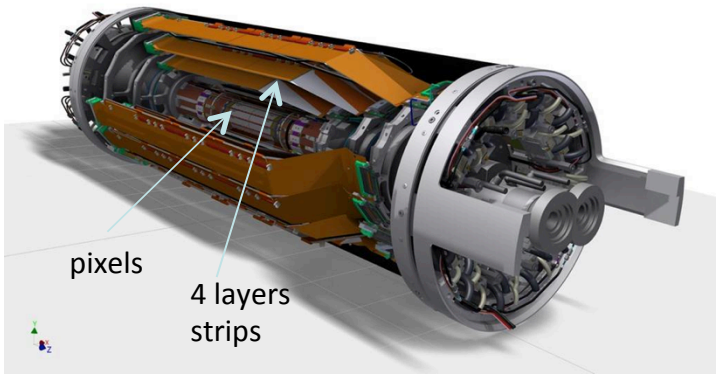
- Switch from parallel to serial powering
  due to granularity and power increase at HL-LHC
- has better power, material, and cost efficiency
- constant current -> voltages via on-chip Shunt-LDOs
- need proof that indiv. module failures, power line ripples, AC coupled data transmission can be dealt with

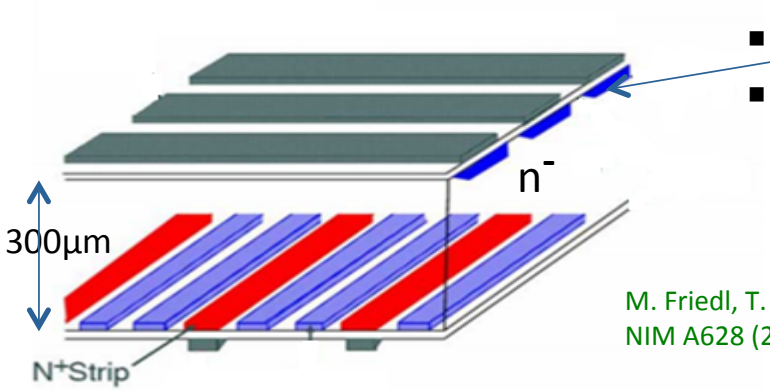
Bao Ta, ... NW et al., NIM A557 (2006) 445-459
L. Gonella, ..., NW, et al. JINST 5 (2010) C12002



QUAD modules (3+3) plus 6 dummies on serially powered double sided stave

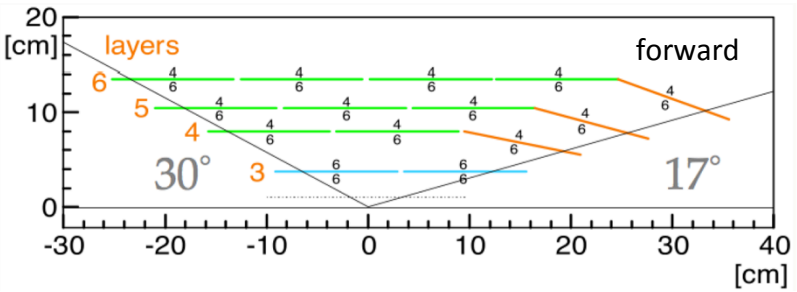
Belle II SVD Double Sided Strips (DSSD)





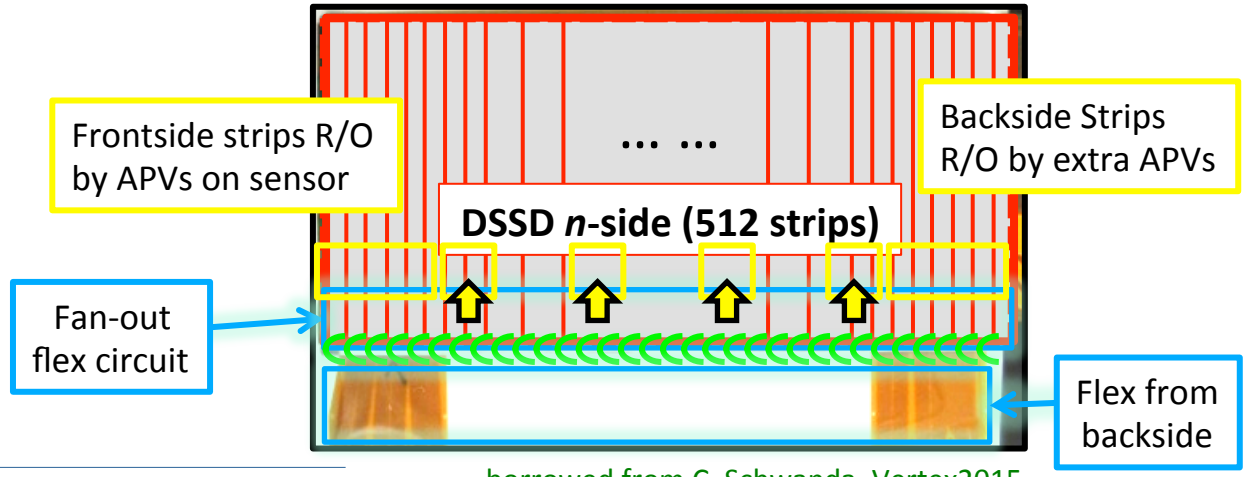
- p^+ in n^- strips
- double sided readout

M. Friedl, T. Bergauer, I. Gfall, C. Irmler, M. Valentan, NIM A628 (2011) 103-106

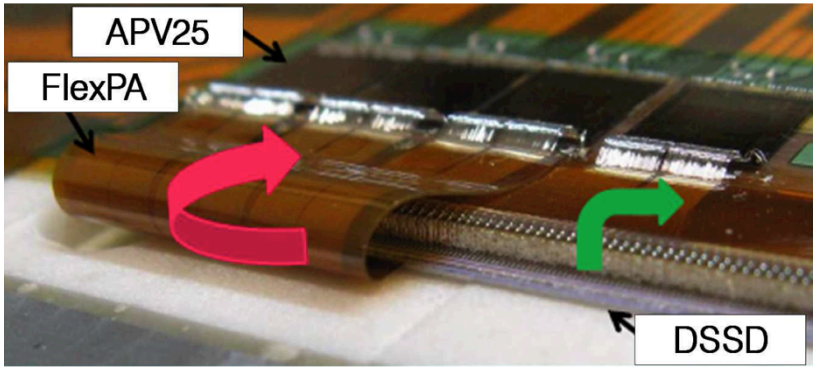


important features

- light weight 0.58% X_0
- "Origami" ASIC placement (chips from both sides placed on sensor)



borrowed from C. Schwanda, Vertex2015



❑ Non – Hybrid (Semi -) Monolithic

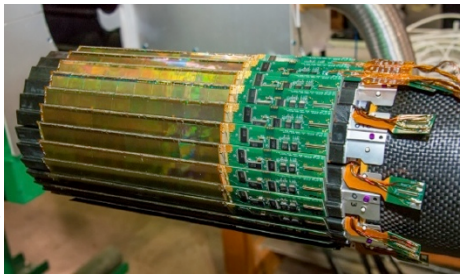
Can one do better than "hybrid"?

universitätbonn

Hybrid Pixel Detectors

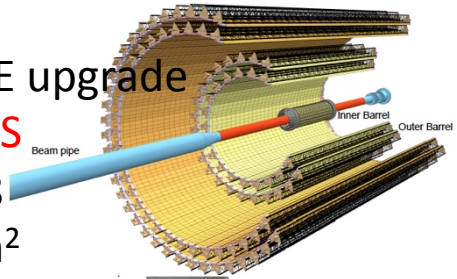
- **PROs**
  - complex signal processing already in pixel cells possible
  - zero suppression
  - temporary storage of hits during L1 latency
  - radiation hard to $>10^{15}$ n_{eq}/cm^2
  - high rate capability (~MHz/mm^2)
  - spatial resolution ~ 10 – 15 µm
- **CONs**
  - relatively large material budget: ~3% X_0 per layer (1% X_0 @ ALICE)
  - sensor + chip + flex kapton + passive components
  - support, cooling (-10°C operation), services
  - resolution could be better
  - complex and laborious module production
  - bump-bonding / flip-chip
  - many production steps
  - expensive
- hence: (Semi-)Monolithic pixels in part relying on commercial CMOS processes have come in focus (at first outside LHC-pp)

STAR
MAPS
2014
0.16 m^2

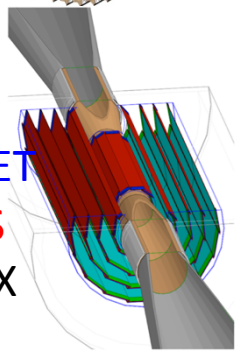


Belle II
DEPFET
2017
0.014 m^2

ALICE upgrade
MAPS
2018
10 m^2

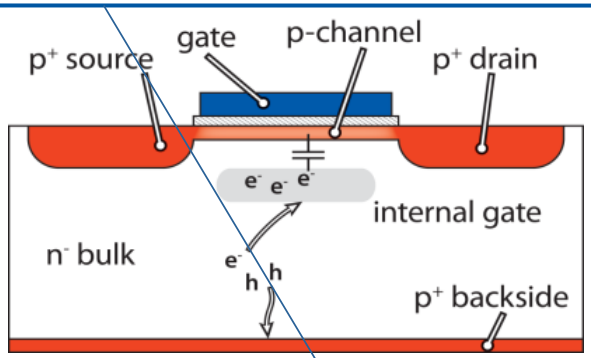


ILC
DEPFET
MAPS
SOIPIX
20??

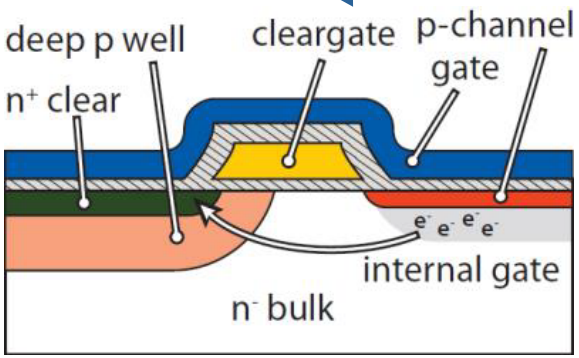


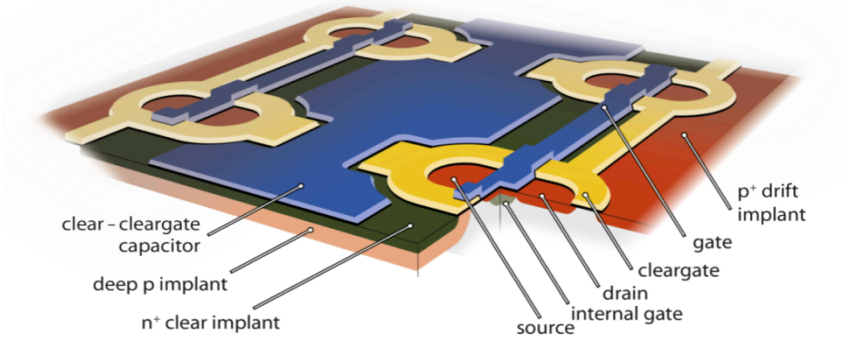
DEPFET pixels for BELLE II

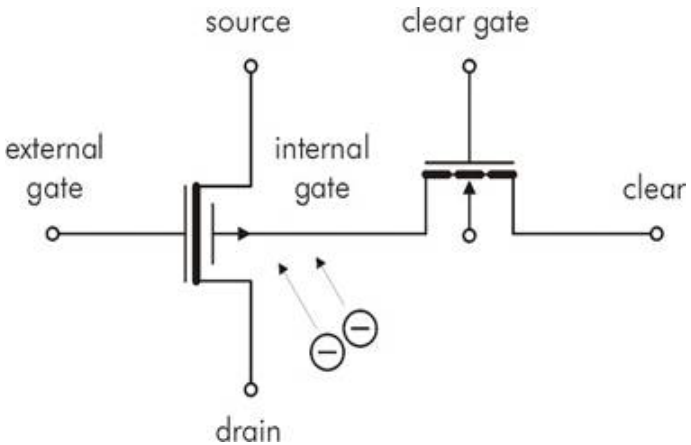
1)



2)







Charge stored in internal gate coupling capacitively into transistor channel, thus moduling the output current I_{drain} .

internal amplification

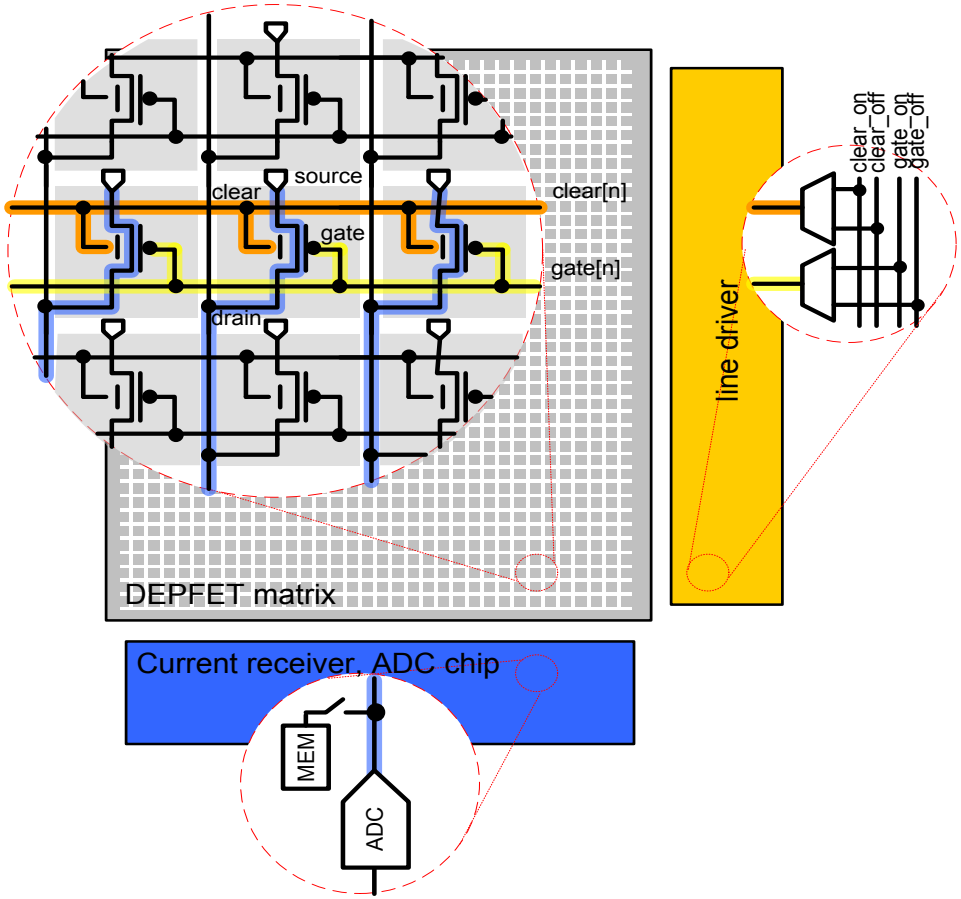
$$g_q = \alpha \frac{g_m}{W L C_{ox}}; \quad \alpha \lesssim 1$$

features:

- g_q~ 700 pA/e^-
- small intrinsic noise
- sensitive off-state, w/o power used

Kemmer, J., G. Lutz et al., Nucl. Inst. and Meth. A 288 (1990) 92

DEPFET pixel array



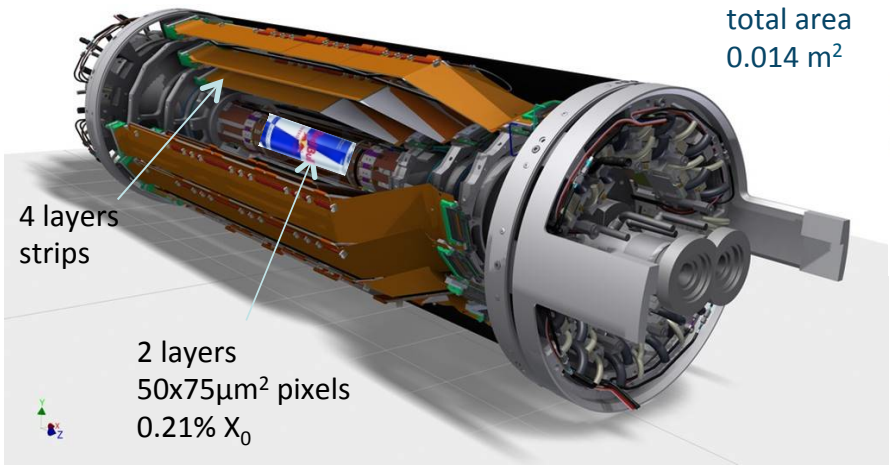
rolling shutter R/O mode

- DEPFET pixel transistors arranged in a matrix
- row wise select -> column wise readout of transistor (drain) currents
- Gate and clear lines need a steering chip
- Long drain readout lines to keep material out of the acceptance region
- 100 ns per row
  20 µs per frame

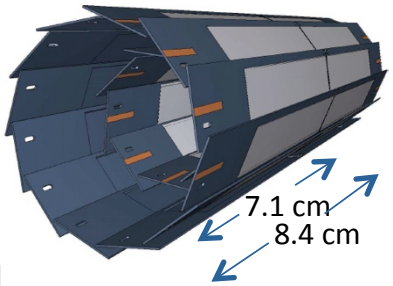
more in talk by Florian Lütticke (next)

BELLE II Pixel Detector

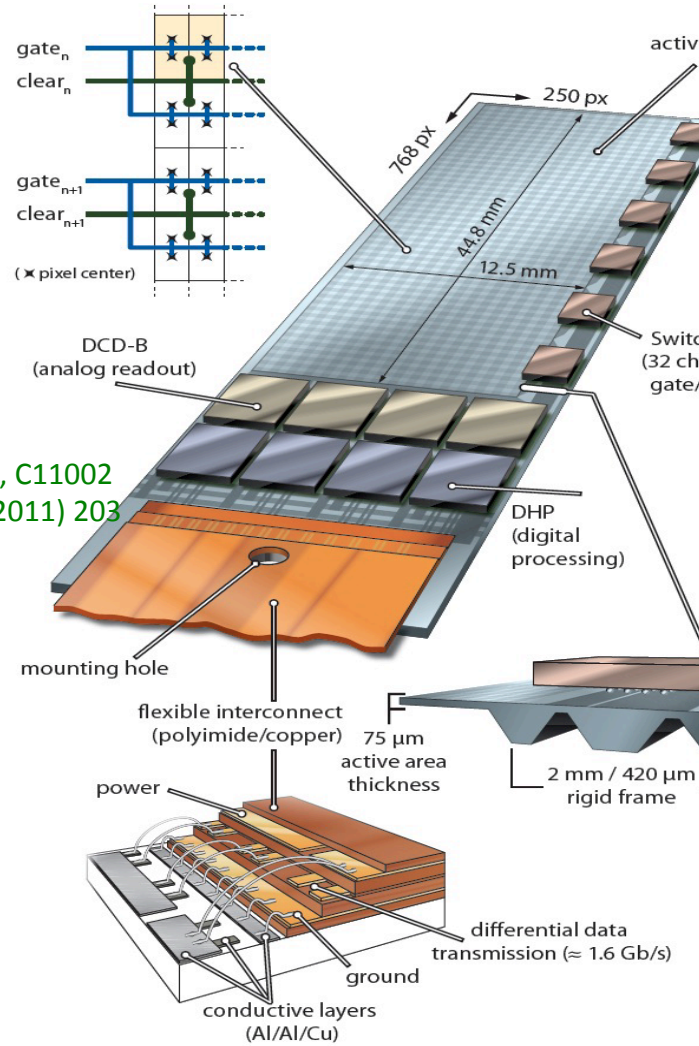
2-layer pixel vertex detector (PXD)

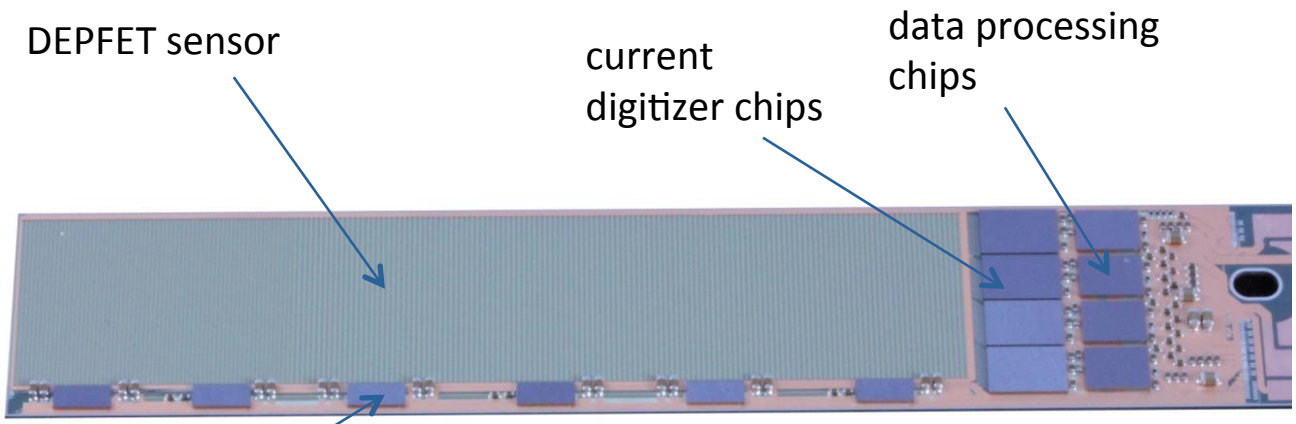


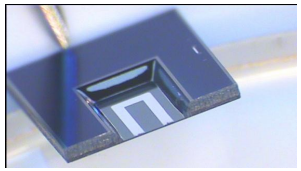
total area
0.014 m²

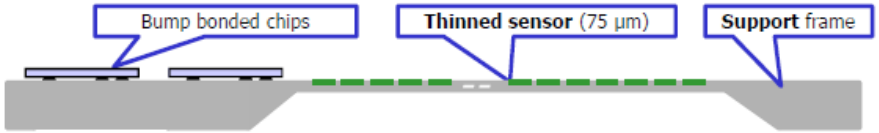


C. Marinas et al., JINST 10 (2015) 11, C11002
C. Kiesling et al., PoS EPS-HEP2011 (2011) 203



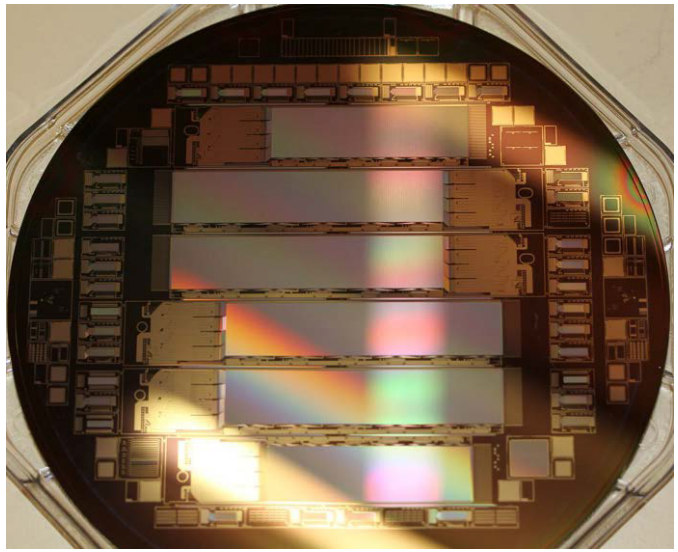


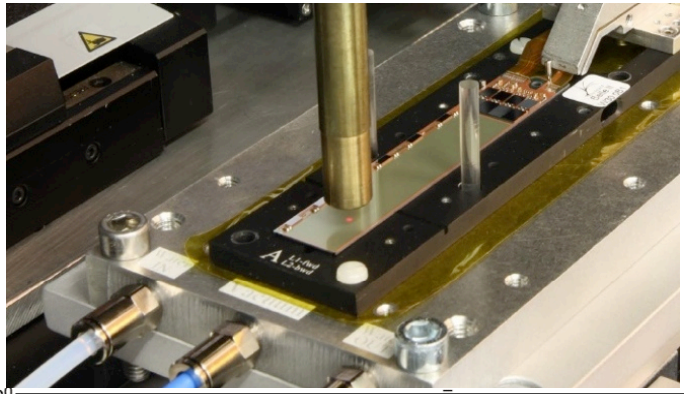


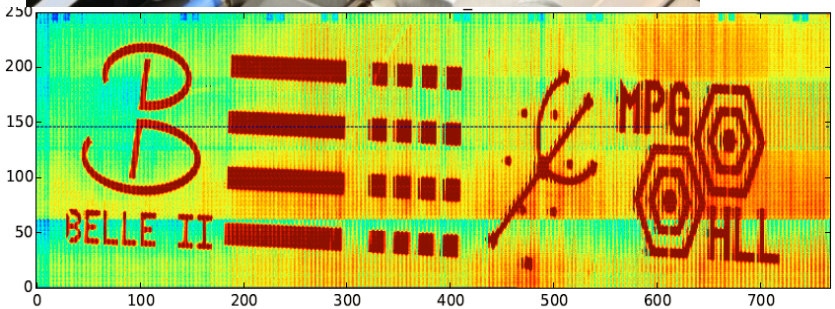


L. Andricek, IEEE Trans.Nucl.Sci. 51 (2004) 1117-1120

DEPFET PXD is closing in on production ...





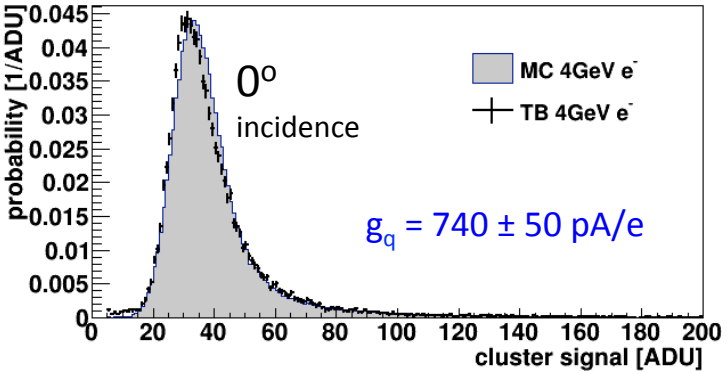


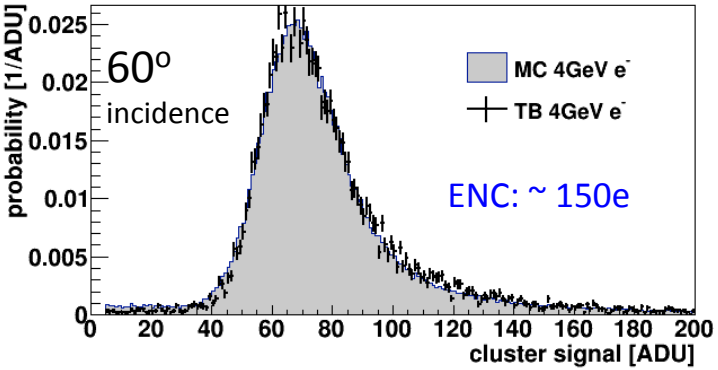
from . F. Müller (MPIM)

<u>expected radiation</u>
electrons and
synchr. radiation

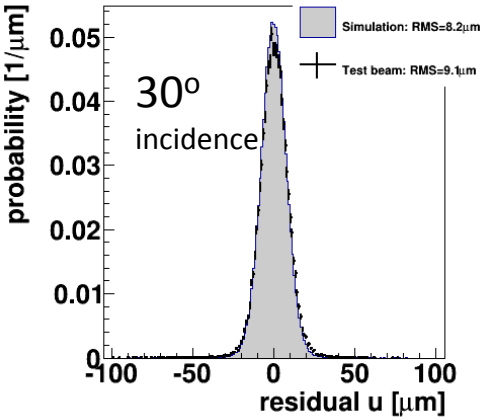
< 20 Mrad

testbeam results



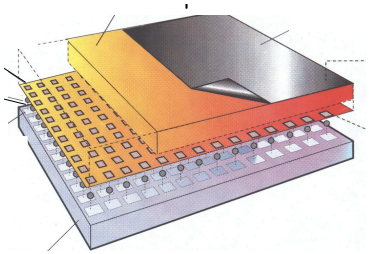


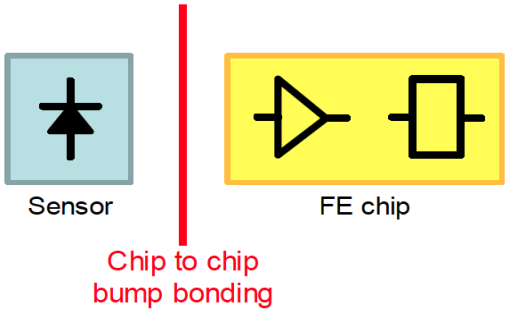
from B. Schwenker (Göttingen)

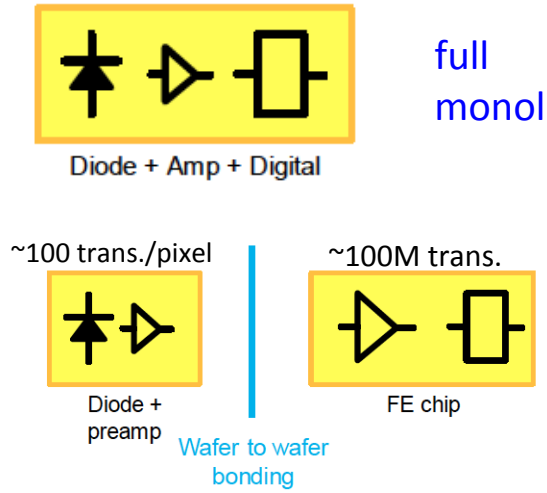


<u>resolution</u>
~ 8-11 μm (50 μm pitch)
~ 13 μm (75 μm pitch)

From HYBRID to monolithic CMOS pixels







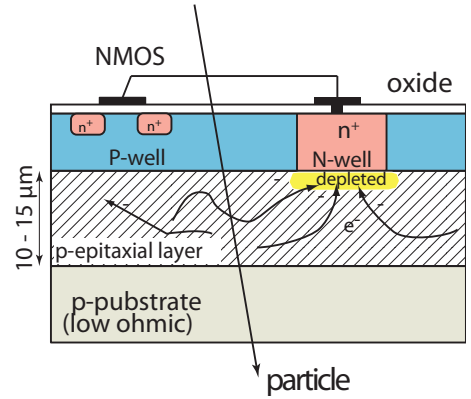
Monolithic **A**ctive **P**ixel **S**ensors

B. Dierickx, D. Meynants, G. Scheffer, SPIE 3410:68-76 (1998)
R. Turchetta, …, M. Winter et al, NIM A458 (2001) 677-689

- **MAPS** using CMOS with Q-collection in **epi**-layer: developed for > 10 yrs
  Q by <u>diffusion</u> → recent advances

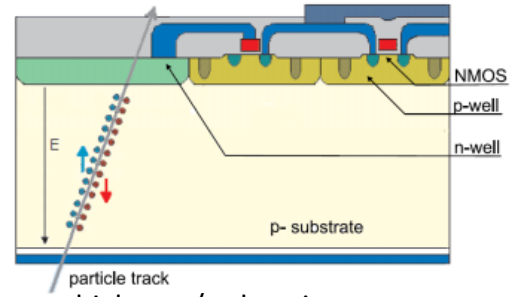
- Depleted **DMAPS** (CMOS pixels)
  - using **HR** substrates and **HV** add-ons to create some depletion region
  - CMOS on **SOI**

STAR + ALICE



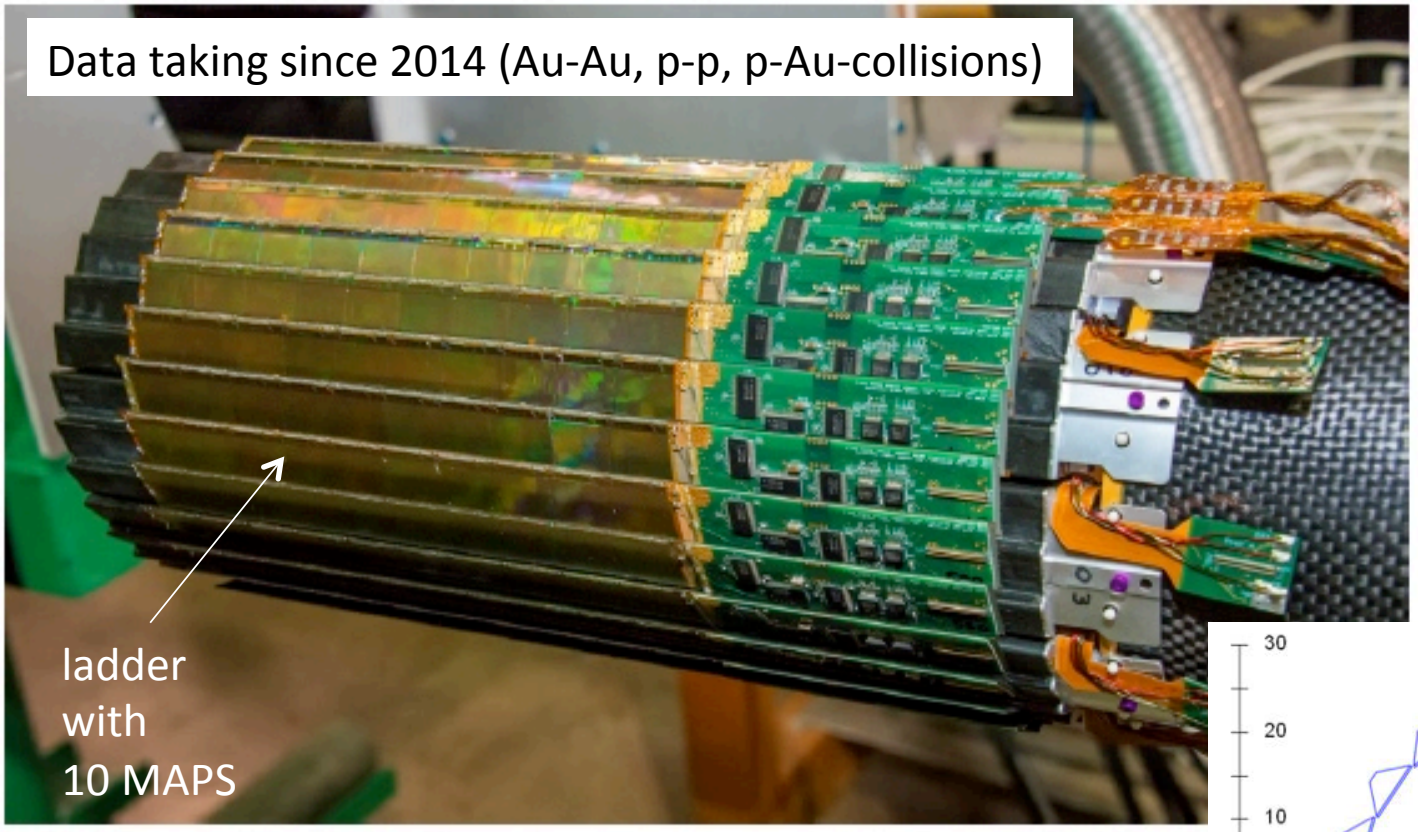
HL - LHC

$$d \sim \sqrt{\rho \cdot V}$$

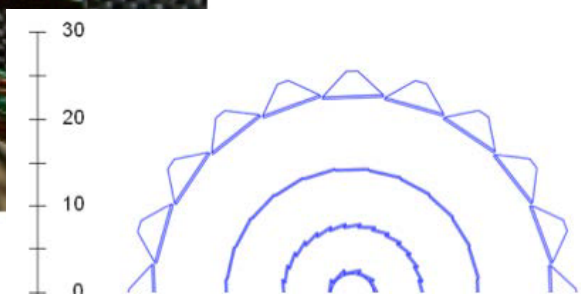


high rate/rad environment

MAPS-Pixels of the STAR detector @ RHIC



356 M pixels
in 2 layers
~0.16 m^2



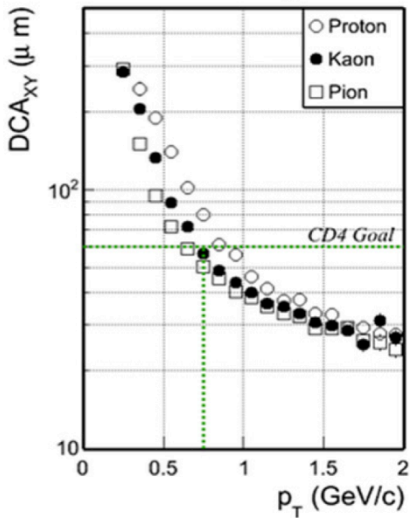
Features

- 20.7 x 20.7 μm^2 pixels
- rolling shutter R/O
- signal ~1000 e-
- S/N ~ 30
- 0.39 % X/X_0

- < 90 krad / year
- < 10^{12} n_{eq}/cm^2/year

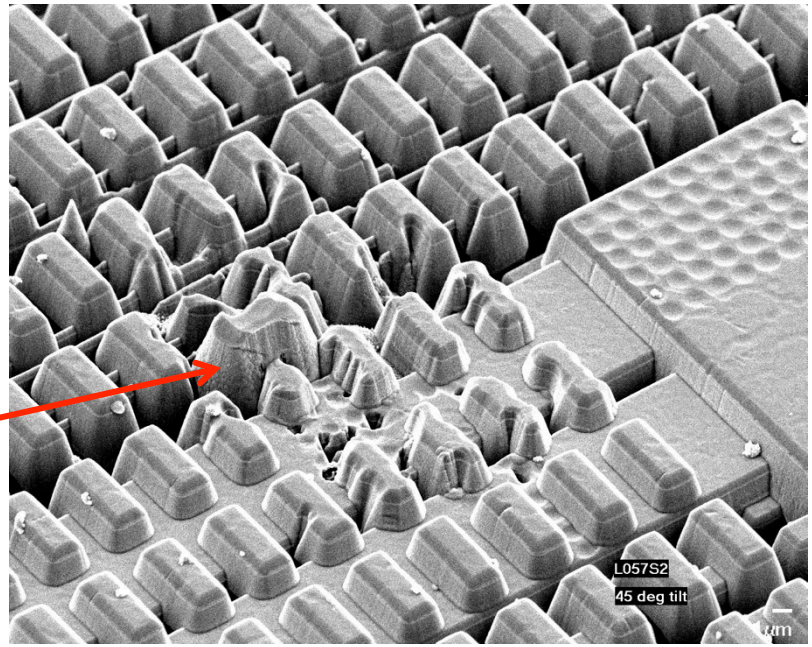
STAR PXL operation experience

- spatial position precision (alignment) < 25 µm
- hit resolution = 6.2 µm



- DCA resolution = (10 ⊕ 24/p) µm

- unexpected damage seen (on 15 ladders)
  - current limited latch-up (~300 mA)
  - shorts due to melted metal parts
  - reproduced only with Heavy Ions
  - mitigated by
    - current protection (80 mA)
    - periodic detector reset



SEM after plasma etching: metal layer appears melted

G. Contin, 10th Hiroshima Conf. , (2015)
J. Schambach, Physics Procedia 66 (2015) 514 – 519

A **BIG** step … ALICE ITS -> 2019/20

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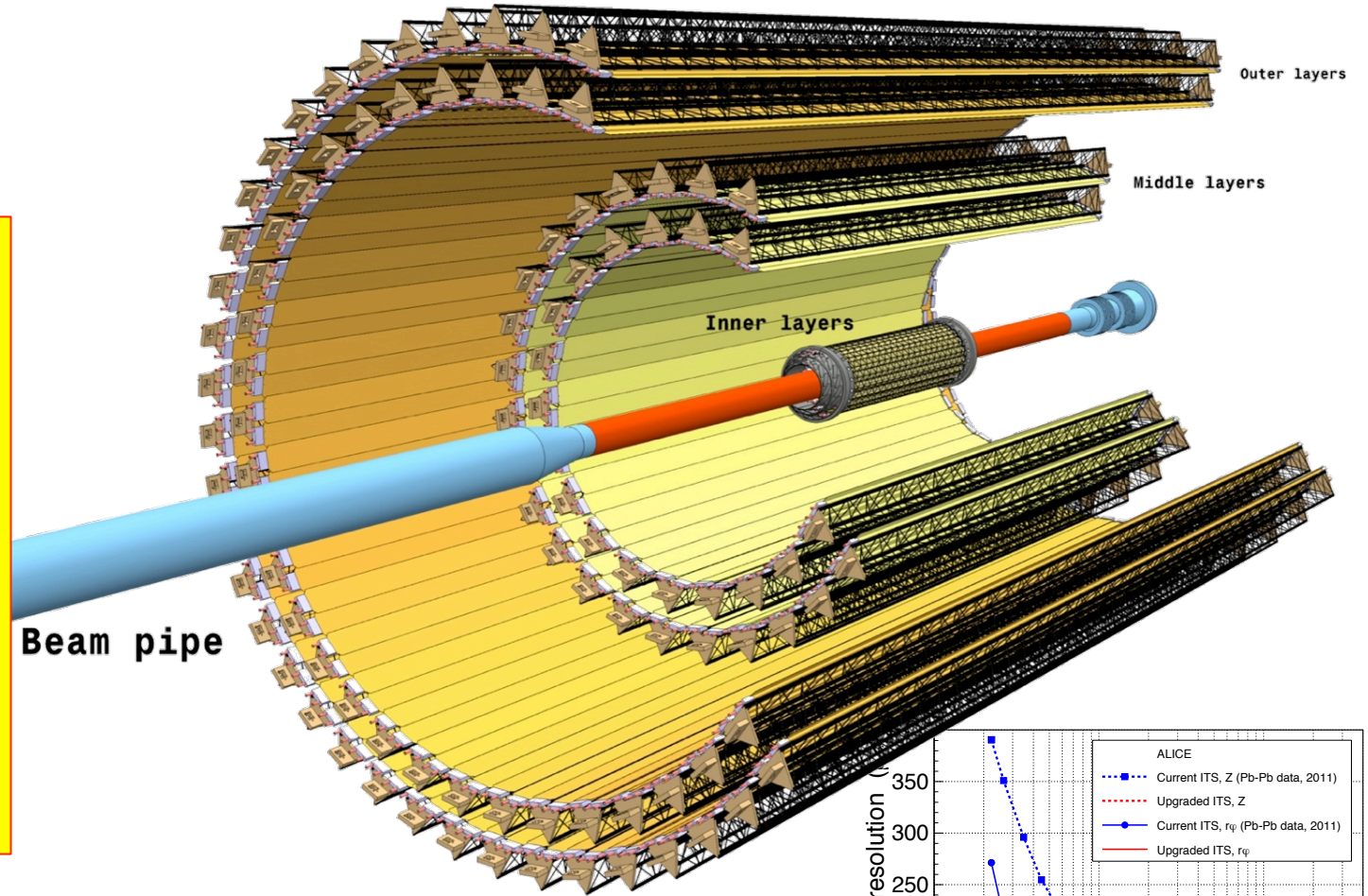
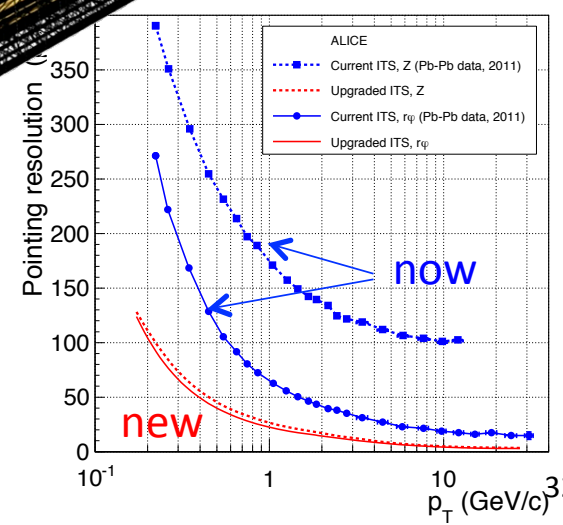
3 Inner Barrel layers (IB)
4 Outer Barrel layers (OB)

- **12.5 G pixel**
- R/O 100 kHz (now 1 kHz)

- $|\eta| \leq 1.22$
- 0.3% X_0 (IB), 1% X_0 (OB)
- **~10 m²**

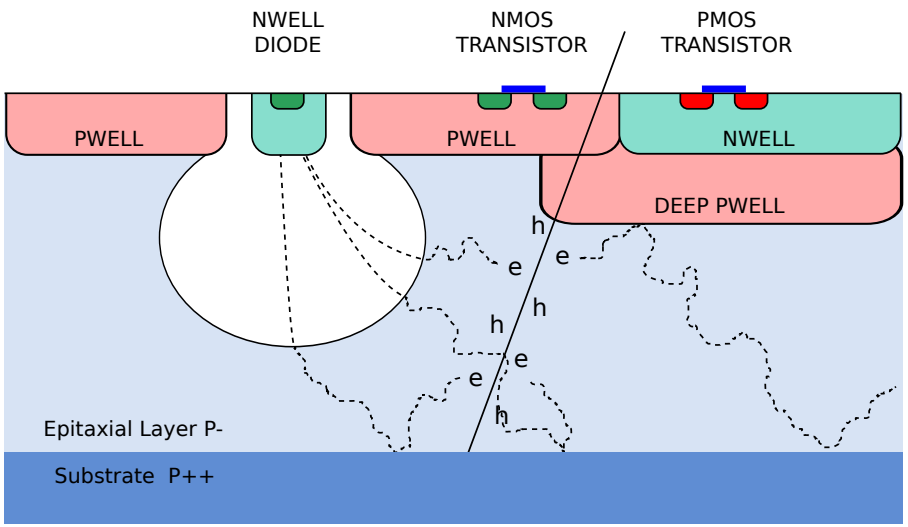
Radiation Load
- TID: ~ 2.7 Mrad
- NIEL: ~ 1.7 x 10^{13} n_{eq} /cm²





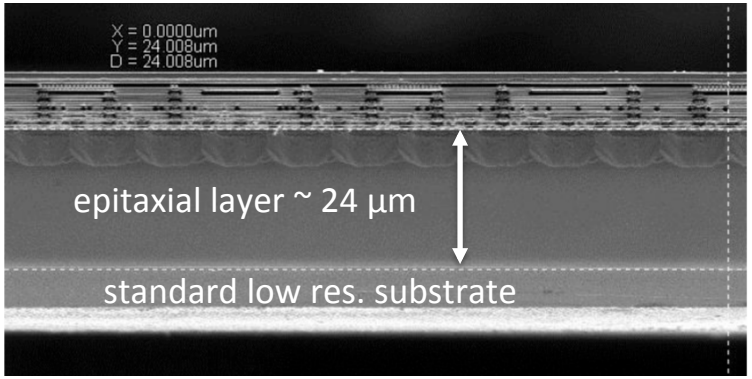
P. Riedler, QM 2015, Proceedings
L. Musa, TWEPP 2015, Proceedings

ALICE ITS: CMOS sensor: TowerJazz 0.18µm imaging process



J.P. Crooks, …, R. Turchetta et al. IEEE TNS 2007 & Sensors (2008), ISSN 1424-8820

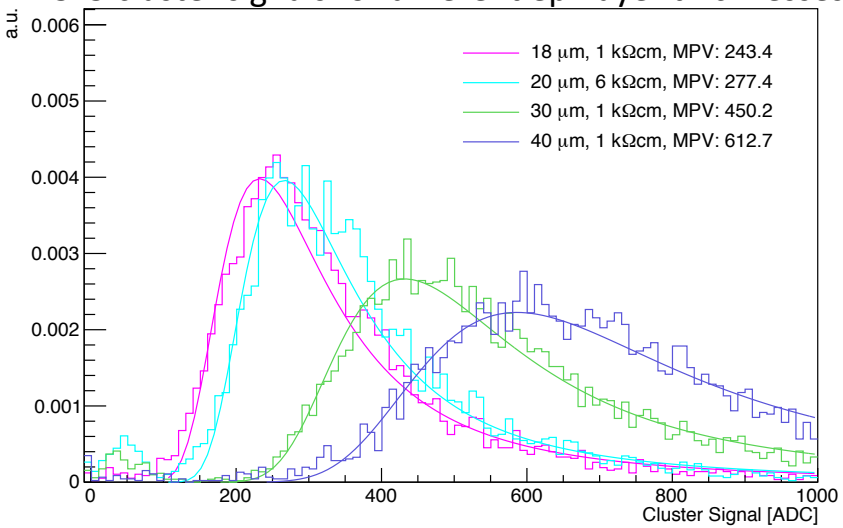
- TowerJazz 180 nm CMOS
- chip 15 × 30 mm^2 , 50 µm thin
- pixel pitch 30 µm (<5 µm resolution)



ALICE ITS, SEM picture of prototype chip

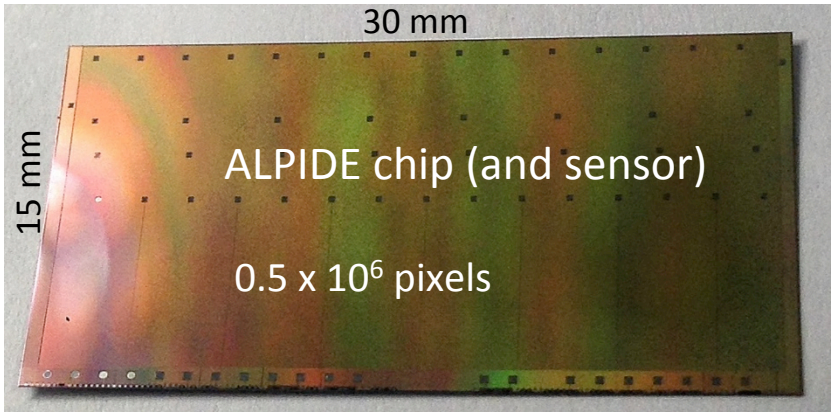
- high resistivity (> 1kΩ cm) p-type epi-layer
- "quadruple" well process => shield Nwells by deep Pwells => full CMOS
- large portion of signal obtained through drift
- very small n-well collecting diodes => small C_{in}
- moderate reverse bias => increased depletion
- radiation tolerance (TID) to 700 krad (= 1/1500 of HL-LHC-pp)

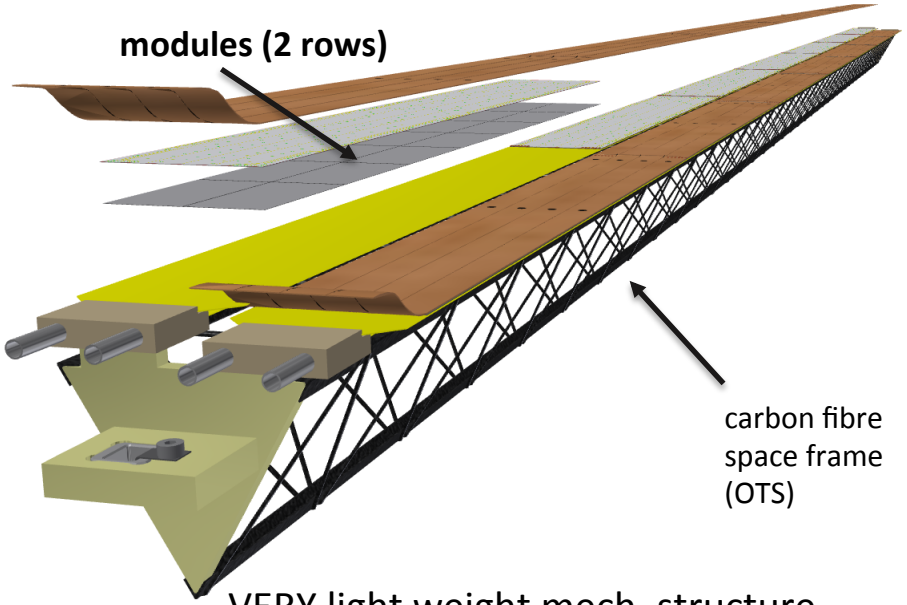
5x5 cluster signals for different epi-layer thicknesses



3.2 GeV/c electron test beam, pixel size 20 µm x 20 µm
J. Van Hoorne, PoS (TIPP2014) 125

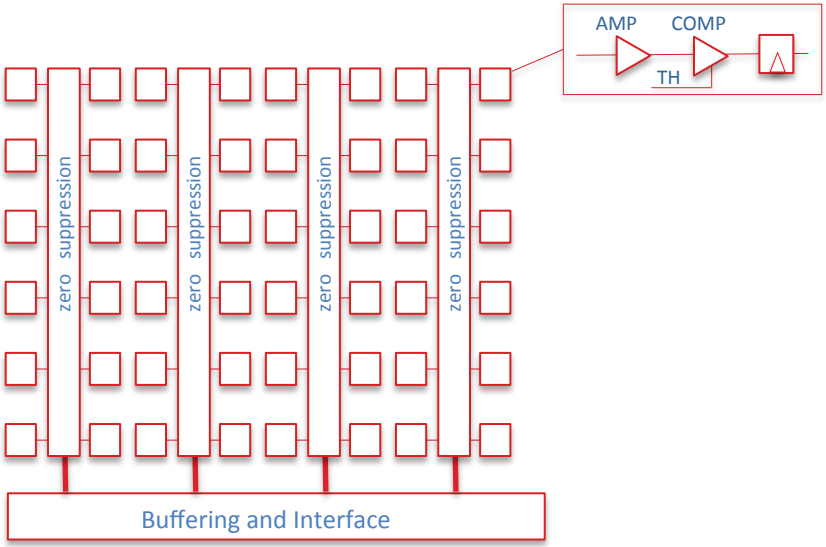
ALICE ITS Upgrade





VERY light weight mech. structure

- "Continuous" asynchronous digital R/O (sparsified)
- MISTRAL alternative ("rolling shutter")



Now: 1.14 % X_0 → 0.3 % X_0 (inner layers)

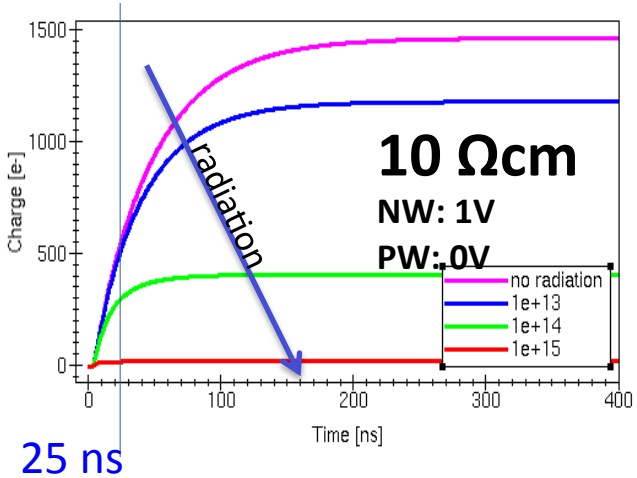
P. Riedler, QM 2015, Proceedings
L. Musa, TWEPP 2015, Proceedings

CMOS Pixels for HL-LHC -> DMAPS

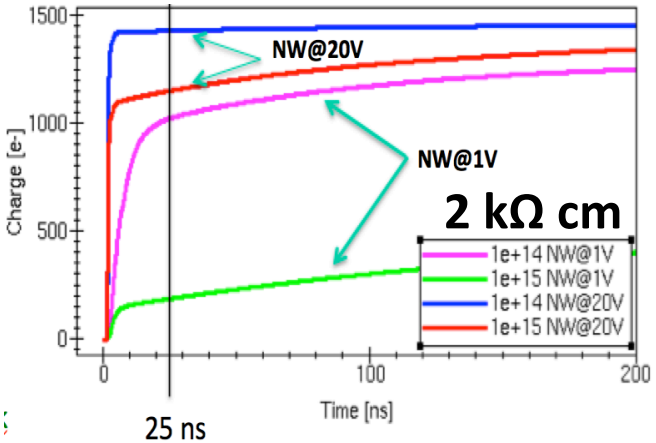
- driven by the need/hope for
  - low cost large area detectors … more pixel layers in trackers …. commercial
  - less material … ? less power … not clear
- but facing the rate/radiation challenges of the HL-LHC
- **goal:** some (40 – 80 µm) depletion depth for …
  - fast charge collection (< 25ns "in-time" efficient)
  - a reasonably large signal ~4000 e-
  - not too large a travel distance to avoid trapping (rad hardness)
- **need**

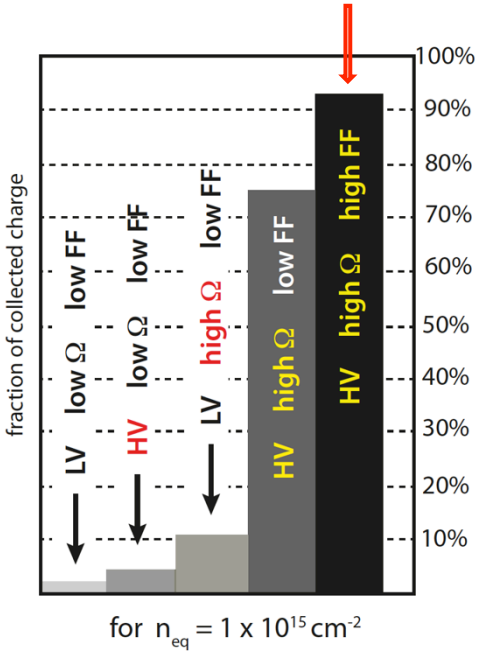
$$d \sim \sqrt{\rho \cdot V}$$

low resistivity, low voltage



high res. plus (high) voltage





from Tomasz Hemperek

Enabling technologies

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"High" Voltage add-ons

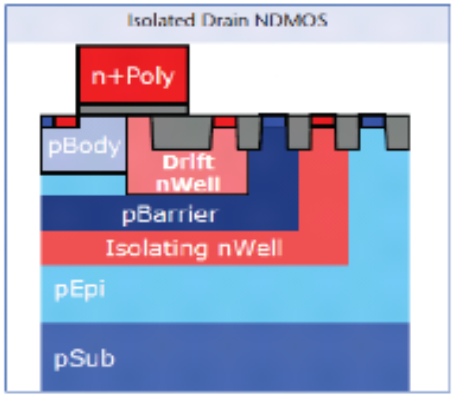
Special processing add-ons (from automotive and power management applications) **increase the voltage handling capability** and create a depletion layer in a well's pn-junction of o(10-15 µm).

"High" Resistive Wafers

8" hi/mid **resistivity** silicon wafers **accepted/qualified by the foundry**. Create depletion layer due the high resistivity.

Technology features (130-180 nm)

Radiation hard processes with **multiple nested wells**. Foundry must accept some process/DRC changes in order to optimize the design for HEP.



from: www.xfab.com

Backside Processing

Wafer thinning from backside and backside implant to fabricate a **backside contact** after CMOS processing.

ATLAS: (1) Demonstrator Program: active CMOS Pixel plus R/O Chip (still hybrid)
(2) R&D towards full monolitic DMAPS devices

Current DMAPS approaches

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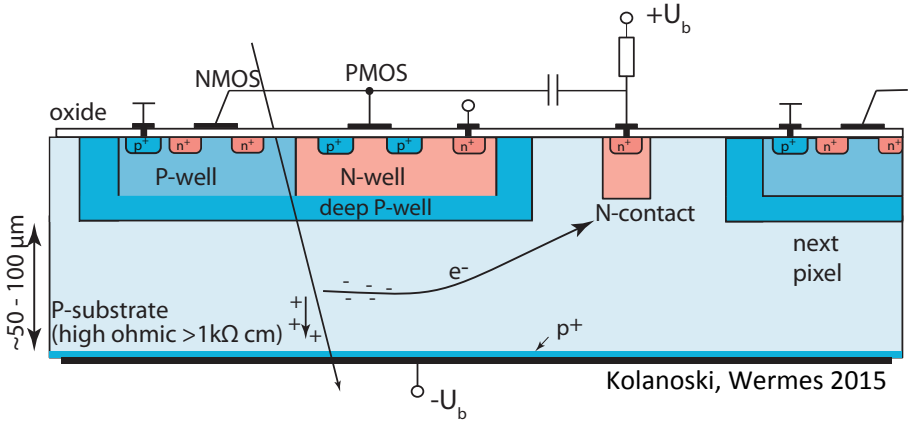
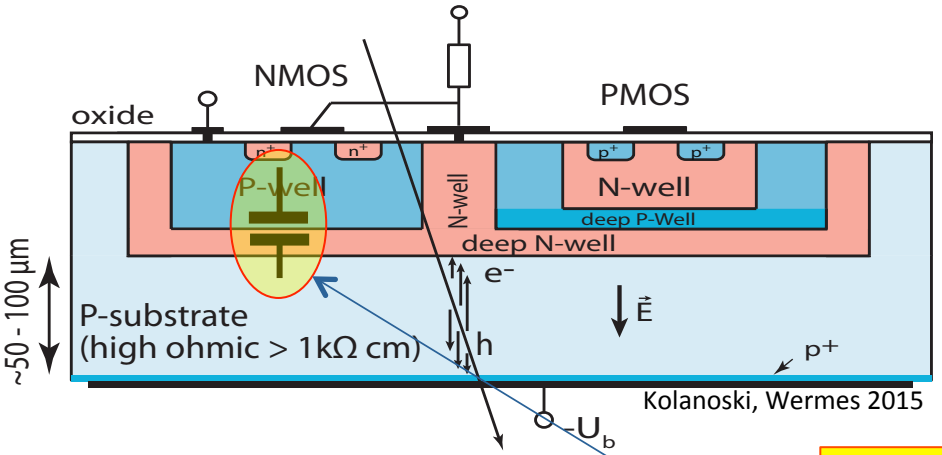
HR/HV - CMOS

I. Peric et al., NIM A582 (2007) 876-885 & NIM A765 (2014) 172-176
S. Mattiazzo, W. Snoeys et al., NIM A718 (2013) 288-291
M. Havranek, Hemperek, Krüger, NW et al. JINST 10 (2015) 02, P02013



- (D)MAPS like configuration but w/ depleted bulk
- small collection node
- long drift path

=> **smaller C, more trapping**



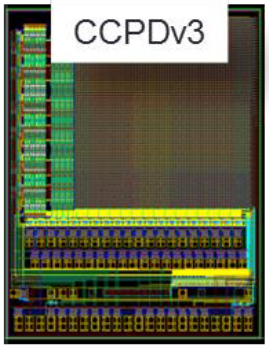
- deep n and deep p wells
- large collection node
- short drift path

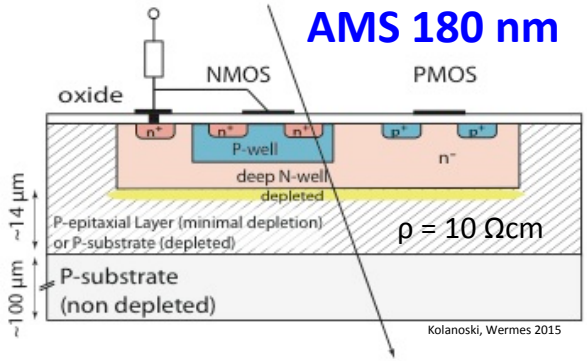
=> **larger C, less trapping**

important: (number of) deep wells and detailed cell geometry

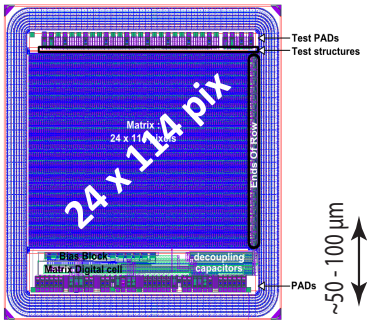
watch: capacitance between deep p- and n-wells

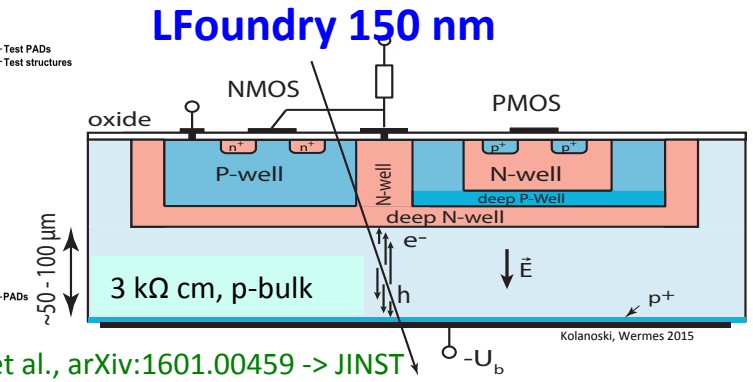
HV/HR CMOS Pixels





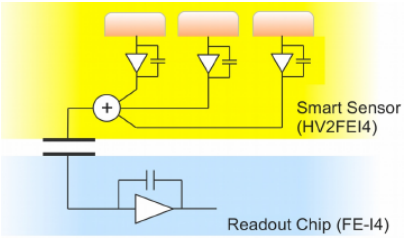
I. Peric et al., NIM A765 (2014) 172-176





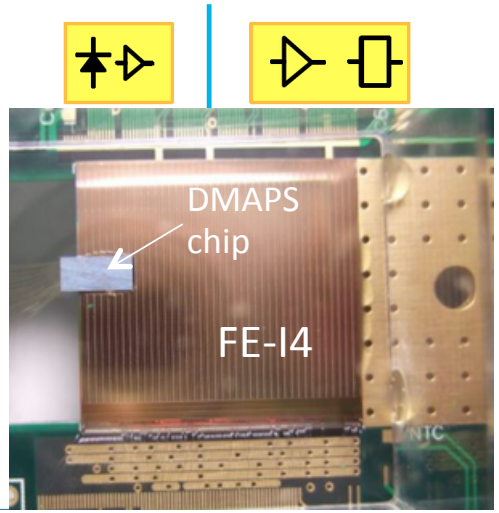
P. Rymaszewski et al., arXiv:1601.00459 -> JINST
T. Hirono et al., doi:10.1016/j.nima.2016.01.088

- triple well process
- 10 Ωcm, 60 – 100 V
- depletion depth 10-20 µm -> 100 µm after irr.
- ~1000 e- by drift
- R/O via ATLAS pixel chip (AC coupling/glue)

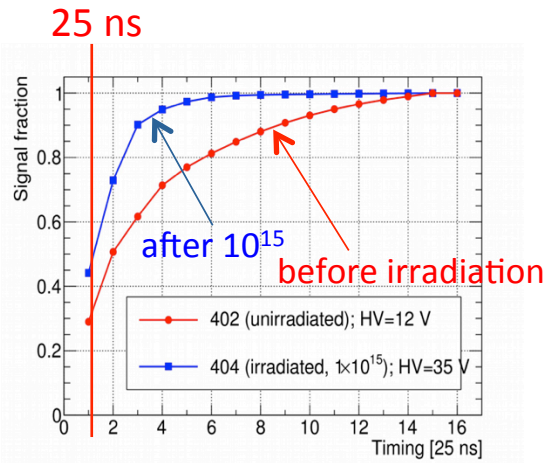


pixel area x 1/3

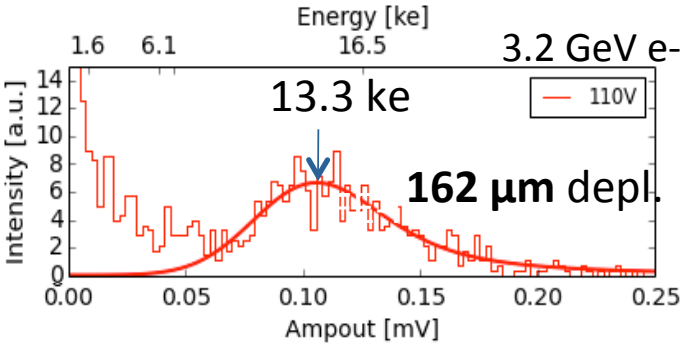
- quadruple well process
- 3 kΩ cm, 110 V bias
- large fill factor
- full CMOS (backside thinned)
- stand alone R/O and CCPD–R/O



N. Wermes, 14th VCI Wien, 2/2016



acceptor removal effect



- ❑ encouraging results
- ❑ OK > 100 Mrad and > 5×10^{15} n_{eq}
- ❑ in-time efficiency still an issue

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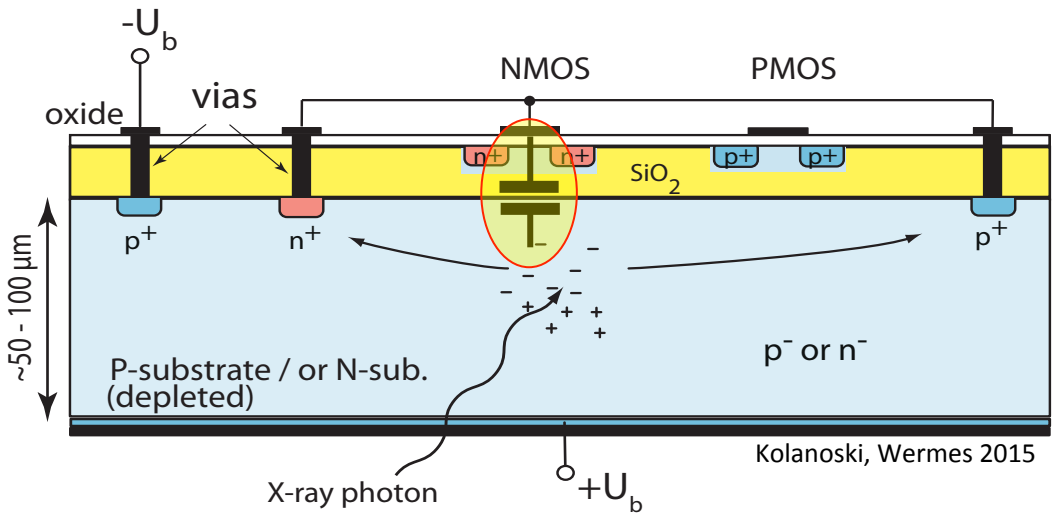
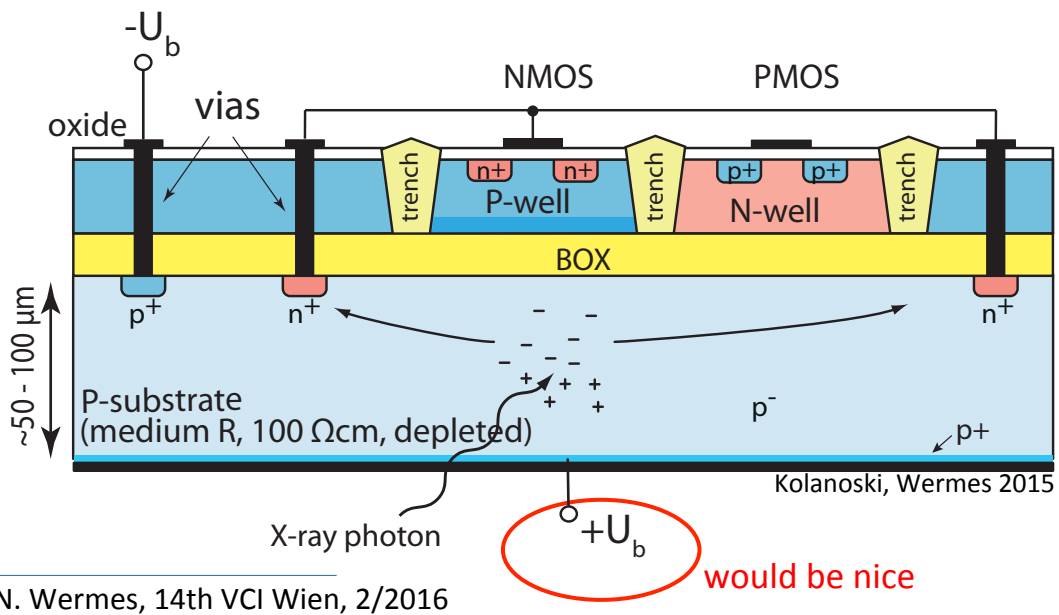
CMOS on SOI

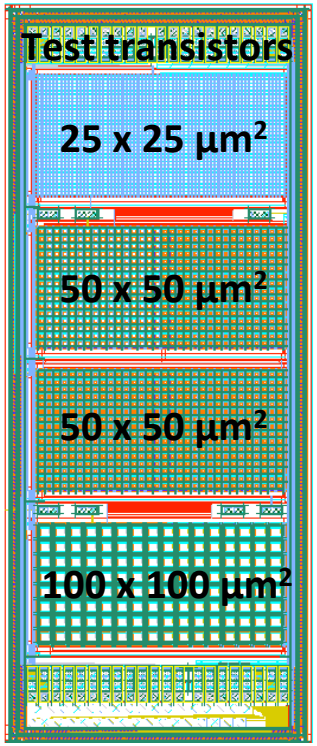


- **FD-SOI**
- OKI/LAPIS/KEK
  Y. Arai et al., e.g. NIM. A636 (2011) 1, S31-S36
- issues
  - back gate effect
  - radiation issues due to BOX
- cures invented in recent years
- proposed for ILC
- but not suited for LHC - pp



- **HV-SOI (thick film)**
  Hemperek, Kishishita, Krüger, NW,
  NIM A796 (2015) 8-12
- a promising alternative
- doped, non-depleted P- and N-wells prevent back gate effect and increase the radiation tolerance

SOI - CMOS

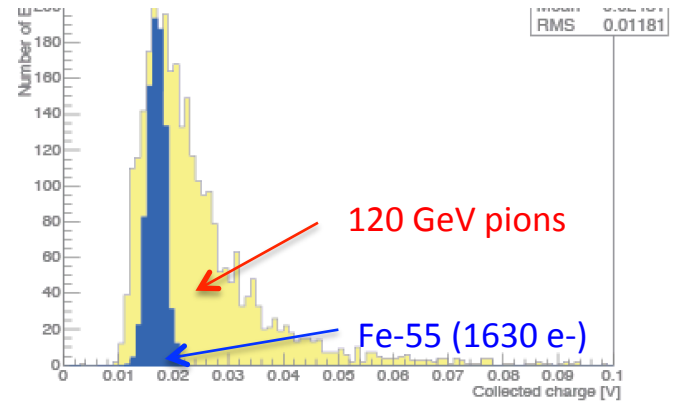


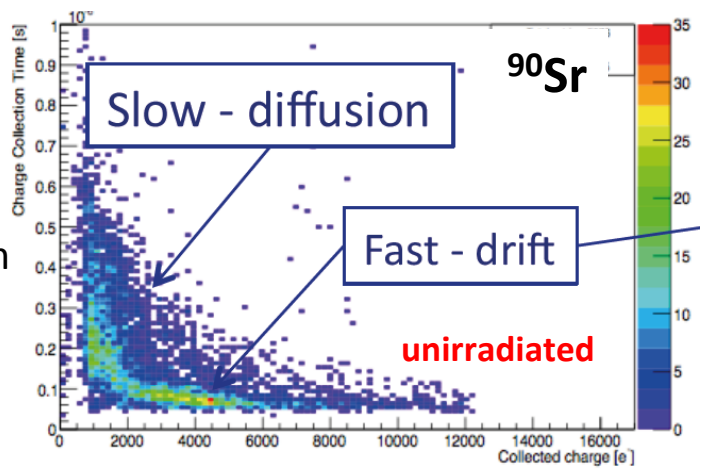
XFAB 180 nm: CMOS electronics outside collection well

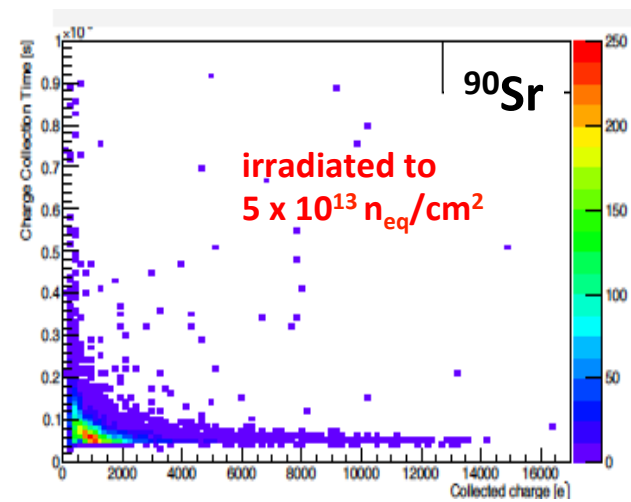
- Small charge collection well -> small C
- HV + medium-R (100 Ωcm), p bulk
- 3 T readout only

TID: 700 Mrad
up to 5×10^{14} n_{eq}/cm^2

S. Fernandez-Perez et al., NIM A796 (2015) 13-18







observation:
charge collected from high-field (fast drift) and low field (slow diffusion) regions

acceptor removal (likely) sets in => resistivity increases
=> larger "drift" - volume

❑ 4D with LGADs ?

Low Gain Avalanche Detectors

New: How to obtain fast timing with Si detectors?

- How would one go about getting into the 10 ps range with (structured) Si detectors?
- => exploit "in-silicon" charge amplification
  - in "Geiger Mode" fashion (like in gas RPCs)

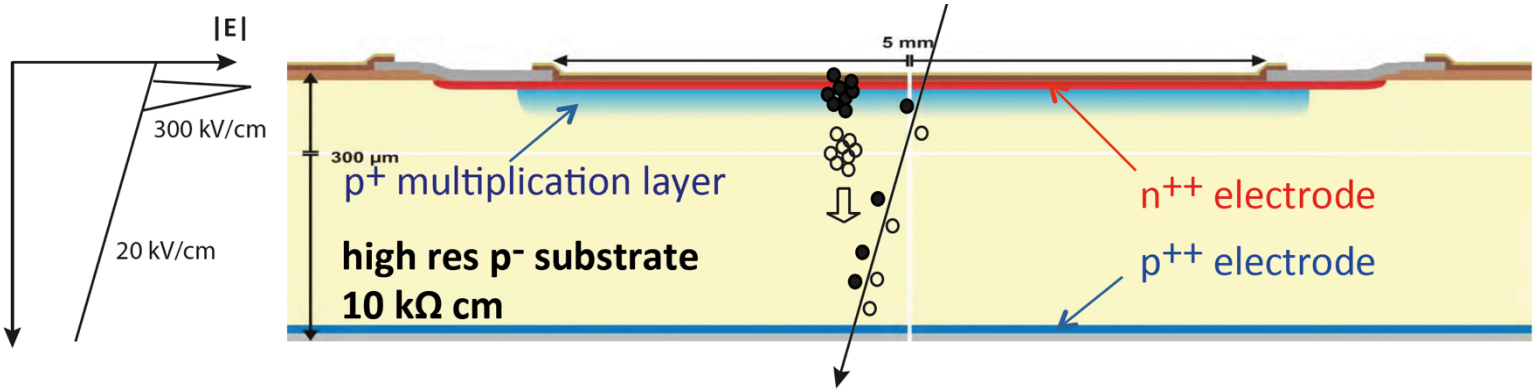
σ_t governed by avalanche fluctuations

$$\sigma_t \approx \frac{1.4}{(\alpha - \eta)\, v_D} \approx 50\text{ps}$$

Townsend coeff. attachment coeff.

see e.g. W. Riegler, C. Lippmann, R. Veenhof NIM A 500 (2003) 144

  - OR .... in "linear mode" fashion
    -> Low Gain Avalanche Detectors



see N. Cartiglia Parallel 2

H. Sadrozinski et al., NIM A730 (2013) 226-231
N. Cartiglia et al., JINST 9 (2014) C02001
A. Seiden et al, Vertex2015, Proceedings

Towards 4D tracking ... Low-Gain Avalanche Detectors

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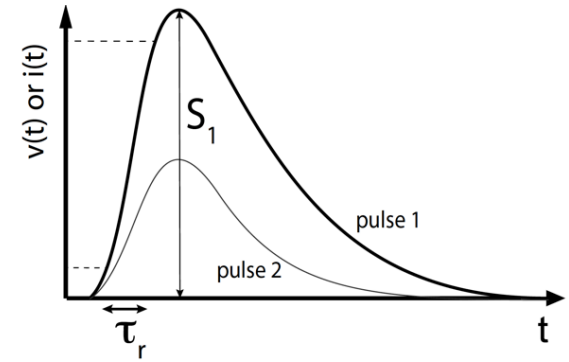
- Separate the "collection" of charge from the signal gain
- Figure of merit for σ_t is the "slew rate" dV/dt ≈ Signal/τ_{rise}

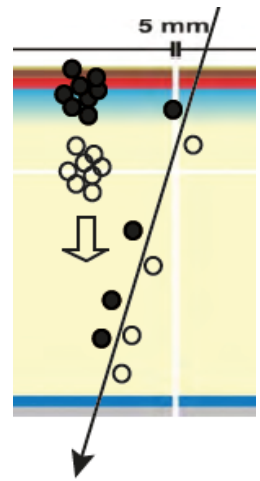
$$\sigma_t^2 = \underbrace{\left(\frac{V_{th}}{dV/dt}\Big|_{rms}\right)^2}_{\text{signal time walk}} + \underbrace{\left(\frac{\text{Noise}}{dV/dt}\right)^2}_{\text{noise time jitter}} + \underbrace{\left(\frac{TDC_{bin}}{\sqrt{12}}\right)^2}_{\text{TDC binning}}$$

can be made negligible

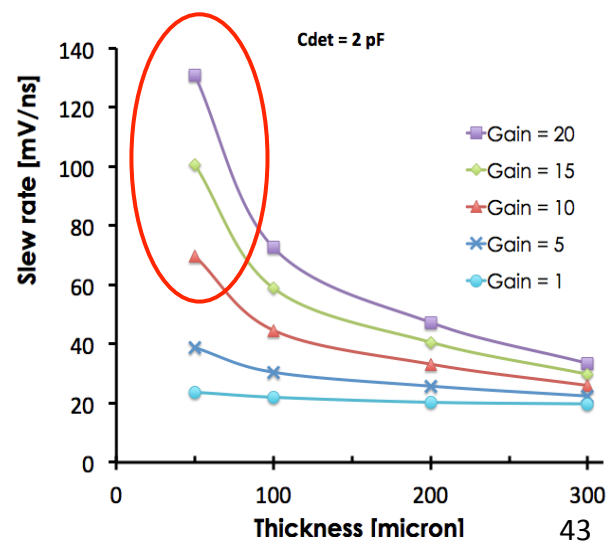


Need: fast drift - large signals – low noise

- e- drift in sat. (E = 20 kV/cm, $v_D \approx 10^7$ cm/s) => HV
- collect electrons fast => thin
- get large signals => from amplified holes (!)
- small C, small i_{leak}, low noise => small electrodes
- broad-band (non-CSA) amplifier & e.g. CF discr.



$$i_S = q\vec{E}_w \cdot \vec{v}$$

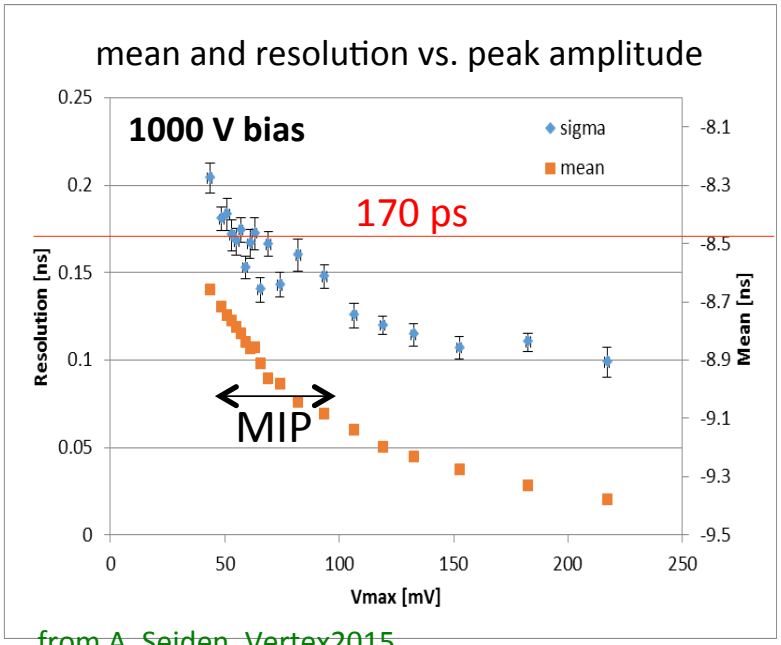


- Ultimate Goal: simultaneous space (~10µm) and time resolution (< 50 ps) -> pile-up killer

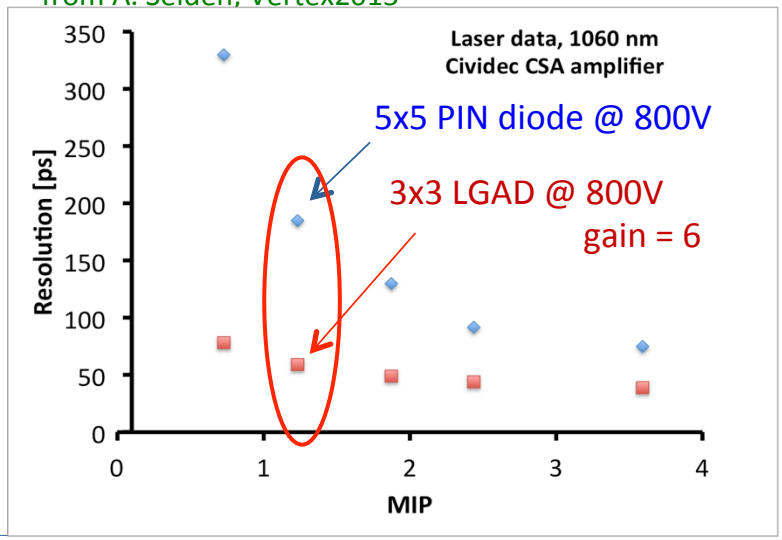
- Options for ATLAS (HighGranularityTimingDetector; Forward) and CMS-TOTEM (in Roman Pots)

LGAD – development starting with PAD detectors

- LGAD pad detectors

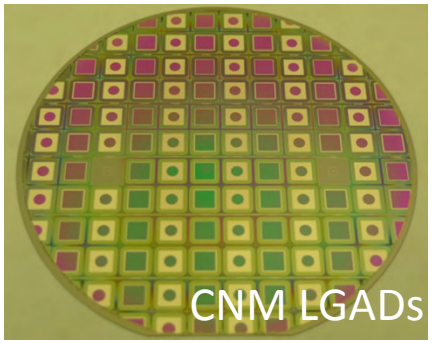


from A. Seiden, Vertex2015



<= CNM 8x8 mm²
300 µm thick, 11 pF

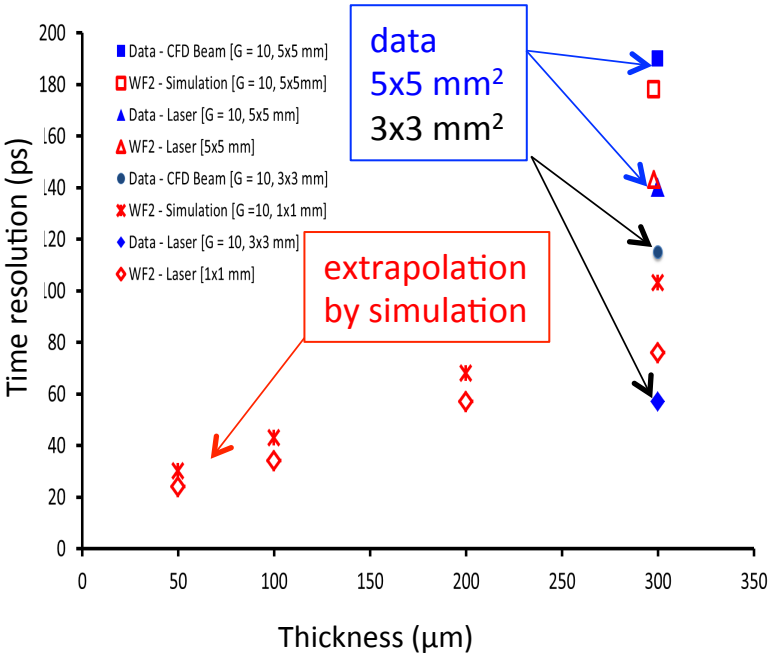
in 120 GeV pion beam



G. Pellegrini et. al, NIM A 765 (2014) 12–16.
G. Pellegrini et al., HSTD 2015, arXiv:1511.07175

<= CNM 3x3 mm²
300 µm thick, 3 pF

in Laser Setup



Conclusions

- Silicon detectors are the working horse for tracking detectors in high rate and radiation environments and the choice for high energy pp-exp's future

- Community is setting out to address their weak points
  - material
  - cost and area coverage
  - integration
  - 4D

Apologies for not having covered ...

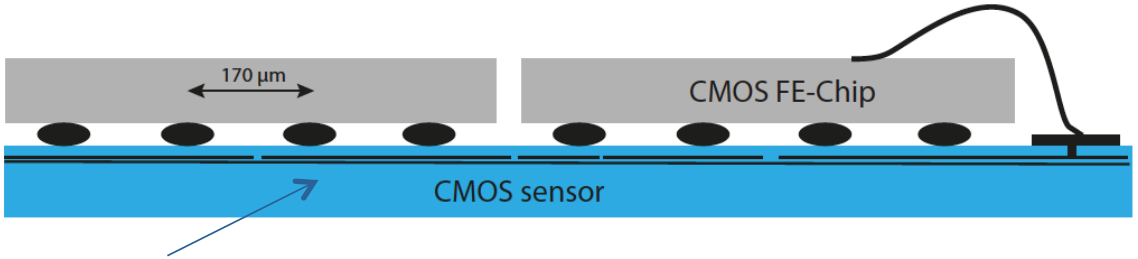
- X-ray imaging sensors (e.g. 4-side butt. Medipix)
- SDD: Si-drift detectors
- Advances in low mass support structures
- CMOS microstrip development
- Mu3e – CMOS Pixels
- Passive CMOS Pixels
- Microchannel cooling
- Active edge sensors
- Random Ghost Hits (CMS)
- TSV progress and 3D integration
- SiPM developments
- ... and many more

Thanks to many colleagues having contributed material and w/ discussions, esp. M. Moll, G-L. Casse, H. Sadrozinski, F. Hügging

BACKUP

For the very cheap & large area .... passive CMOS pixels

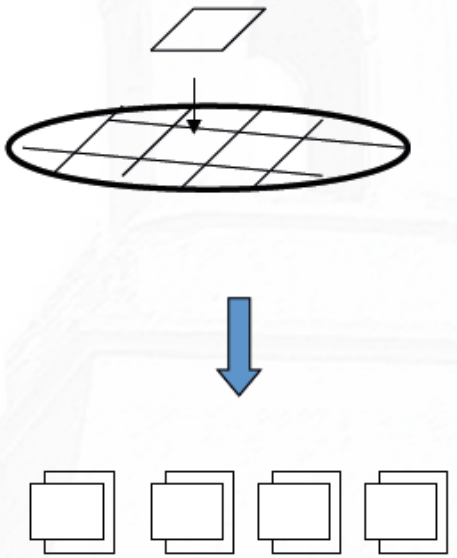
universitätbonn

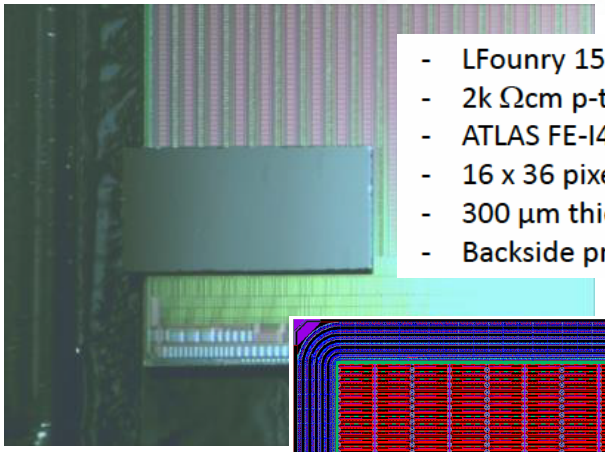


C4 bumps: come with chip fabrication at low cost

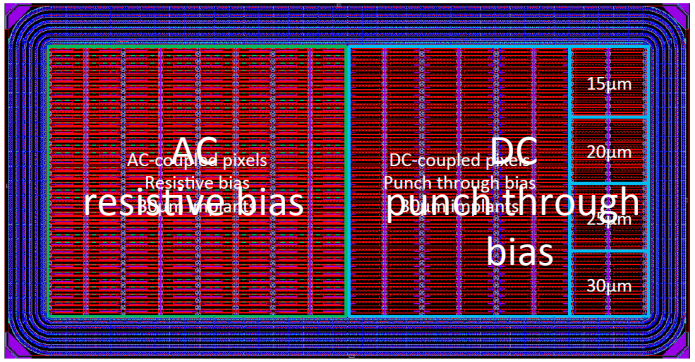
- no bumping
- do flip-chipping in-house (large pitch)
- cheap large feature size technology
- large sensors (reticle stitching)
- wafer based flip-chipping (8“)
- can have in-pixel AC coupling
- fancy RDL possibilities by metal layers (watch C !)

- Question: how good are these CMOS sensors?



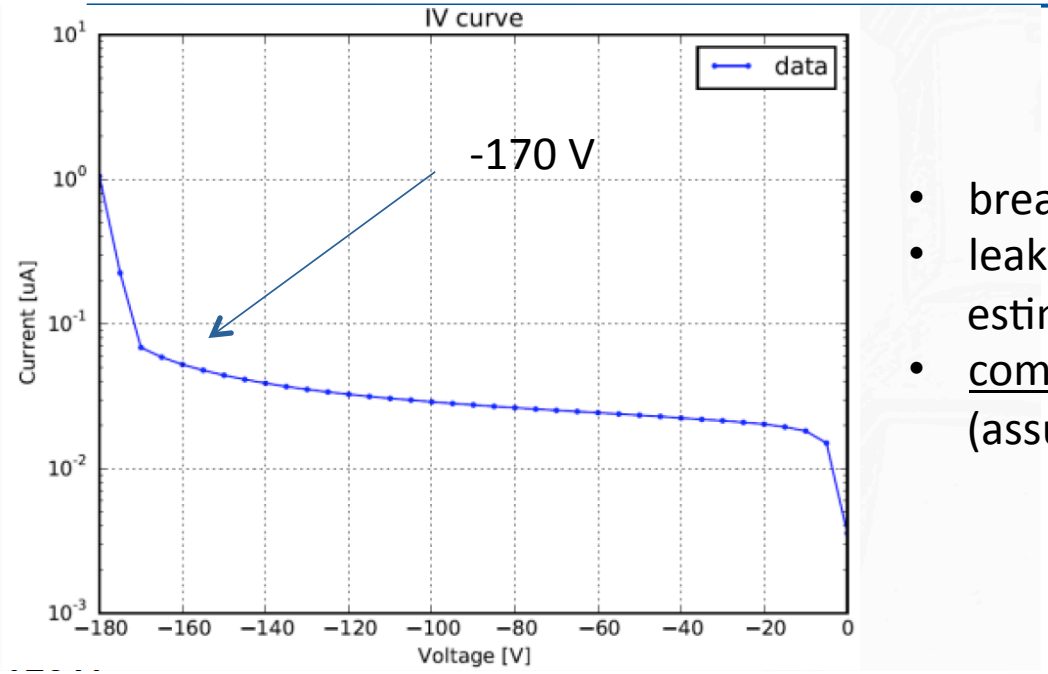


- LFounry 150 nm CMOS technology
- 2k Ωcm p-type bulk
- ATLAS FE-I4 pixel size (50 µm x 250 µm)
- 16 x 36 pixel
- 300 µm thick
- Backside processed

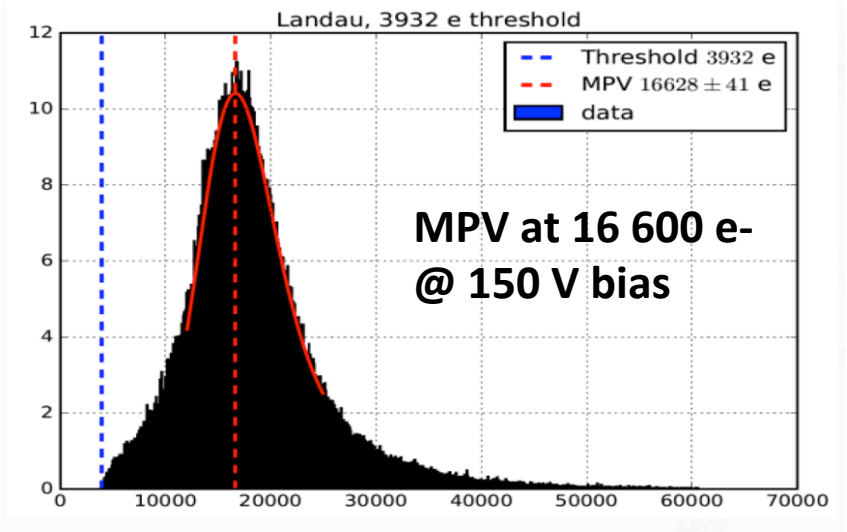


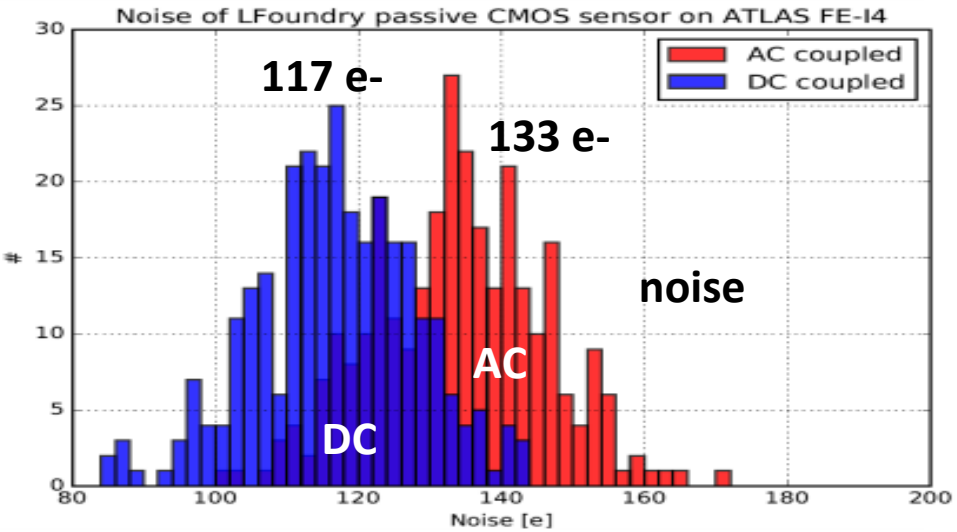
T. Hemperek, F. Hügging, H. Krüger, L. Gonella, J. Janssen, D. Pohl (UBonn), NW
A. Macchiolo (MPI M)

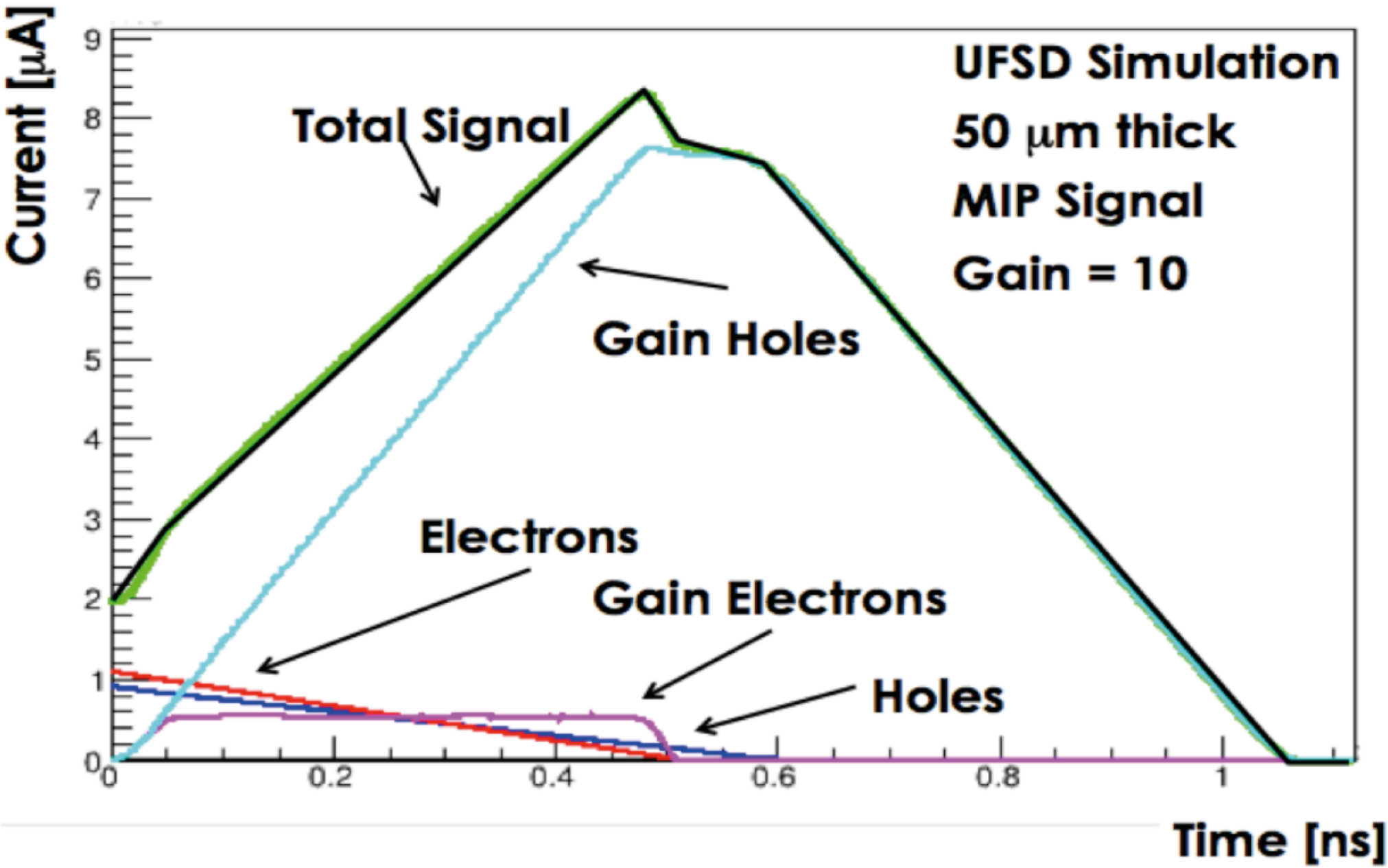
some initial results



- break down at 170 V
- leakage 20 µA / cm³ (assuming 220 µm depletion, estimated from simulation and indep. measurements)
- compare: planar sensor ATLAS IBL: 15 µA/cm³ (assuming 200 µm depletion depth)






UFSD Simulation
50 μm thick
MIP Signal
Gain = 10
Total Signal
Gain Holes
Electrons
Gain Electrons
Holes
Current [μA]
Time [ns]
0
1
2
3
4
5
6
7
8
9
0
0.2
0.4
0.6
0.8
1