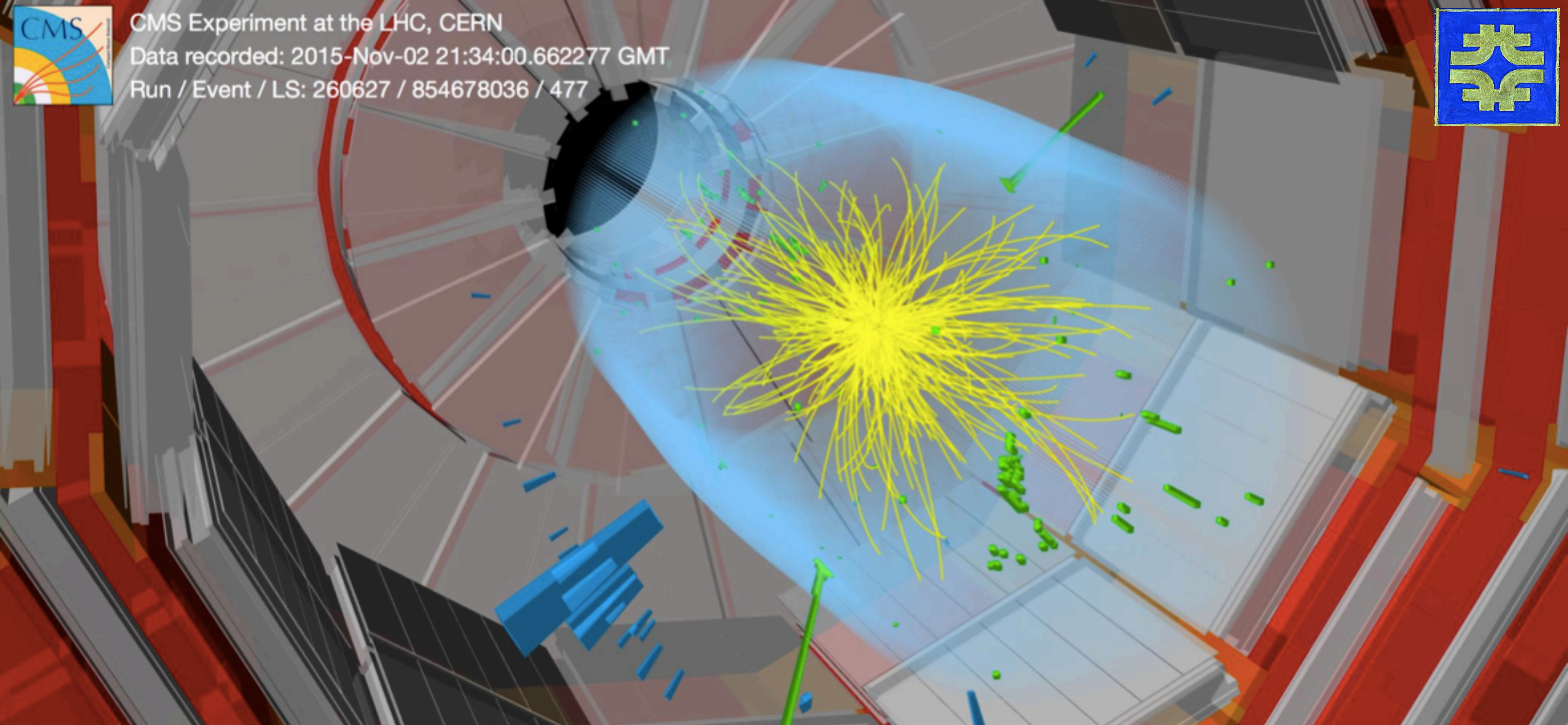


Level-1 Track Trigger for CMS in HL-LHC

Sergo Jindariani (Fermilab)

Mark Pesaresi (Imperial College)

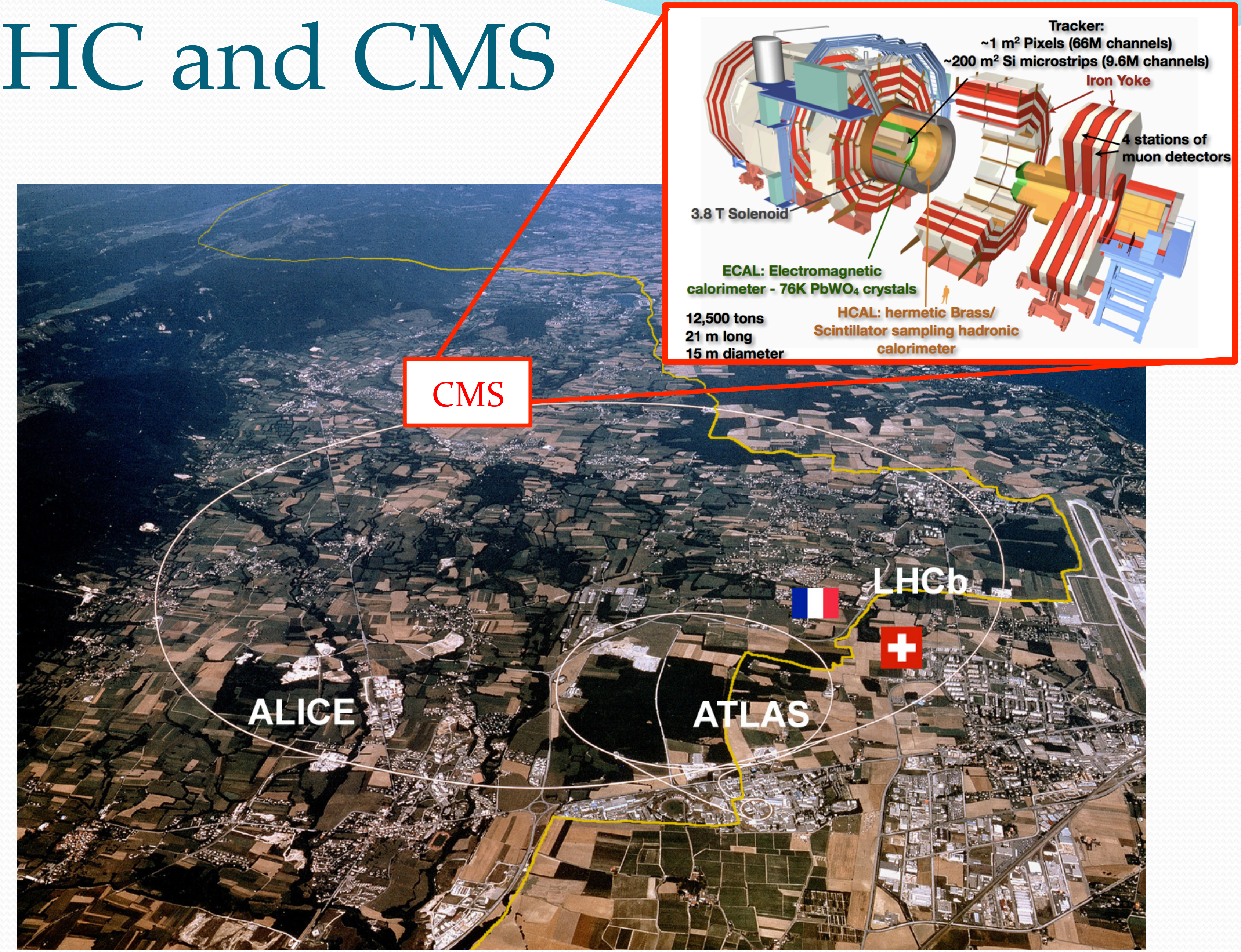
on behalf of the CMS collaboration

Vienna Conference on Instrumentation, February 2016

Outline

- Why Level-1 (L1) tracking trigger ?
- Challenges of implementing L1 track trigger at LHC
- Overview of current R&D efforts.
- Roadmap

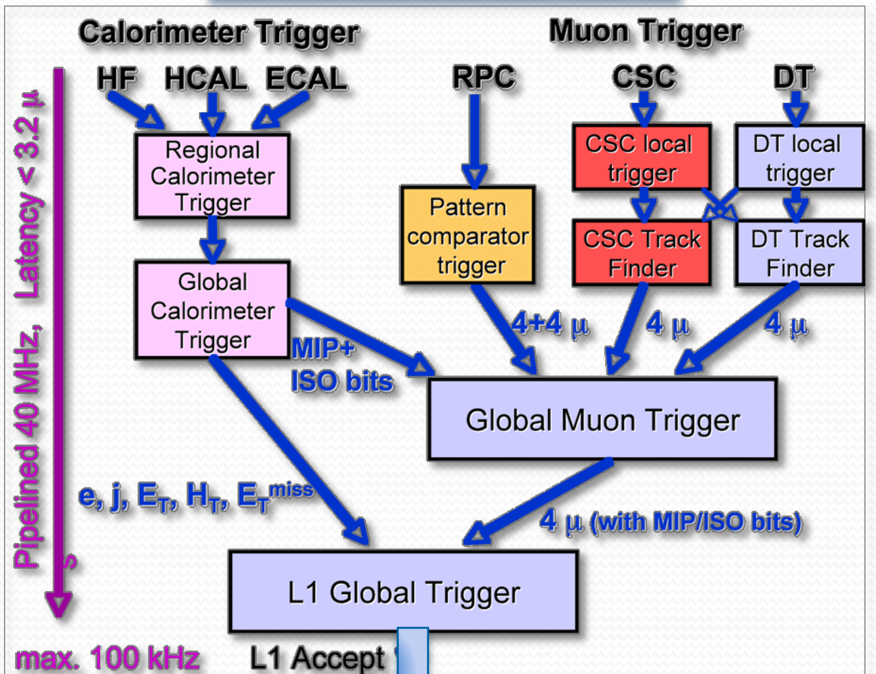
LHC and CMS



Tracker:
~1 m² Pixels (66M channels)
~200 m² Si microstrips (9.6M channels)
Iron Yoke
4 stations of muon detectors
3.8 T Solenoid
ECAL: Electromagnetic calorimeter - 76K PbWO4 crystals
12,500 tons
21 m long
15 m diameter
HCAL: hermetic Brass/ Scintillator sampling hadronic calorimeter
CMS
LHCb
ALICE
ATLAS

Current CMS trigger

Level-1 Trigger



High Level Trigger

Tracker Data

Data Storage

40 MHZ

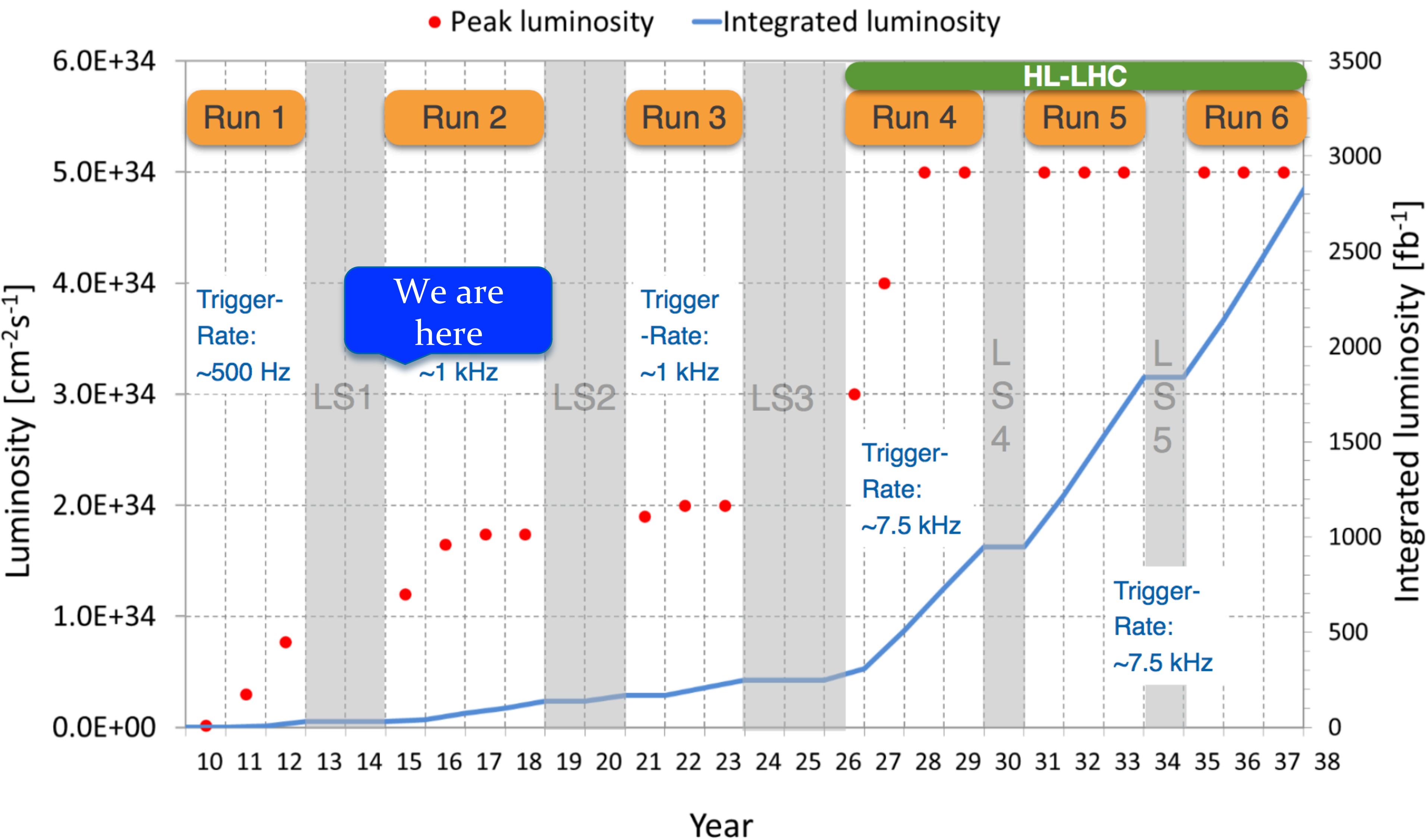
100 kHZ

~1 kHZ

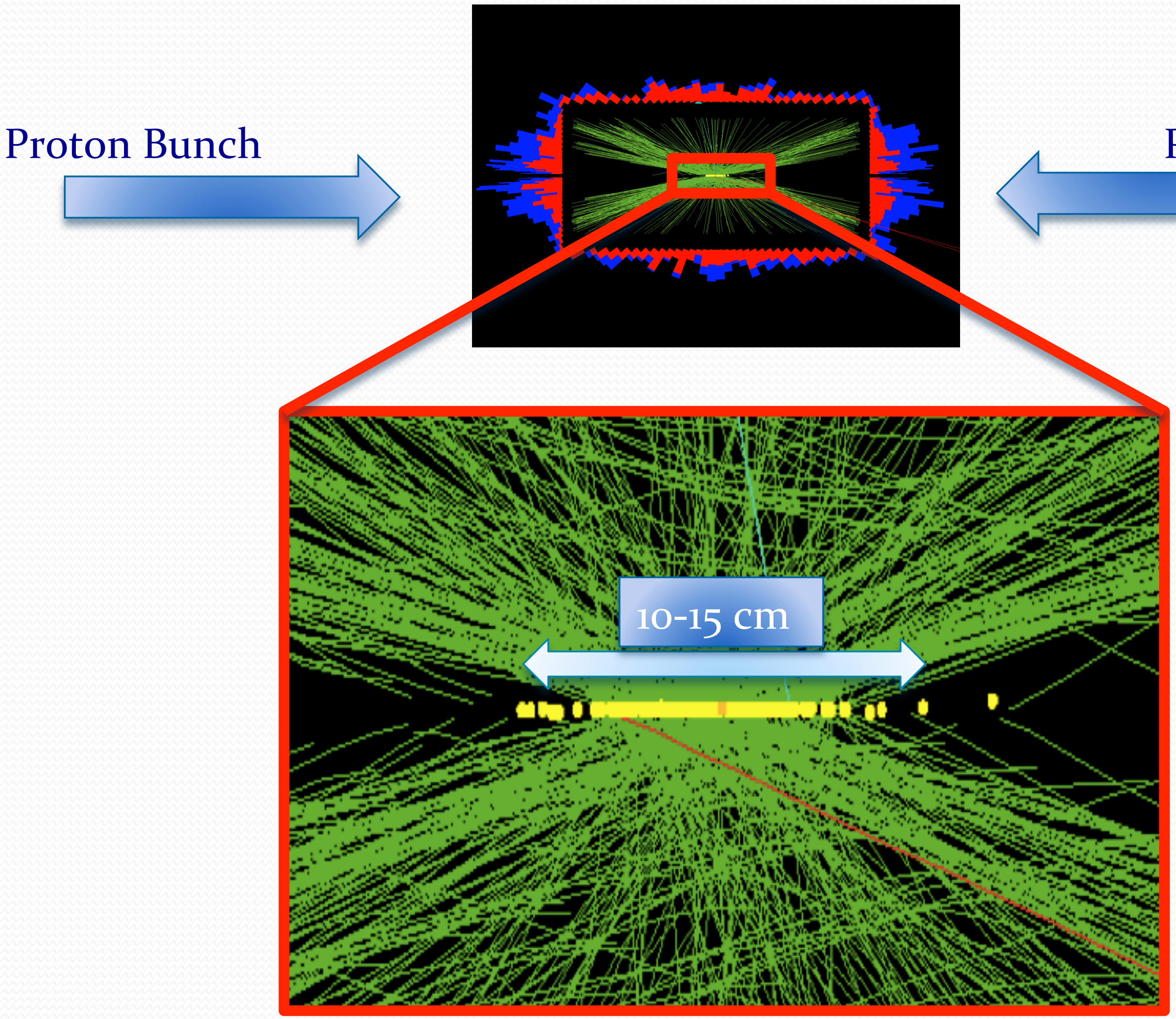
- L1 trigger system reduces event rate from 40 MHz down to 100 kHz
- Until HL-LHC, Level-1 decision is based solely on calorimeter and muon system information
- Tracker data available at the HLT level only

LHC timeline

Trigger rates are shown for the High-Level Trigger



Pile-up



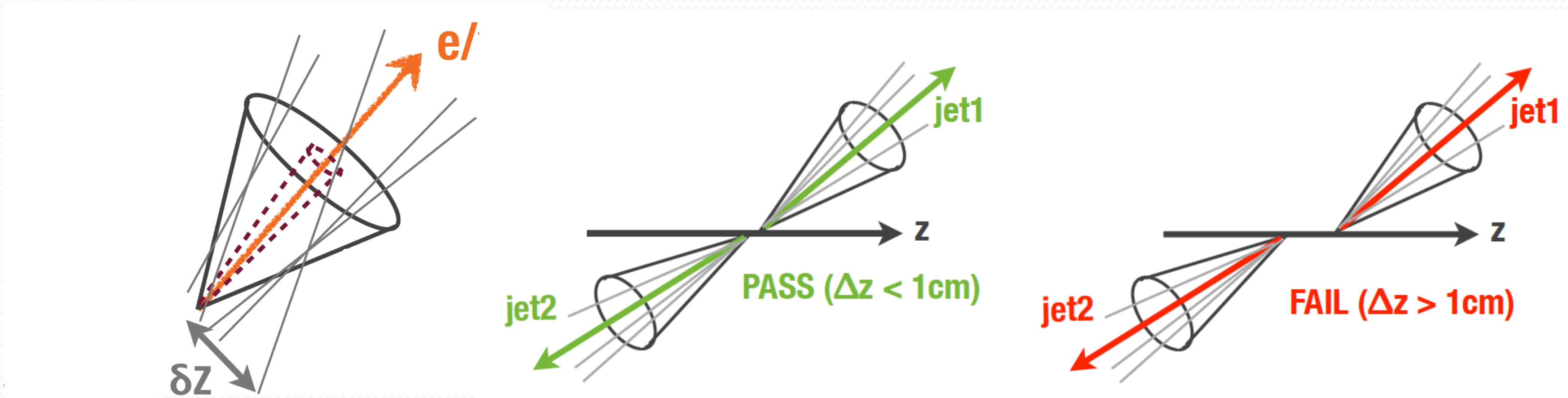
Shown: 78 collisions in one bunch crossing

Expect up to 200 in HL-LHC

Tracking in L1 trigger:

Tracking is highly effective for pileup mitigation

- Electron/Photons
  - Extra measurement – Rate Reduction
  - Isolation
- Muons
  - Excellent Pt Resolution
  - Isolation
- Tau Triggers
  - Multiprong
- Separation of Interactions
  - Hadronic/Multi-object Triggers
  - Track-based Missing Energy

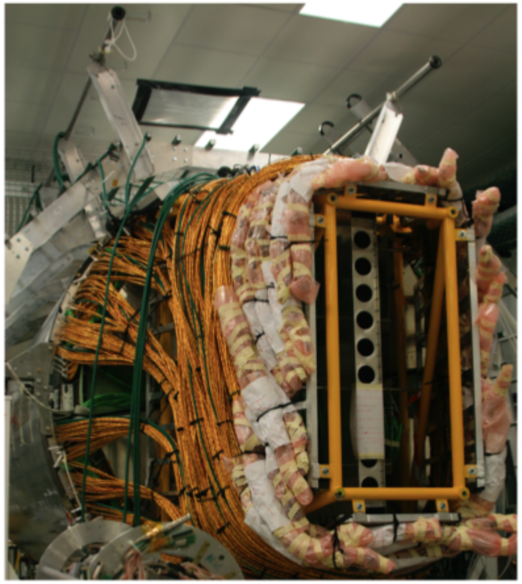


Scale of the problem

Sheer amount of data in collisions:

- Bunch Spacing = 25 ns i.e. 40 million bunch crossings per second
- Up to 200 interactions per bunch crossings
- Several particles per interaction
    - **=> Reconstruct billions of particles per second**

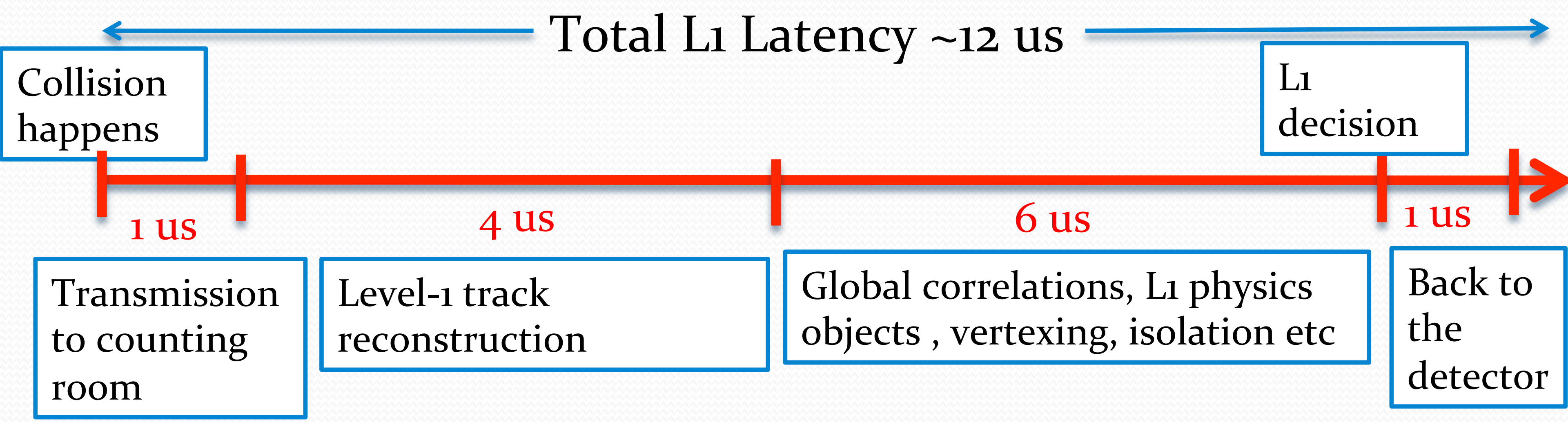
Challenge 1:



Up to 1 Pb/s bandwidth needed (50-100 Tbs after soft track suppression)

Scale of the problem

Challenge 2:

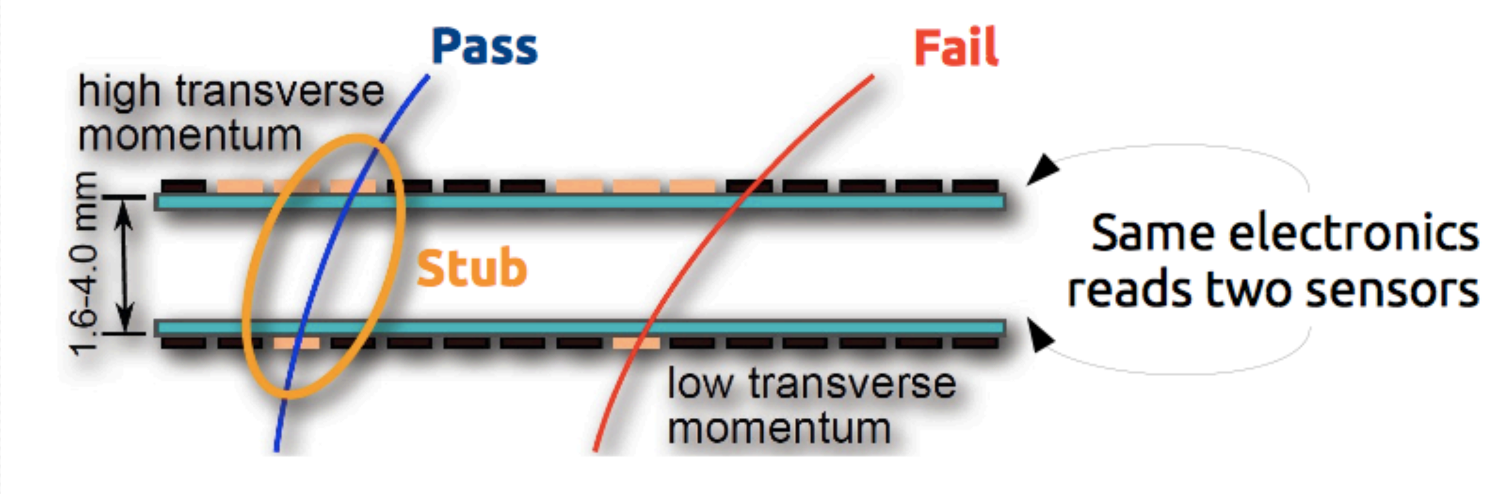


Tracks have to be reconstructed in < 5 us

New CMS Tracker

More on the tracker in the talks by Giacomo SGUAZZONI and Axel KONIG (Wednesday)

Tracker design is from the ground up done for triggering



- Stub = pair of clusters in the 2 sensors of a module within a predefined strips window (enabling pT cut at the module level).
- Pass/Fail window is programmable (2 GeV default cut)
- Stubs drastically reduce (by a factor 10-20) the amount of data to extract from the tracker @40MHz
- Stubs allow L1 tracking possibility

- ~15000 modules transmitting
  - p_T-stubs to L1 trigger @ 40 MHz
  - Full tracker readout @ 750 kHz

General Strategy

Data transfer

Partition detector into trigger towers

Associative Memory (AM)
Hough Transformation
Tracklet-based
…

Fit filtered hits in FPGA to determine track parameters

Data formatting

Pattern Recognition

Track Fitting and duplicate removal

Tracks out

$\Delta t1$

$\Delta t2$

$\Delta t3$

Total processing Latency Δt ?

Approaches

Need to handle the high occupancy and combinatorics that result from there (faster than linear scaling) . Done using:

- data partitioning (tracklets)
- Hough transform (TMT)
- Associative Memory (AM+FPGA)

Hardware:

FPGA-only (Tracklets and TMT): perform both pattern recognition and track fitting in FPGA:

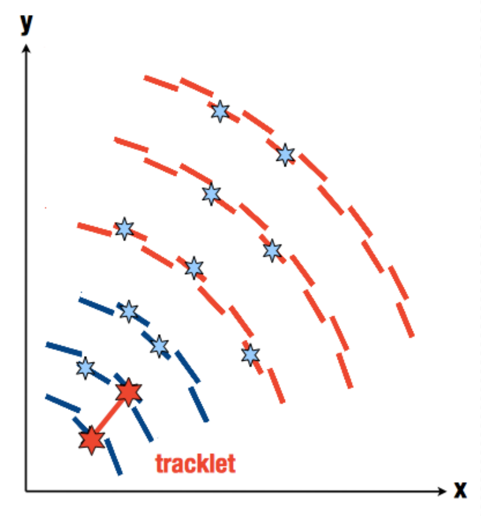
- Can be done using conventional hardware (FPGA)
- challenging to fit within FPGA resources and the latency budget

Associative Memory (AM) based: Use AM for pattern recognition followed by track fit performed in an FPGA.

Proven: CDF SVT and ATLAS FTK (in progress), but not at L1
Requires custom ASIC

Tracklet Based Approach

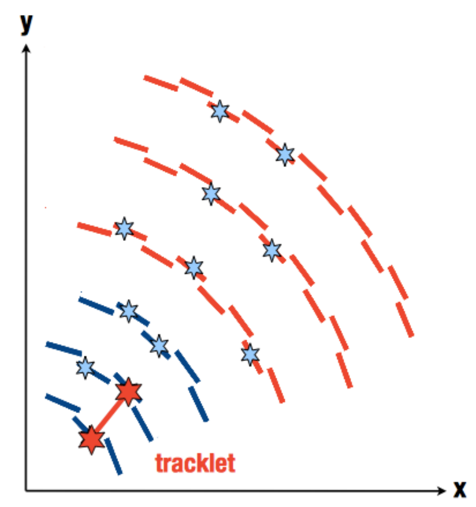
Tracklet based approach

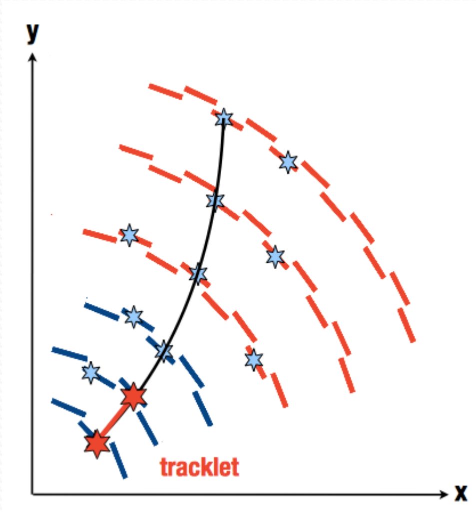


Seeding:

- Form tracklets from pairs of stub in adjacent layers
- Use beamspot constraints
- Tracklet must be consistent with Pt and z0 requirements

Tracklet based approach

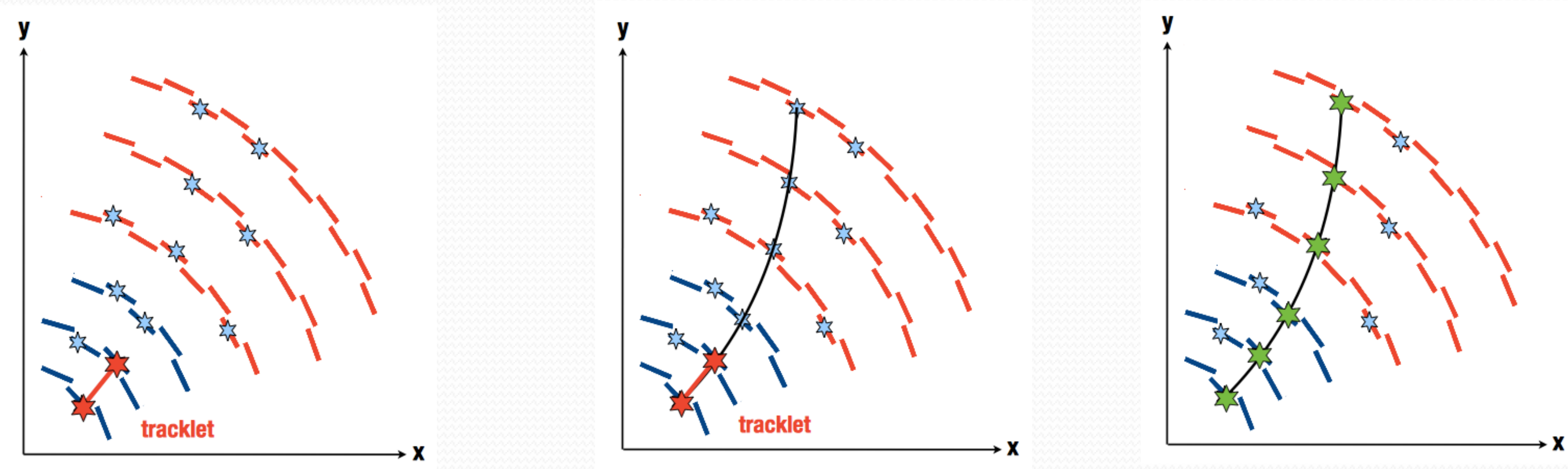




Seeding:
- Form tracklets from pairs of stub in adjacent layers
- Use beamspot constraints
- Tracklet must be consistent with Pt and z0 requirements

Projecting:
- Project to other layers and disks
- search window derived from residuals b/w projected tracks and stubs
- In-out & Out-in

Tracklet based approach



Seeding:
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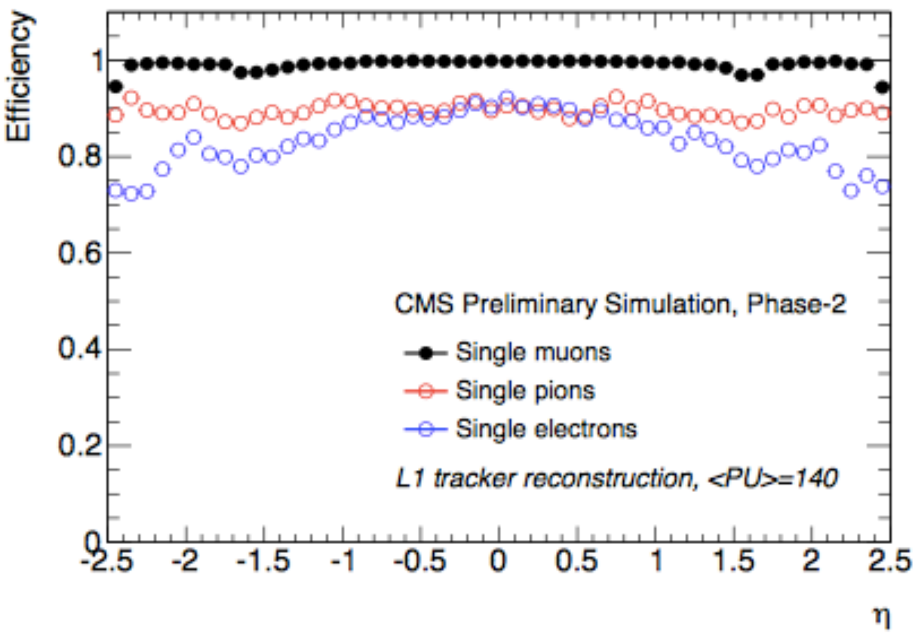
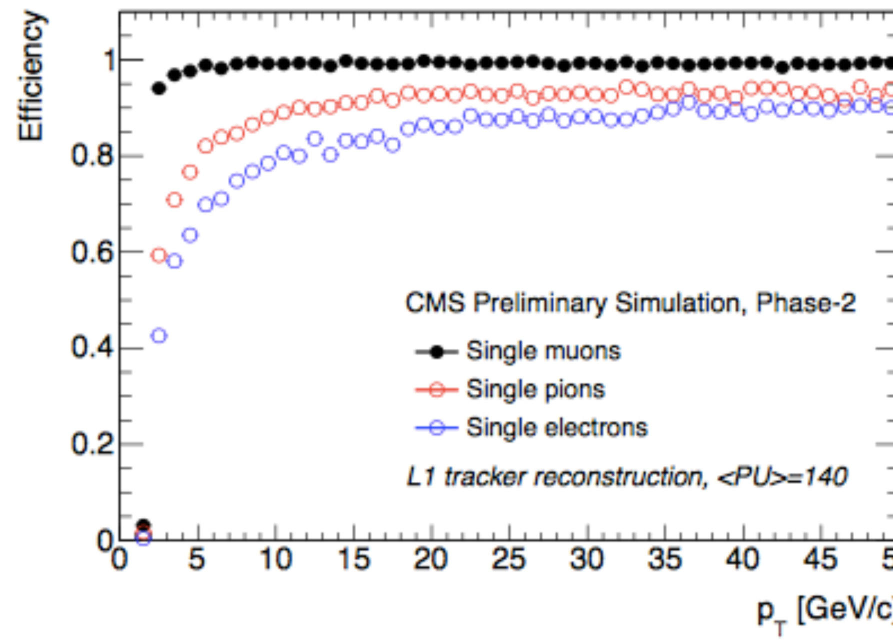
Projecting:
- Project to other layers and disks
- search window derived from residuals b/w projected tracks and stubs
- In-out & Out-in

Fitting
- linearized track fit

Duplicate Removal:
Based on number of shared stubs

Performance in Simulation





- Muons: Sharp turn-on at 2 GeV & high efficiency across all η. Eff ~99%
- Pions: Somewhat lower efficiency due to higher interaction rate. Eff~90%
- Electrons: Slower turn-on curve, efficiency reduced from bremsstrahlung. Eff~90%.

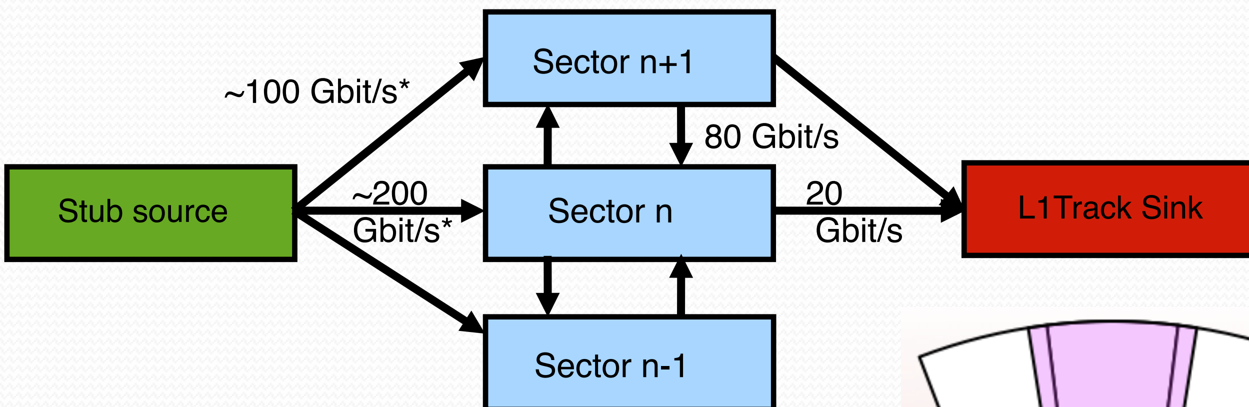
Similar performance is expected in other approaches

Tracklets in Hardware

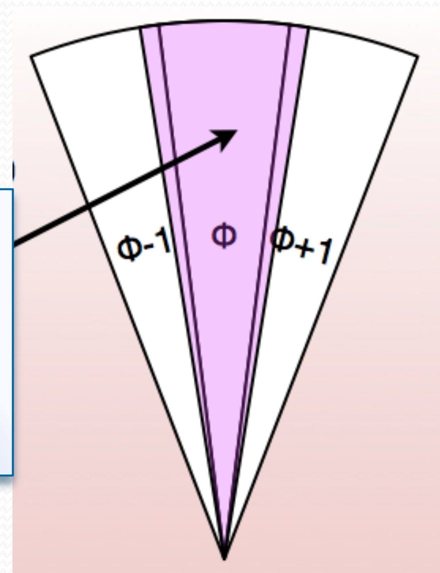
Demonstration in hardware is needed to show that the approach can work within latency budget

Xilinx Virtex-7 based board CTP7 is being used for demonstration

Work on firmware implementation ongoing



One sector processor covers the entire eta range and is 1/28 wide in phi



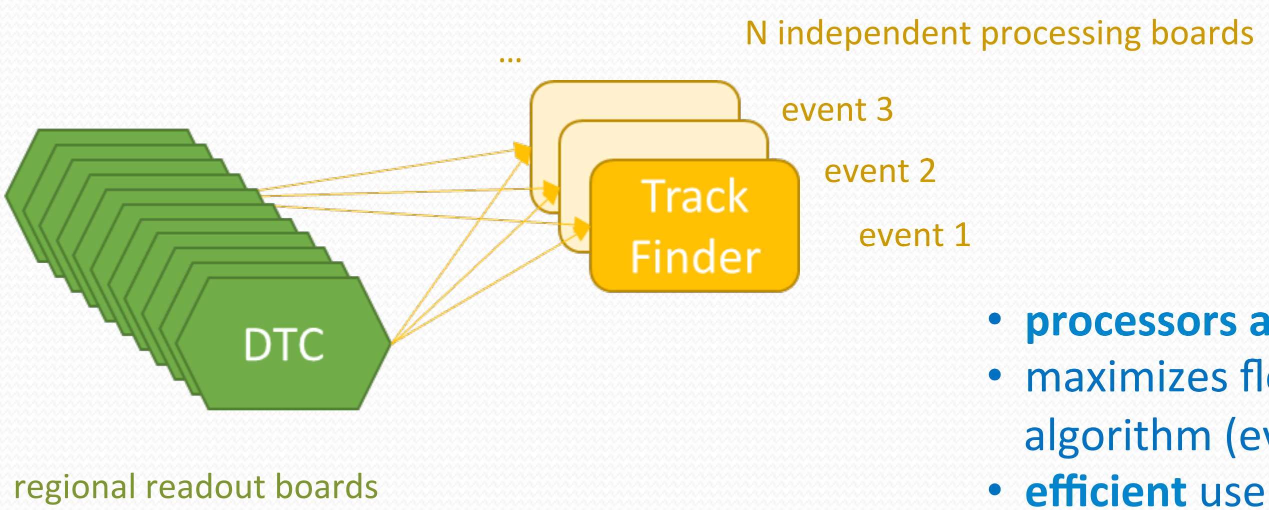
uTCA CTP7 board for demonstrator

Fully Time Multiplexed Based Approach

FM-TMT

Time multiplexed architecture

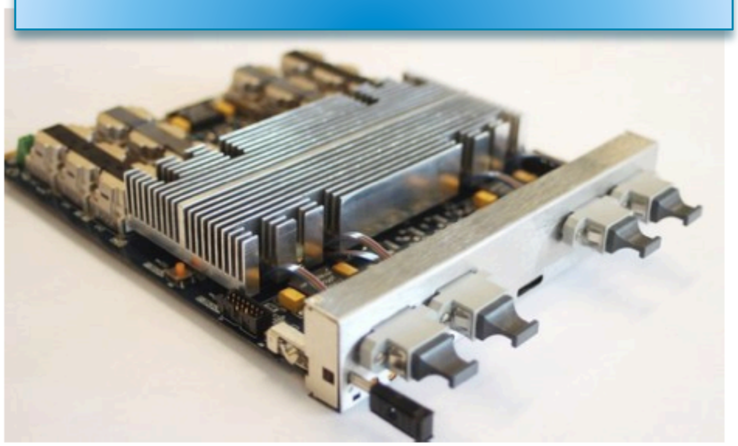
- HLT-like architecture – event data flows to a single processing node
- now implemented in CMS Level 1 Calorimeter Trigger
- allows for a simple, scalable slice demonstration system



- **processors are independent in time**
- maximizes flexibility to make changes to algorithm (even during operation!)
- **efficient** use of FPGA resources
- minimizes hardware regions
- *regional data sharing avoided*

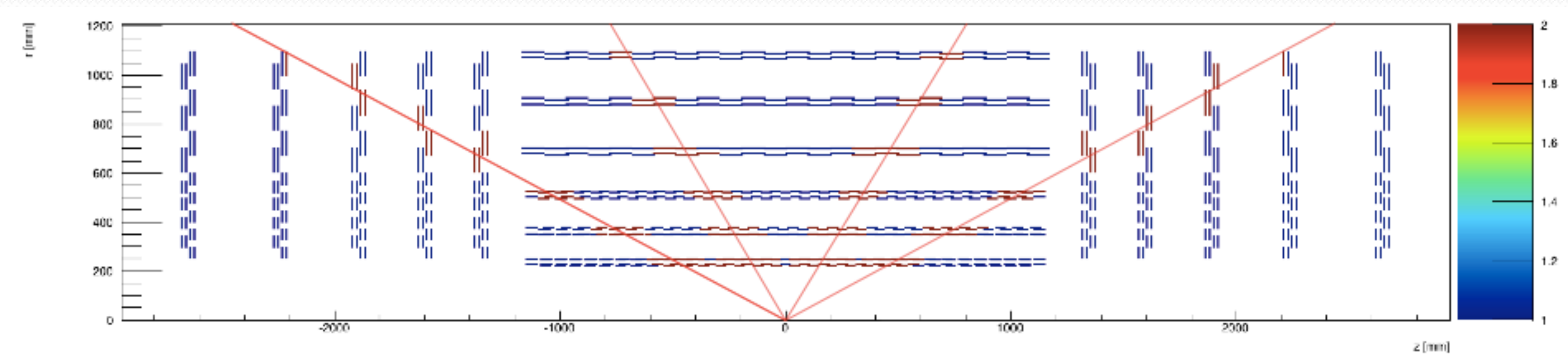
FM-TMT

uTCA MP7 board for demonstrator



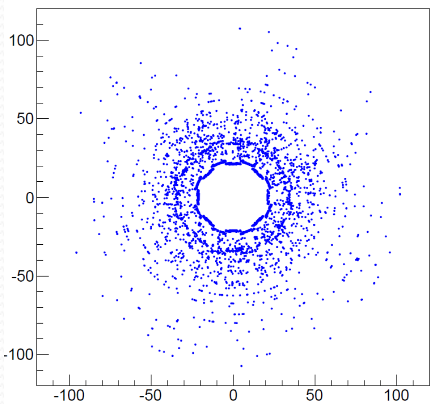
- μTCA card built for CMS upgrade L1 calorimeter trigger
- Contains a Virtex-7 XC7VX690T
- 72 input/ 72 output optical links that operate up to 12.5 Gbps
- Total bandwidth > 0.9 Tbps

- maximum number of links into the L1 Track Finder (72) imposes limit on DTCs connected
- need to divide tracker into at least five regions, e.g. in η (Δη ~ 1.0)
- flexibility to choose 24-36x time multiplexing

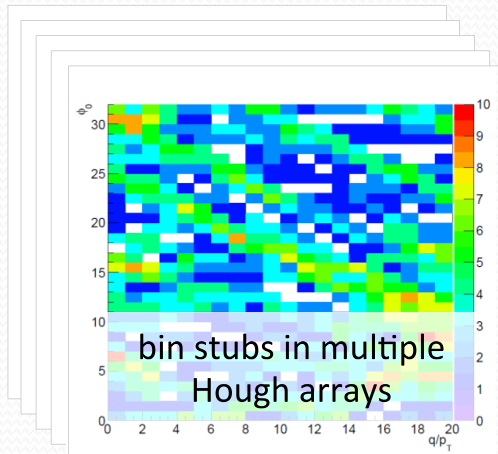


FM-TMT

two step track finding approach based on coarse **2D Hough Transforms**



apply Hough Transform in 2D (e.g. r,ϕ)

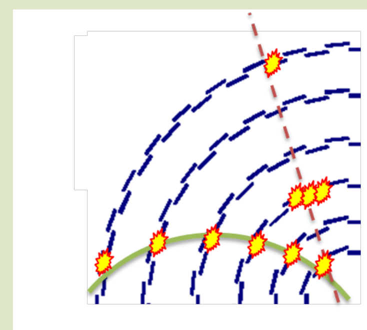


- orders stubs into valid track candidates
- binning of stubs according to projections

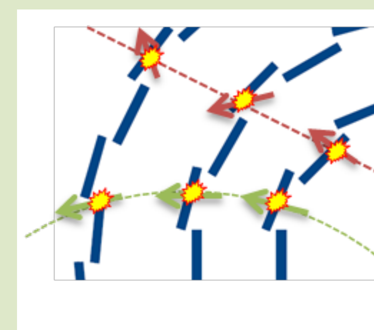
~20x20 typical array size required

36 ϕ segments, each an independent HT

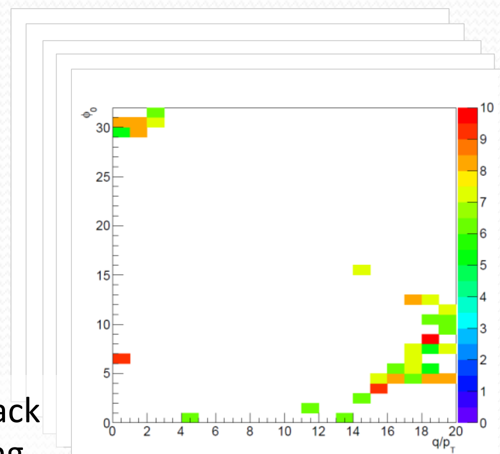
apply track criteria to accept

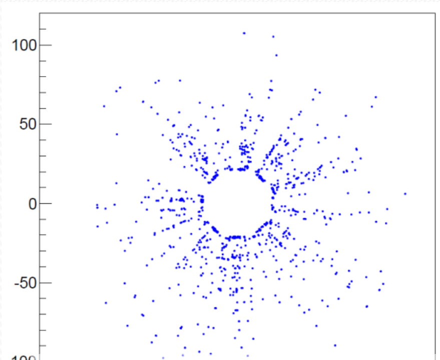


bins with more than 5 stubs at unique radii



bins with stubs that have compatible local bend

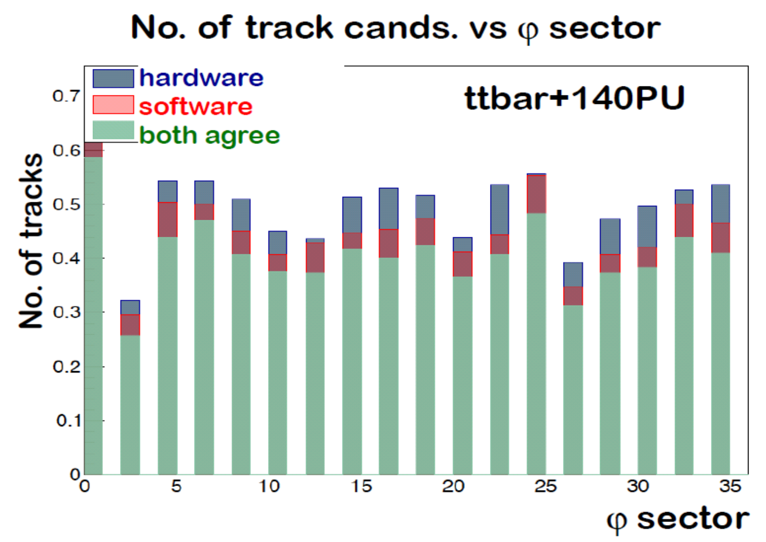


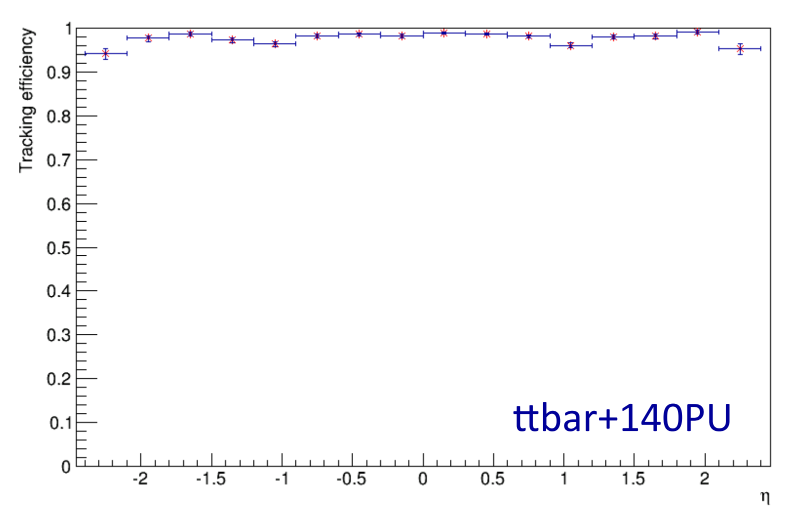


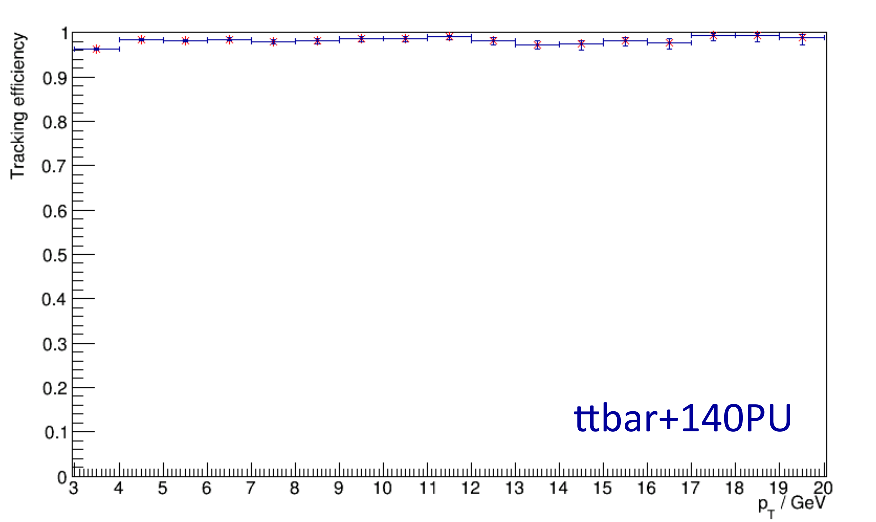
stubs from selected bins form track candidates for further processing

FM-TMT

- injecting stubs from "ttbar+140PU" into hardware & comparing kinematic distributions of tracks found with those predicted by software
- fairly good agreement so far with remaining discrepancies to be debugged
- simulated performance indicates high efficiency for track finding above 3 GeV/c



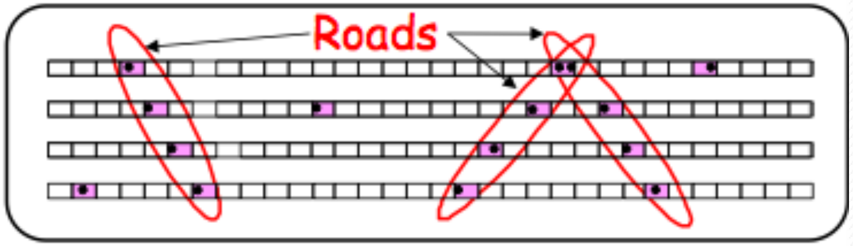


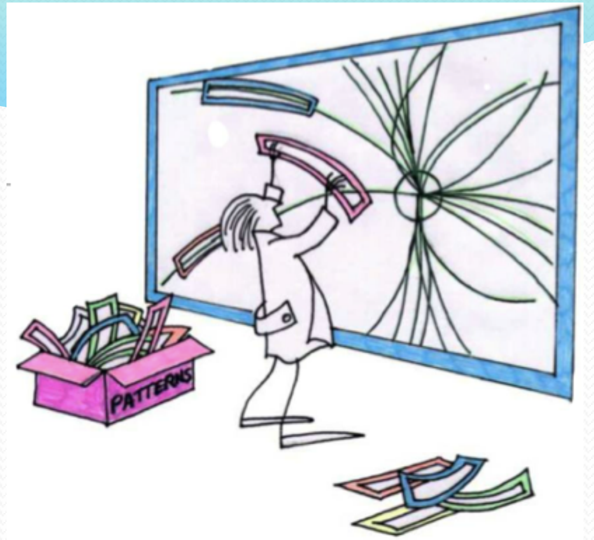


AM+FPGA Based Approach

Associative Memory

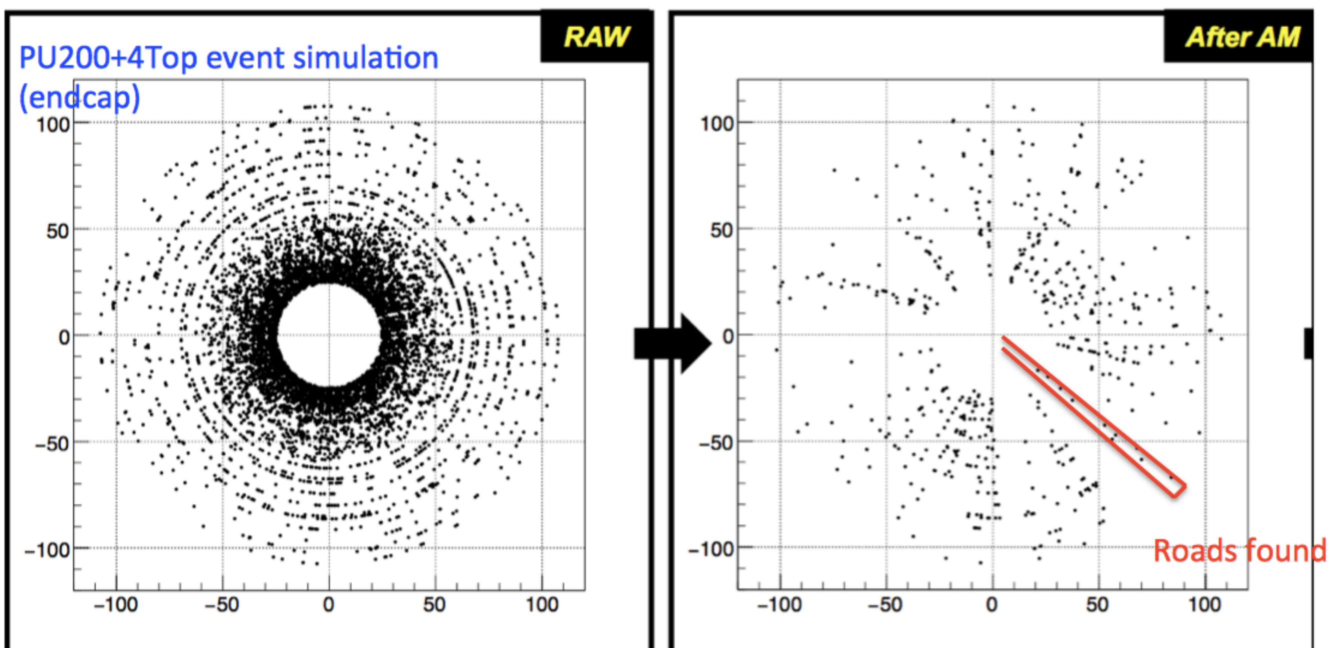
Pattern **R**ecognition **A**ssociative **M**emory = content addressable memory (CAM) cells + majority logic (ML)





Massive parallel processing to tackle the intrinsically complex combinatorics

- Avoid the typical power law dependence of execution time on occupancy
- Solving the pattern recognition in times roughly proportional to the number of hits

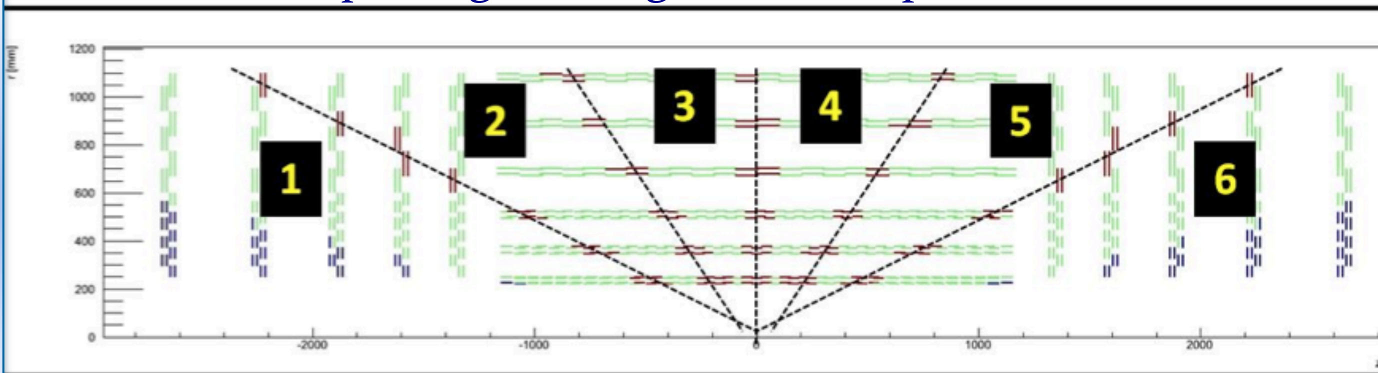


CMS L1 track trigger applications require high pattern density and high operational frequency while managing power needs

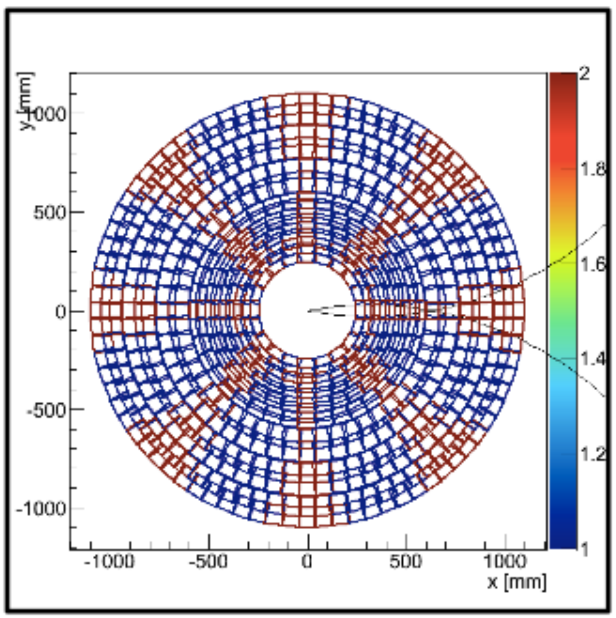
Sectors and processors

Regional multiplexing => divide the detector into trigger towers
Time multiplexing => assign different processors for events

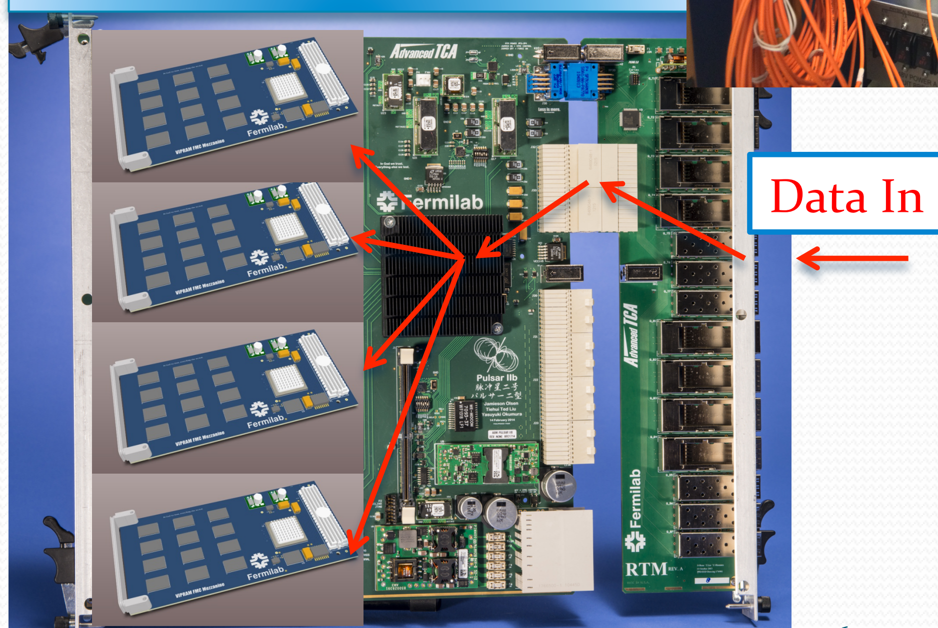
6 regions in r-z



8 regions in r-phi



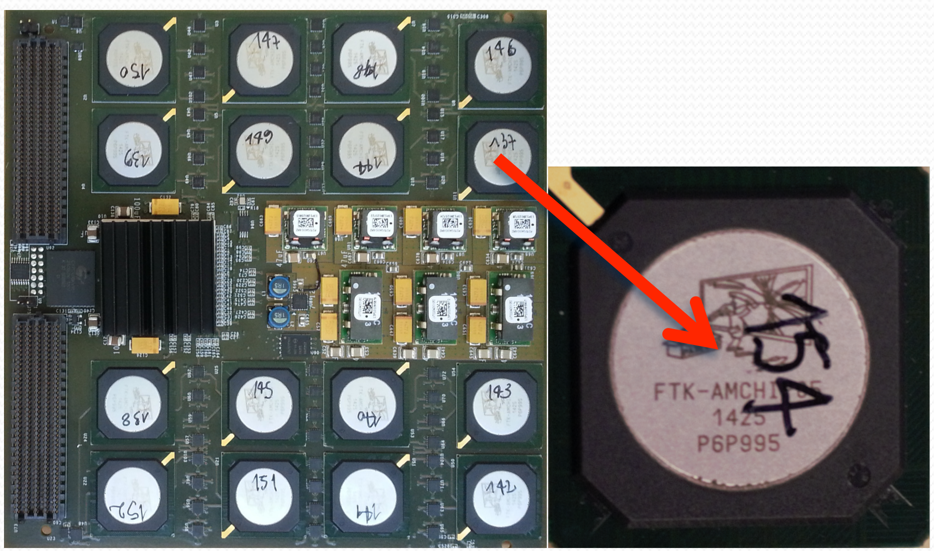
ATCA Pulsar-2b board for demo



Tale of two mezzanines

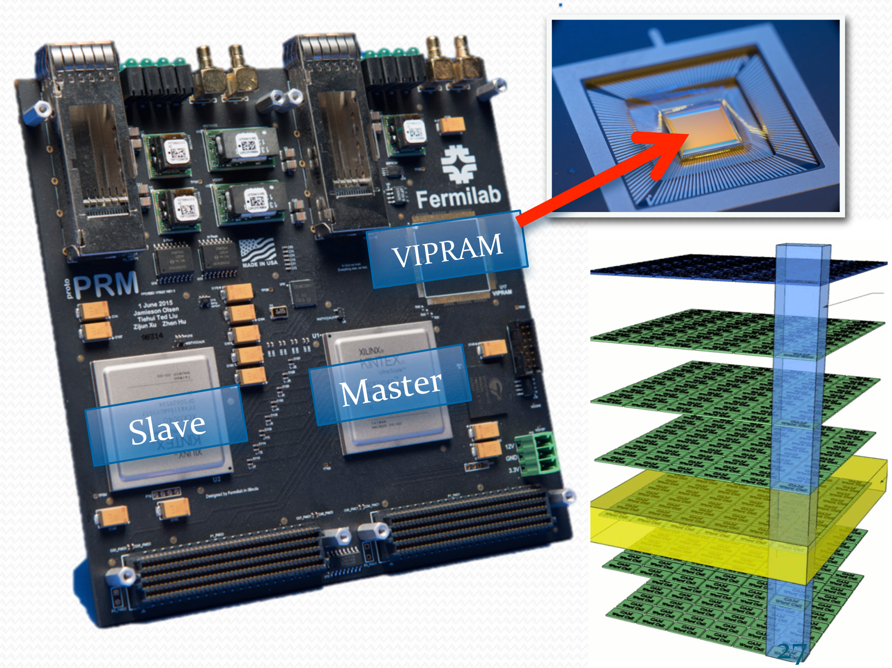
Kintex-7 FPGA + AMchip05/06

- Designed based on ATLAS FTK chip
  - High pattern density (AM05/6, 2k/128k)
  - AM05 version in hand and working
- *Goal: to prove that the 2M patterns can be implemented with today's technology*



UltraScale FPGA + VIPRAM

- Designed for L1 applications
  - Low latency
  - *Low pattern density (4-16k)*
- UltraScale FPGAs, *more capability*
- *Goal: to optimize for latency and performance, develop the spec for the final chip*

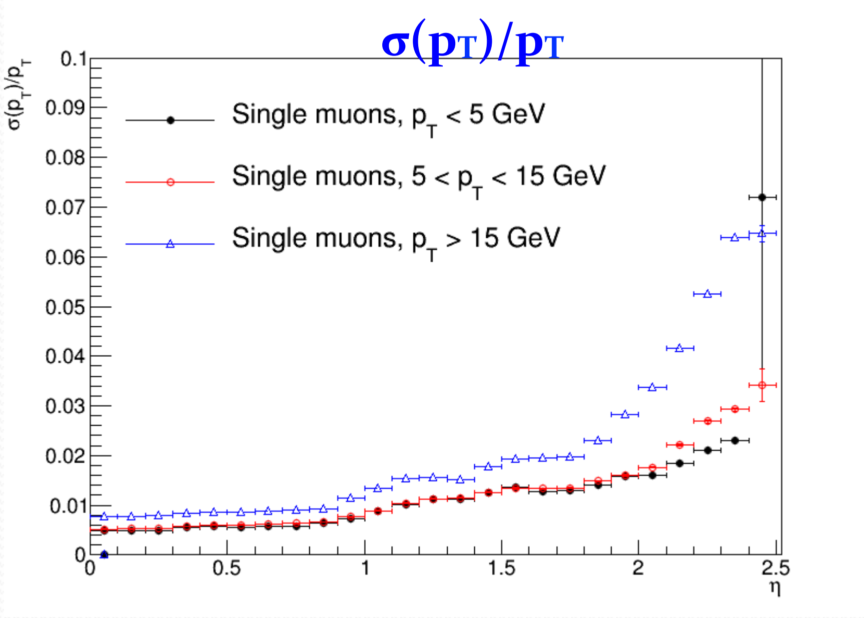


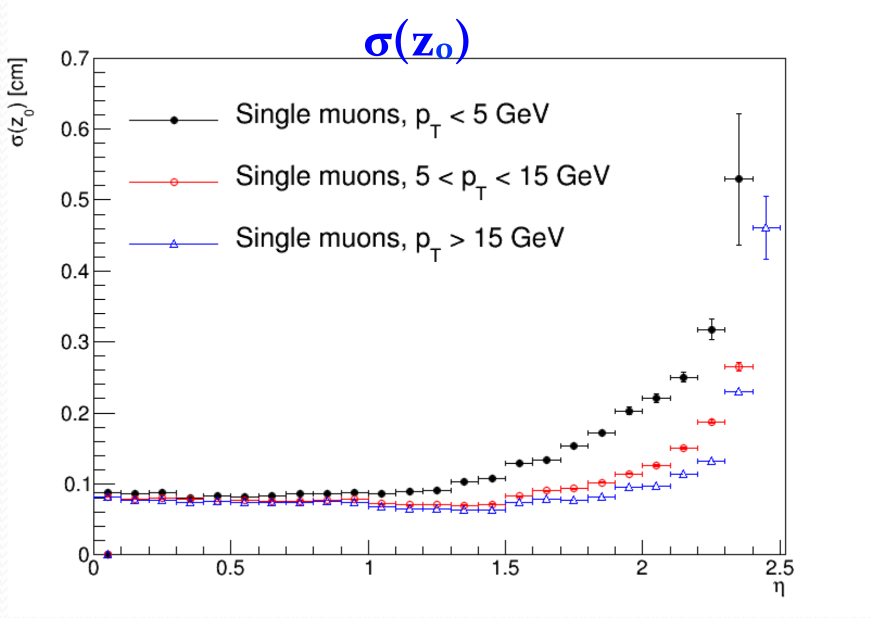
Linearized track fitting

Given a set of stubs estimate:
- compatibility with a track: χ^2/ndof
- track parameters: charge/p_T, ϕ_0, z_0, cot(θ) and d_0

Method: Linearized Track Fit $\phi_0 = \sum_i A_i \Delta\phi_i + \bar{\phi}_0$ where $\Delta\phi_i = \phi_i - \bar{\phi}_i$

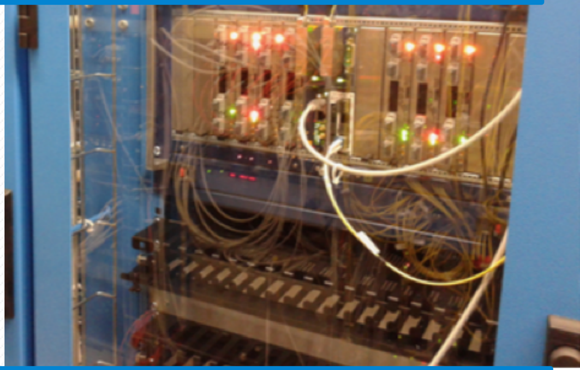
New Idea: To minimize number of constants transform the tracker into a smooth cylinder (only 20k constants for the entire tracker)



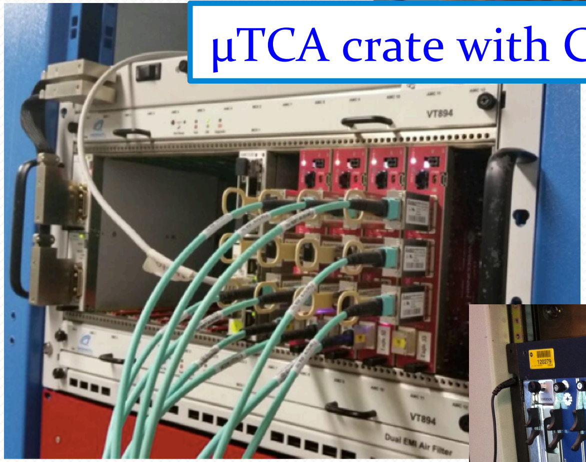


Gearing up for demonstration

- Need to demonstrate feasibility to finalize design of the tracker
- At least one approach has to be proven to work
- Equation with many variables:
  - Latency
  - Efficiency & Fake Rate
  - Anticipated size and cost of the system
  - Robustness (against material, alignment, beam shifts, etc)`
- Target – end of this year



μTCA crate with MP7 (TMT)



μTCA crate with CTP7 (Tracklet)

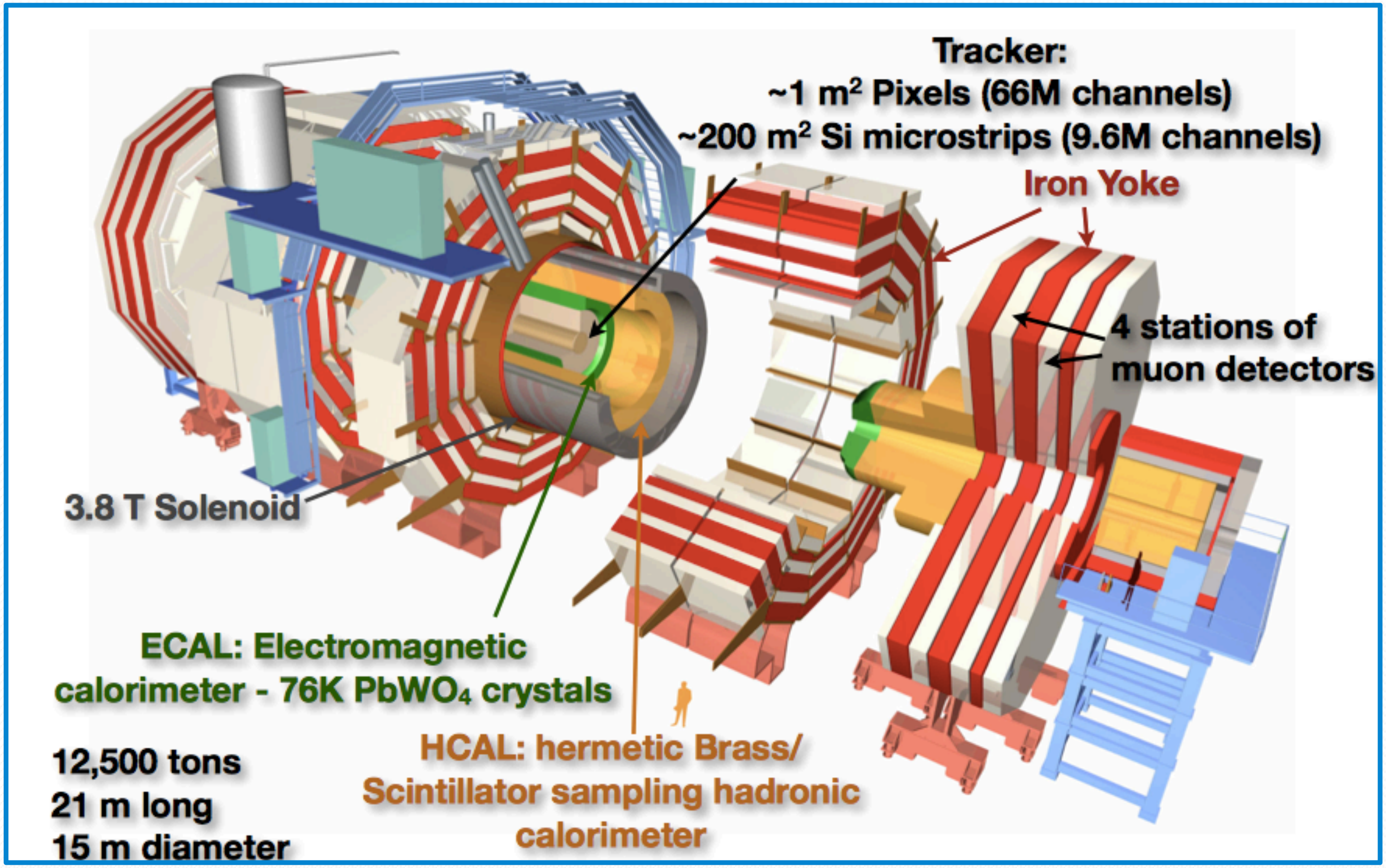
ATCA crate with Pulsar-2b (AM+FPGA)

Conclusions

- Having L1 track trigger is crucial for success of CMS physics goals in HL-LHC
- Highly challenging as track triggering at this scale and speed has never been implemented before
- Aggressive R&D efforts to address the challenge -> both FPGA-only and AM+FPGA approaches
- Plan to demonstrate by the end of 2016 (with Tracker Technical Design Report planned in 2017)

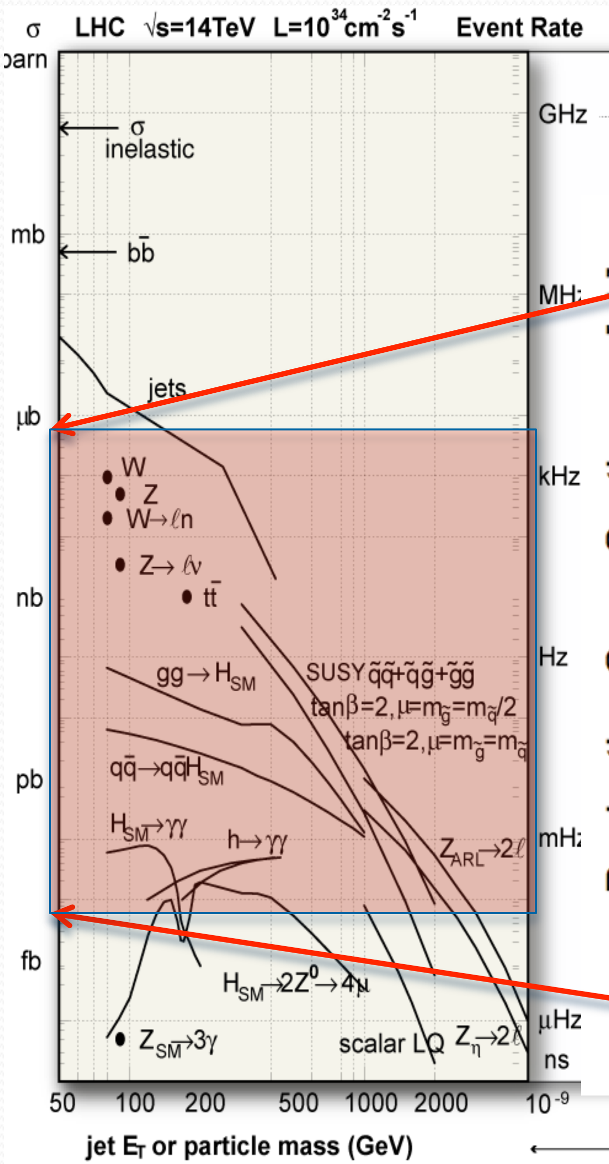
Backup

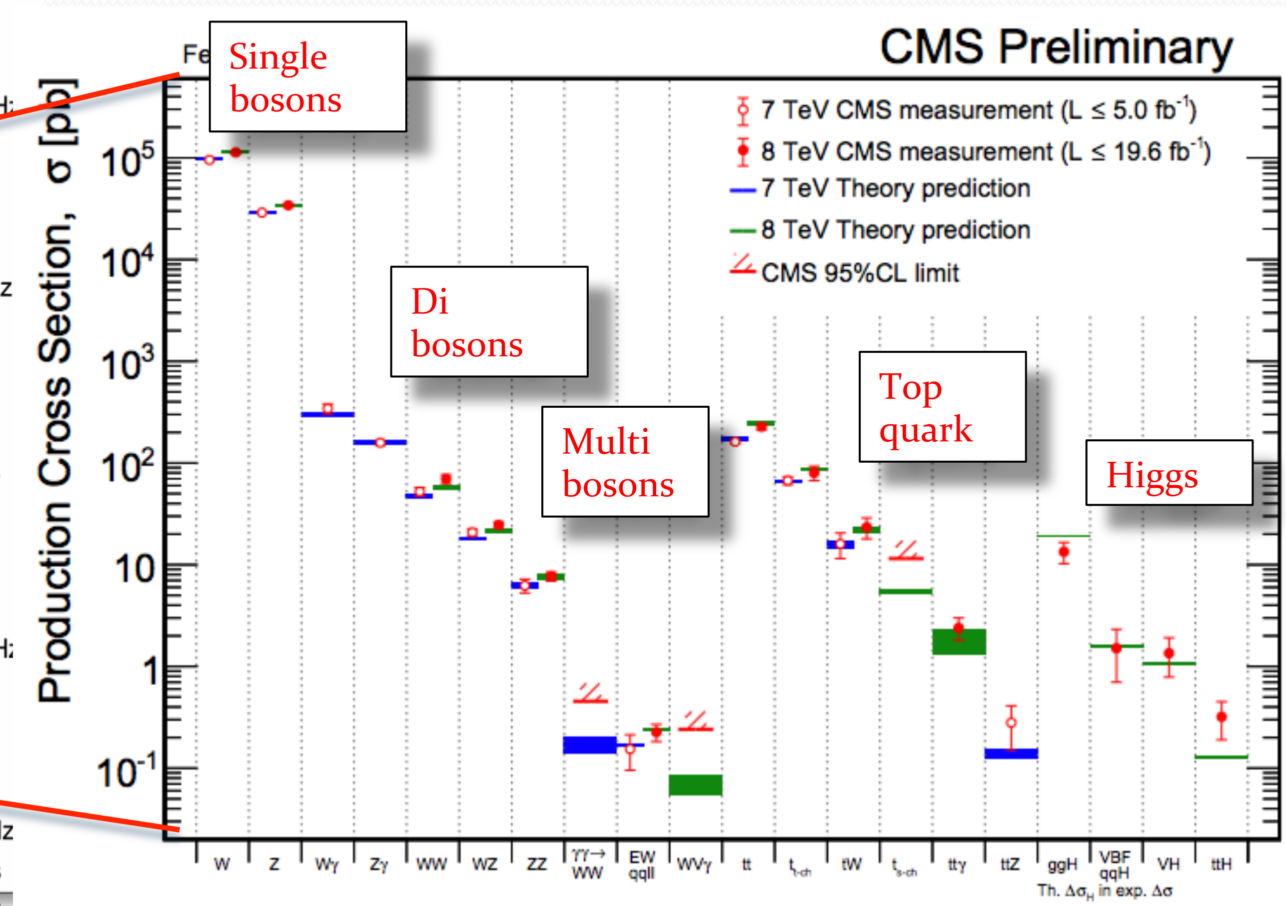
CMS Detector



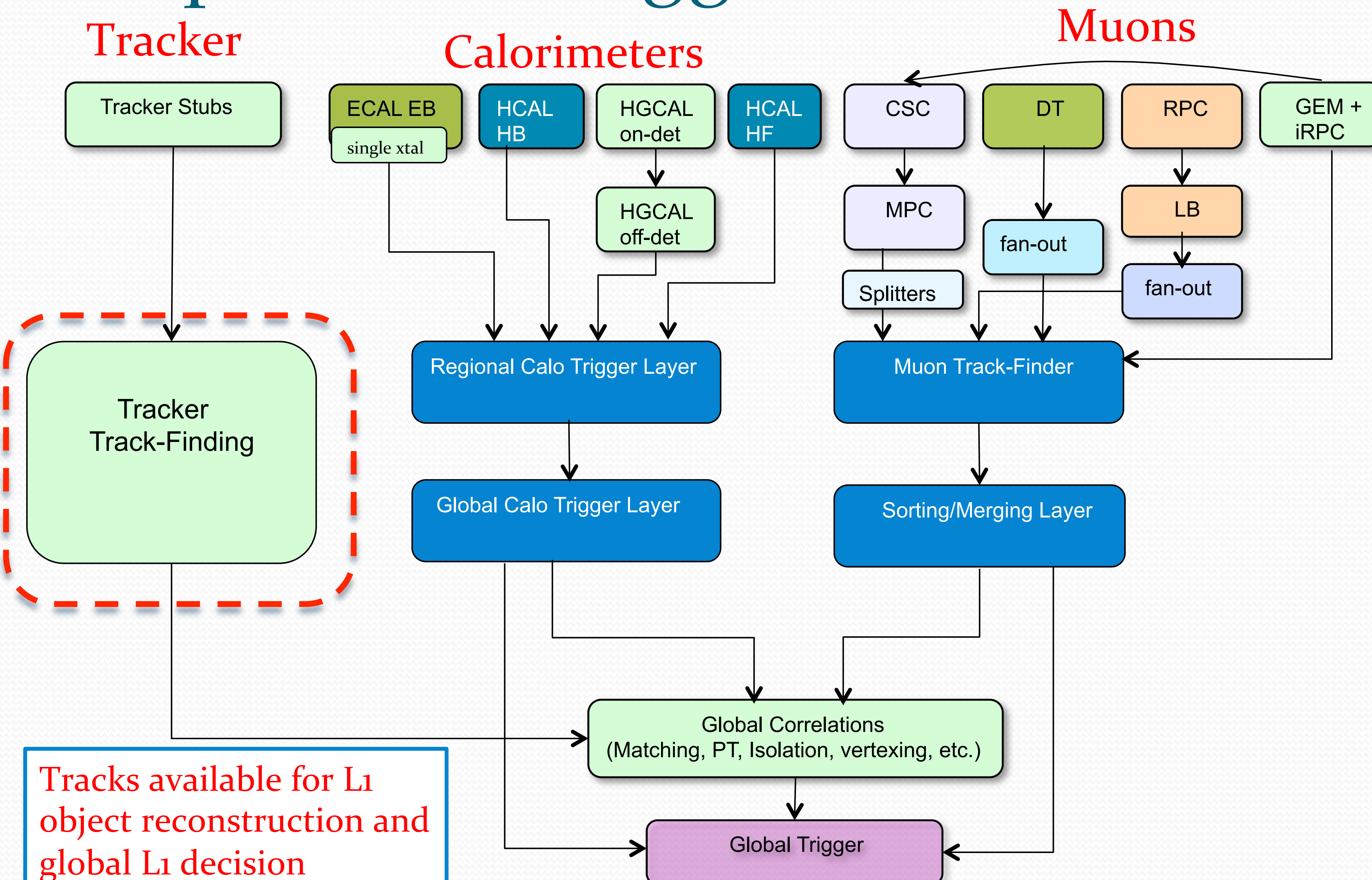
More data

Need a lot of data to probe rare processes!



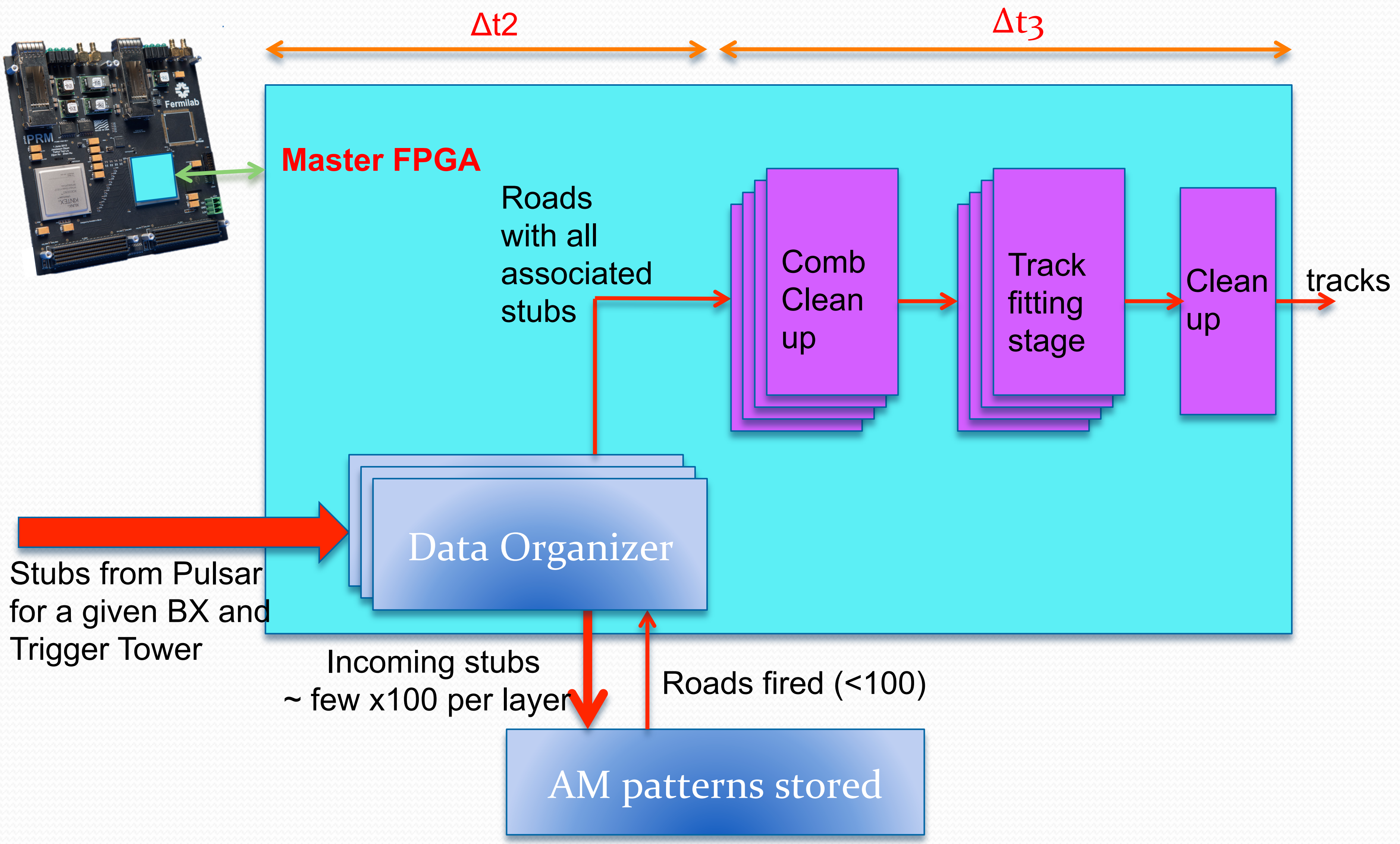


Proposed L1 Trigger Architecture

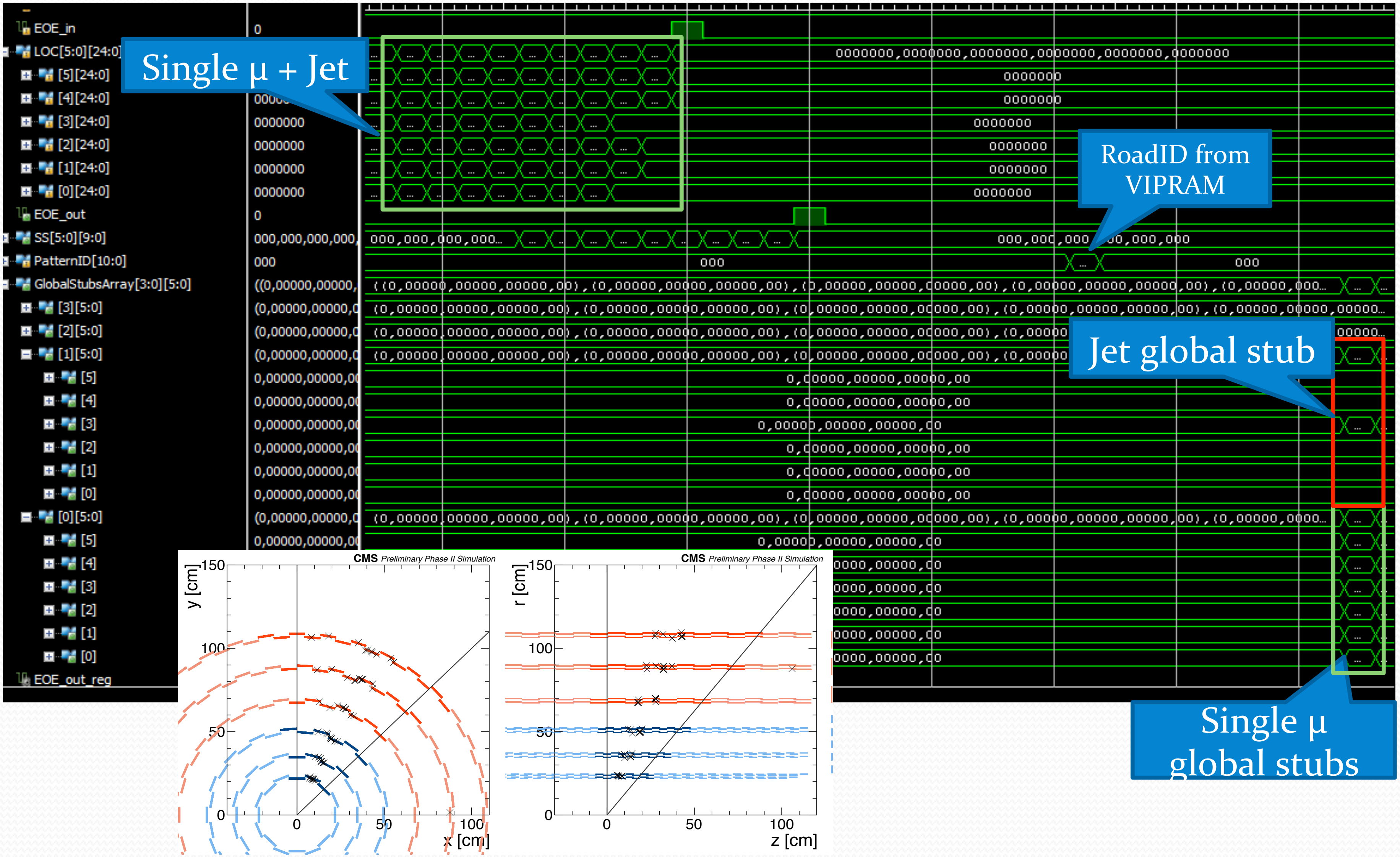


Tracks available for L1 object reconstruction and global L1 decision

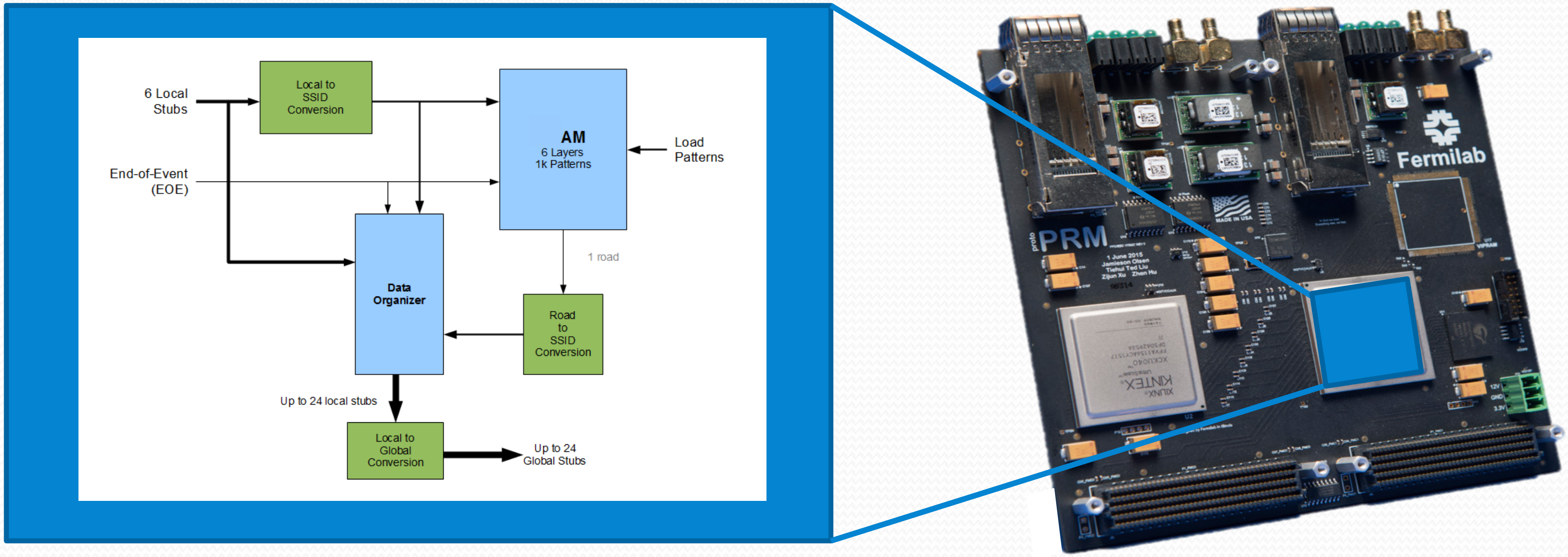
Pattern Recognition Engine Flow

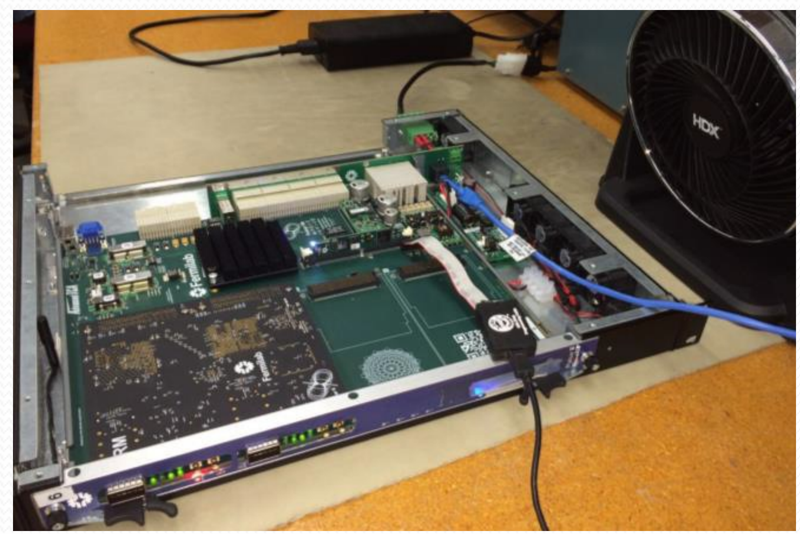


Single Muon + Jet



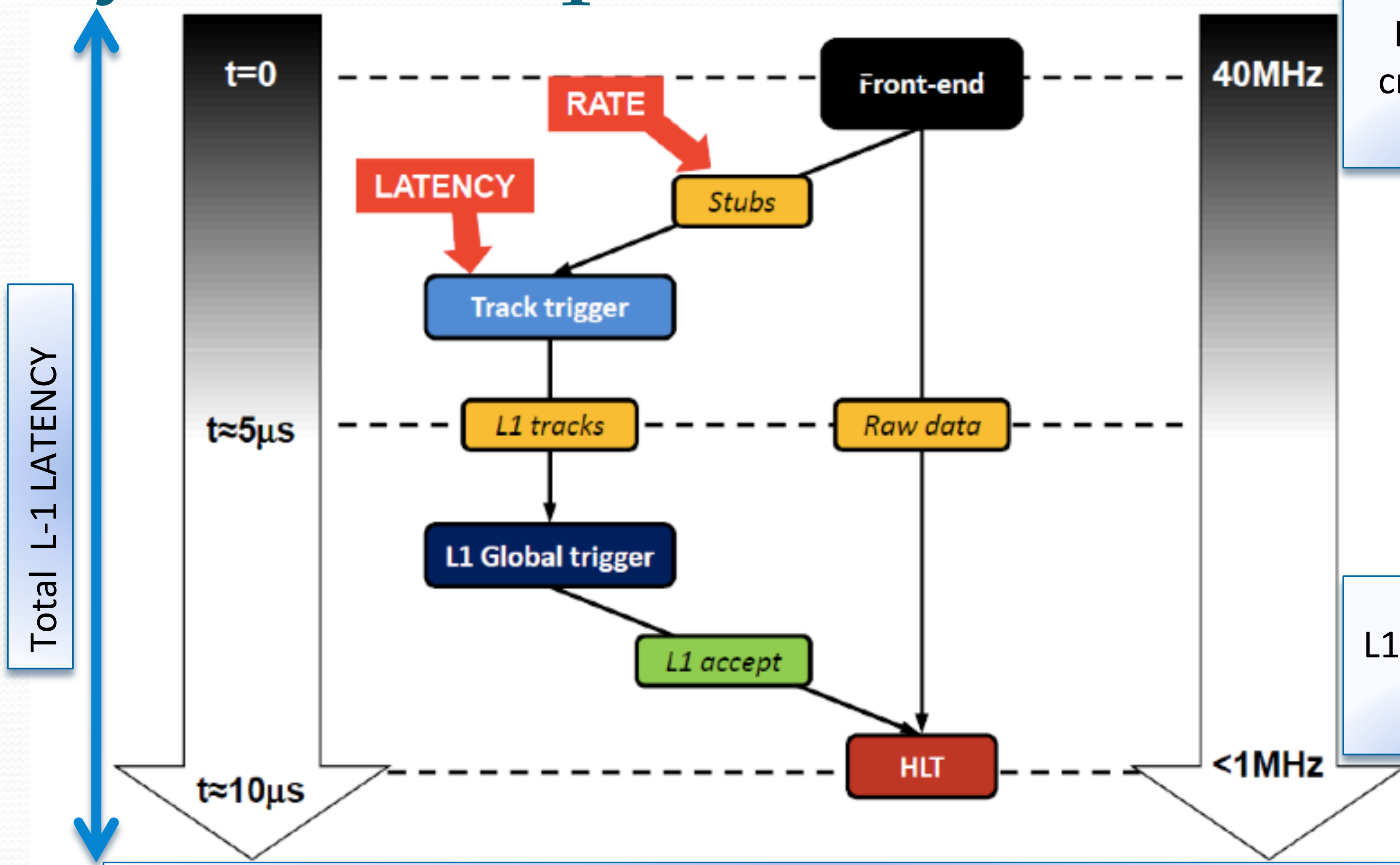
Running Firmware in PRM Board





- First time running everything in PRM board
  - ✓ All the function blocks are implemented in the Master FPGA of proPRM for simplification
  - ✓ Event MEM and Init MEM are BlockRAM with Initial Values (ROM)

System Requirements



Bunch crossing rate

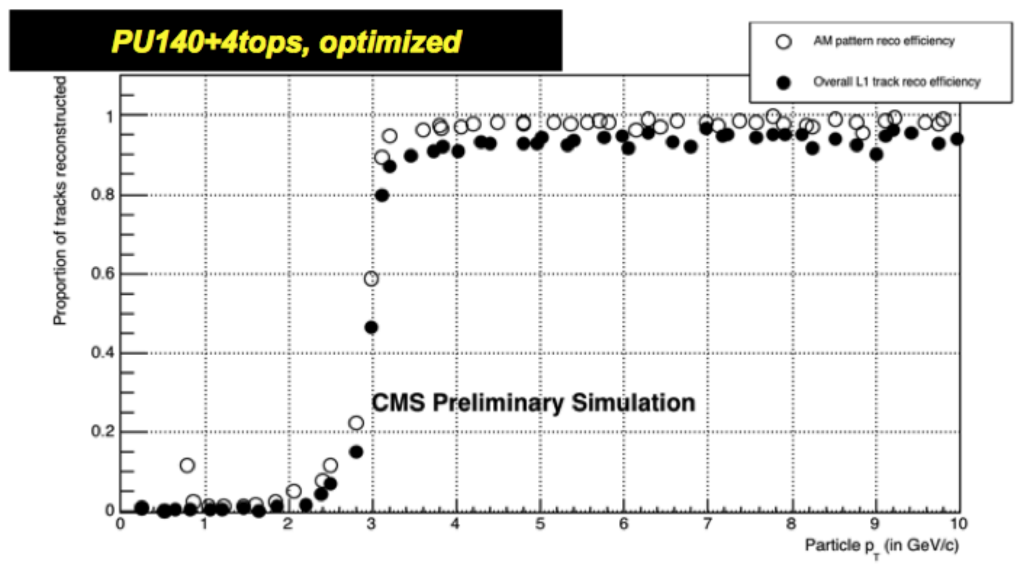
L1 Output Rate

- ~ 500 Tb/s bandwidth needed(50-100 Tbs after soft track suppression)
- ~5 us to reconstruct tracks (~12 us total L1 latency)

AM Simulation

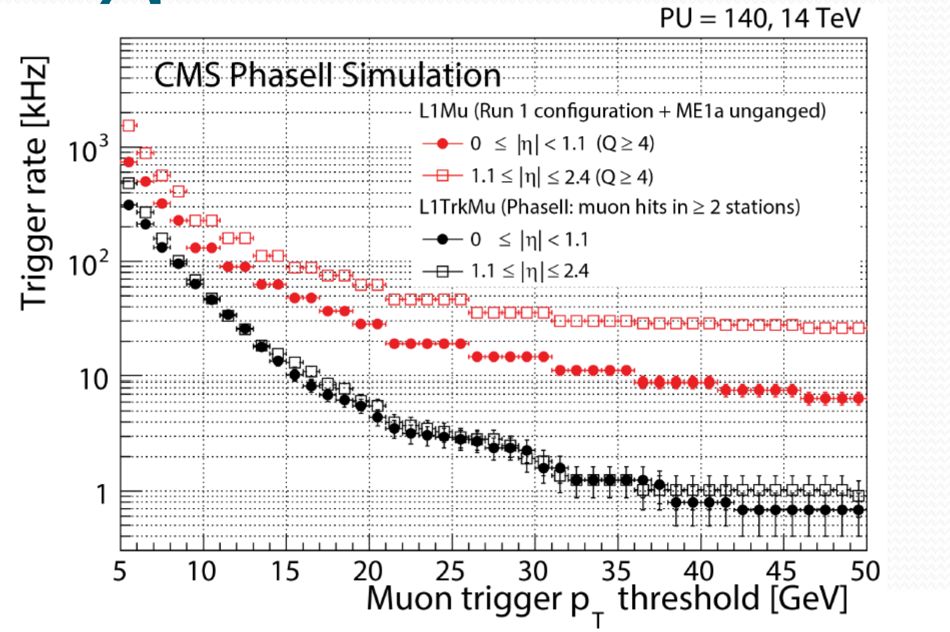
Fountain-like Sstrips, w/o z-segmentation, seem to achieve smaller pattern bank sizes with less fit combinations

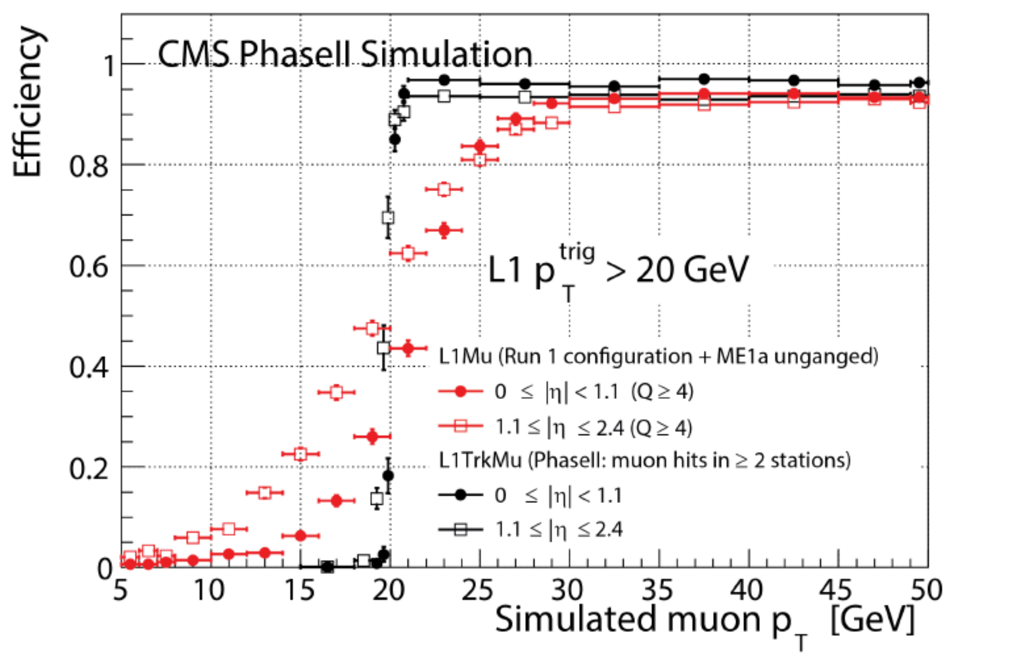
- Stubs input per trigger tower: ~ few x 100
- With patterns per trigger tower: ~ 4 M
- Roads fired per trigger tower: <50 *unique* patterns fired
- Stubs left for track fitting af AM stage filtering: ~ 20% (th is a set of "stubs of interests"



Impact of tracking at L1:

- Immense trigger challenge facing CMS
- EXAMPLE: At upgraded luminosity trigger curve flattens out for L1 muons
  - Most important handle (pt) no longer works with just the information from the muon system
- Need additional information from the tracker to control trigger rates





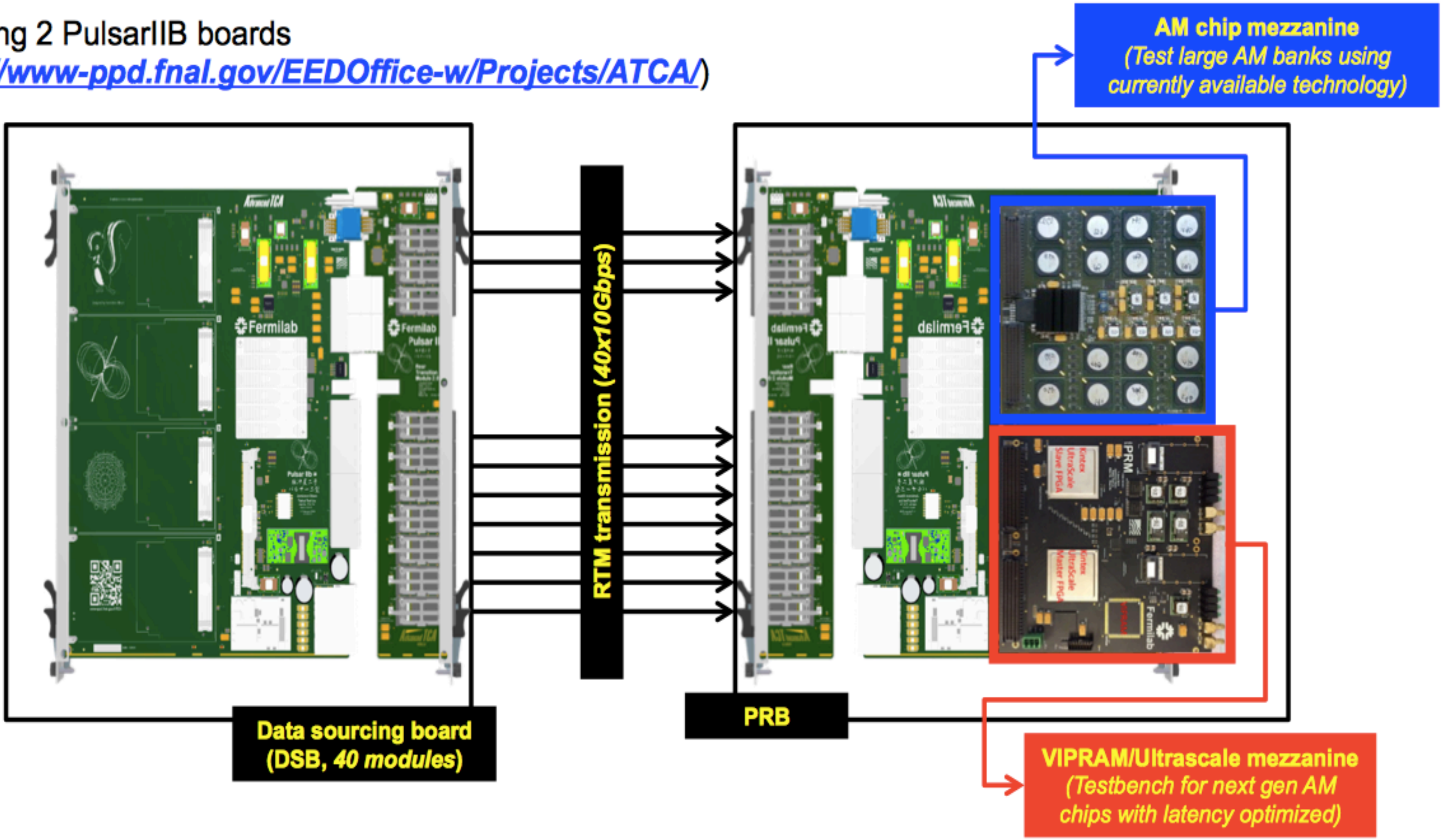
Impact of tracking at L1:

- Current Level-1 Trigger
  - No central tracking information
  - Electrons/Gammas (EG), Taus, Jets based solely on calorimeter deposits.
  - Muons reconstructed from tracks in muon chambers.
  - **Maximum Bandwidth: 100 kHz**
- HL-LHC:
  - Current Trigger System:
    - EG rate @25 GeV > 100 kHz
    - Muon rate plateaus
    - Overall Trigger Rate > 1000 kHz (***unsustainable***) to reach physics goals
  - Upgraded System
    - Must increase total bandwidth
    - Must increase trigger capabilities
    - **Level-1 Tracking is a completely NEW handle.**

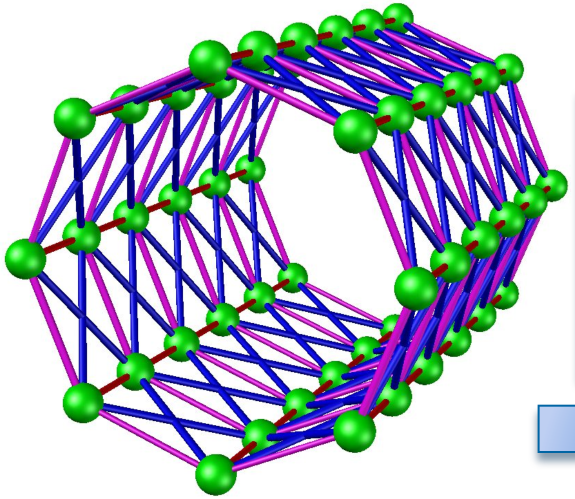
$L = 5.6 \times 10^{34}\ \mathrm{cm}^{-2}\mathrm{s}^{-1}$ $\langle PU \rangle = 140$	Level-1 Trigger with Level-1 Tracks	
Trigger Algorithm	Rate [kHz]	Offline Threshold(s) [GeV]
Single Mu (tk)	14	18
Double Mu (tk)	1.1	14 10
ele (iso tk) + Mu (tk)	0.7	19 10.5
Single Ele (tk)	16	31
Single iso Ele (tk)	13	27
Single γ (tk-iso)	31	31
ele (iso tk) + e/γ	11	22 16
Double γ (tk-iso)	17	22 16
Single Tau (tk)	13	88
Tau (tk) + Tau	32	56 56
ele (iso tk) + Tau	7.4	19 50
Tau (tk) + Mu (tk)	5.4	45 14
Single Jet	42	173
Double Jet (tk)	26	2@136
Quad Jet (tk)	12	4@72
Single ele (tk) + Jet	15	23 66
Single Mu (tk) + Jet	8.8	16 66
Single ele (tk) + H_T^{miss} (tk)	10	23 95
Single Mu (tk) + H_T^{miss} (tk)	2.7	16 95
H_T (tk)	13	350
Rate for above Triggers	180	
Est. Total Level-1 Menu Rate	**260**	

Board level development

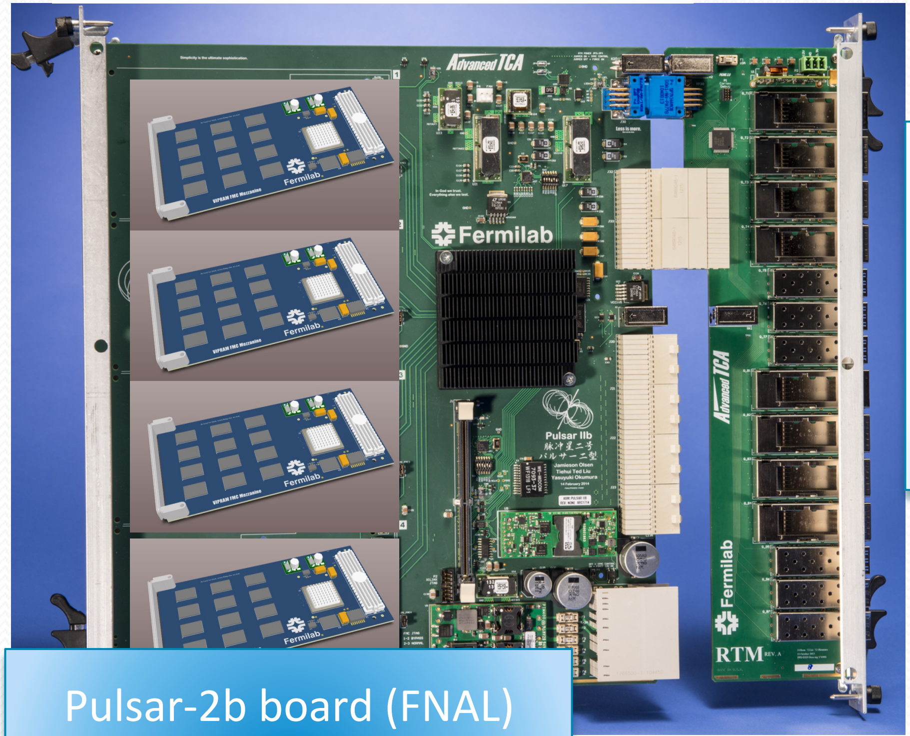
→ Using 2 PulsarIIB boards
(http://www-ppd.fnal.gov/EEDOffice-w/Projects/ATCA/)



AM Architecture



Architecture is flexible and scalable



Pulsar-2b board (FNAL)

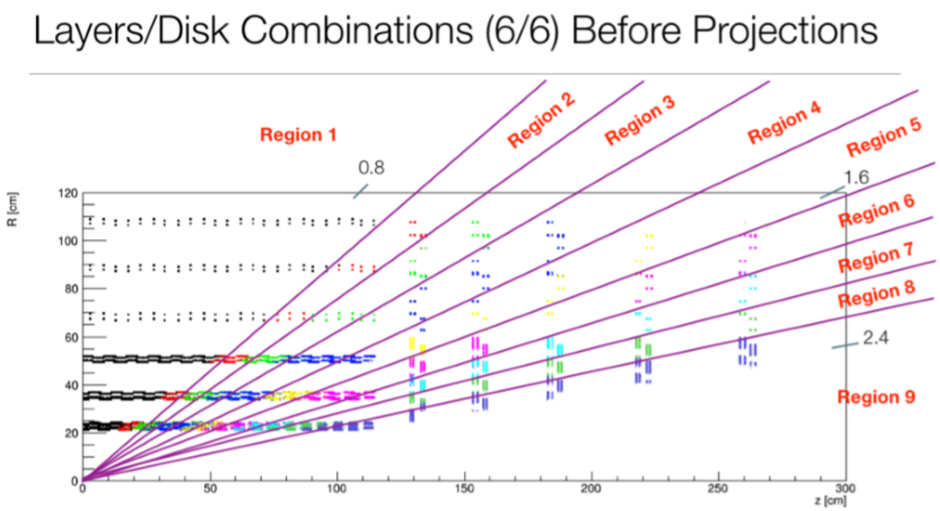
- Ten Processors send target Processor Blade in a round robin scheme.

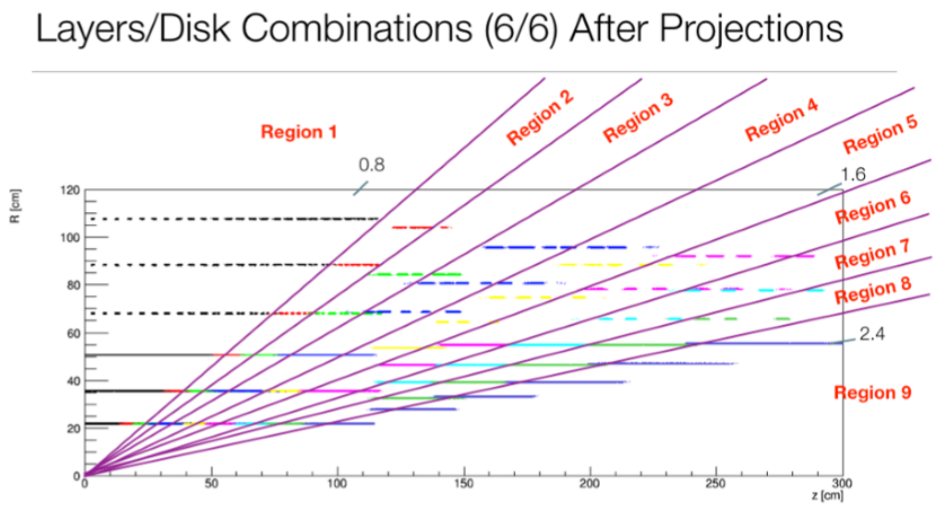
Linearized track fitting

Given a set of stubs estimate:
- compatibility with a track: χ^2/ndof
- track parameters: charge/p_T, ϕ_0, z_0, $\cot(\theta)$ and d_0

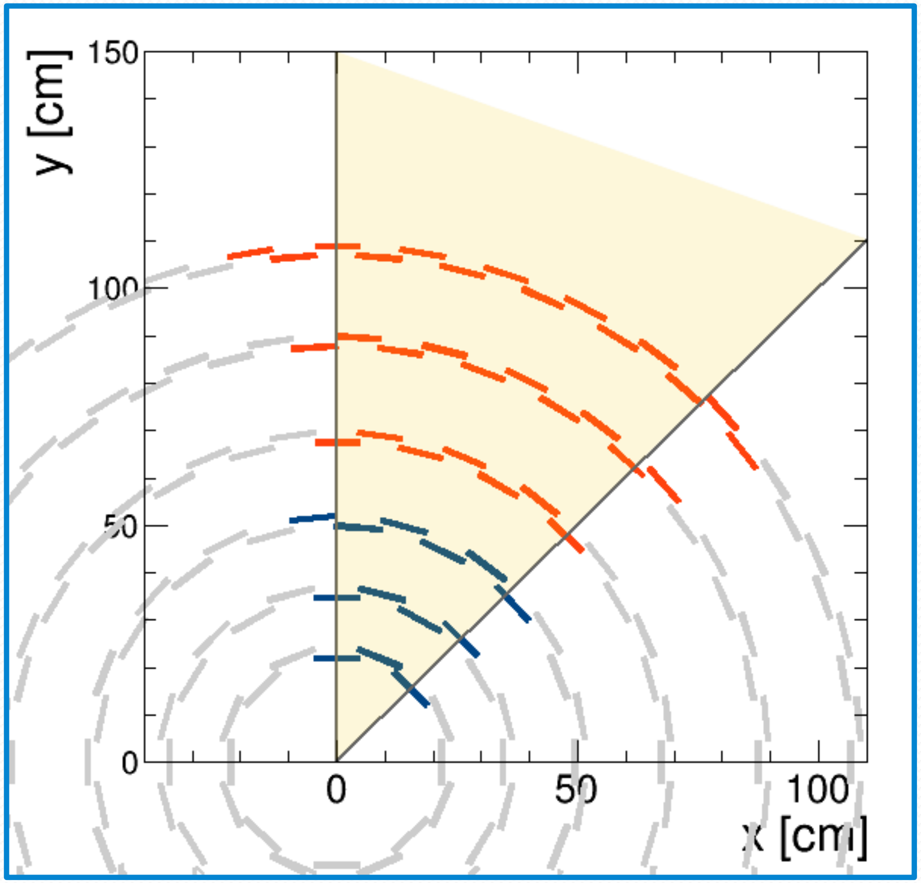
Method: Linearized Track Fit $\phi_0 = \sum_i A_i \Delta\phi_i + \bar{\phi}_0$ where $\Delta\phi_i = \phi_i - \bar{\phi}_i$

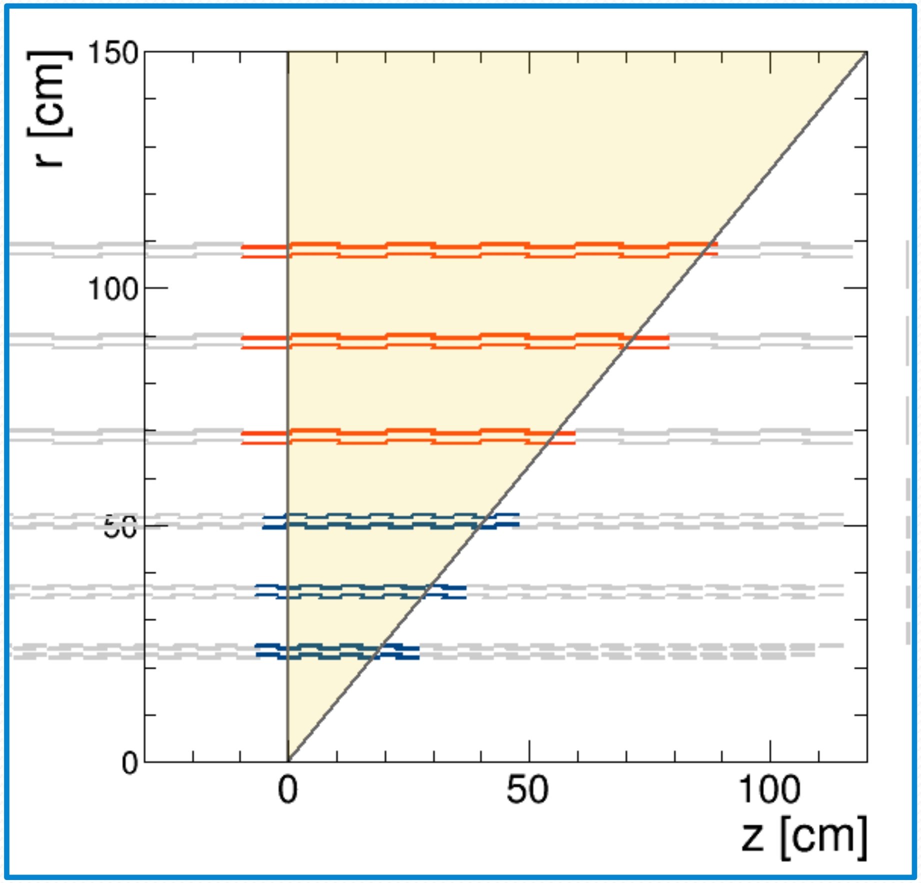
To minimize number of constants transform the tracker into a smooth cylinder





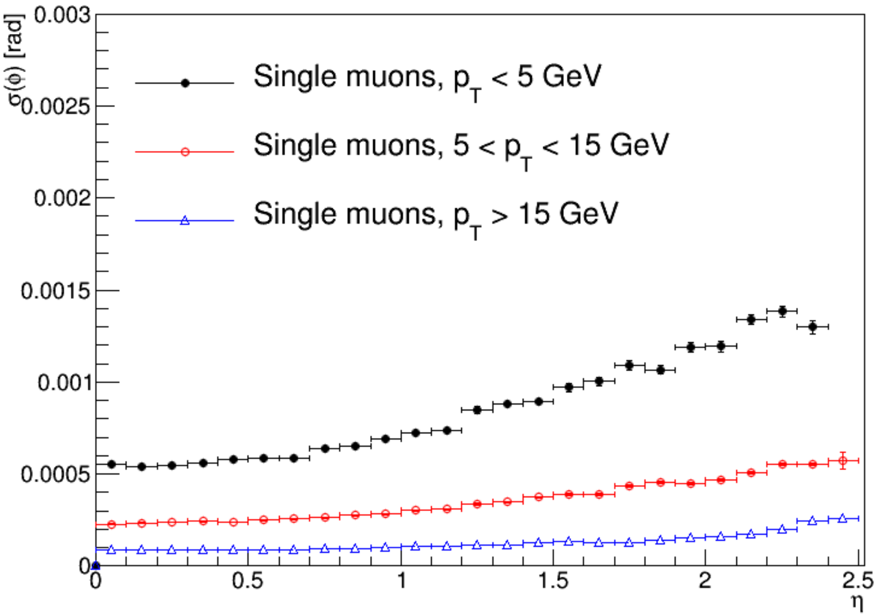
Example: Barrel Trigger Tower



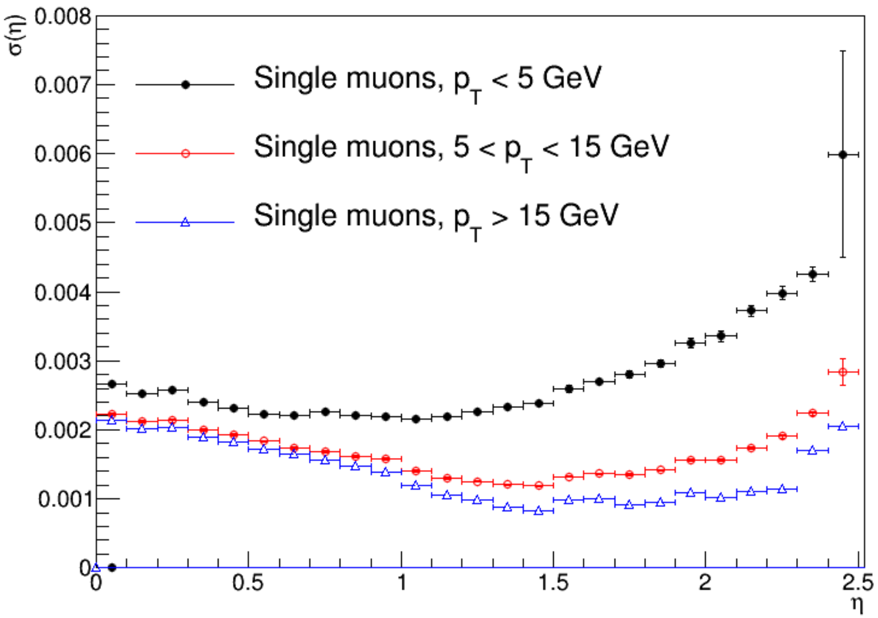


Linearized track fitting

σ(φ₀)



σ(η)

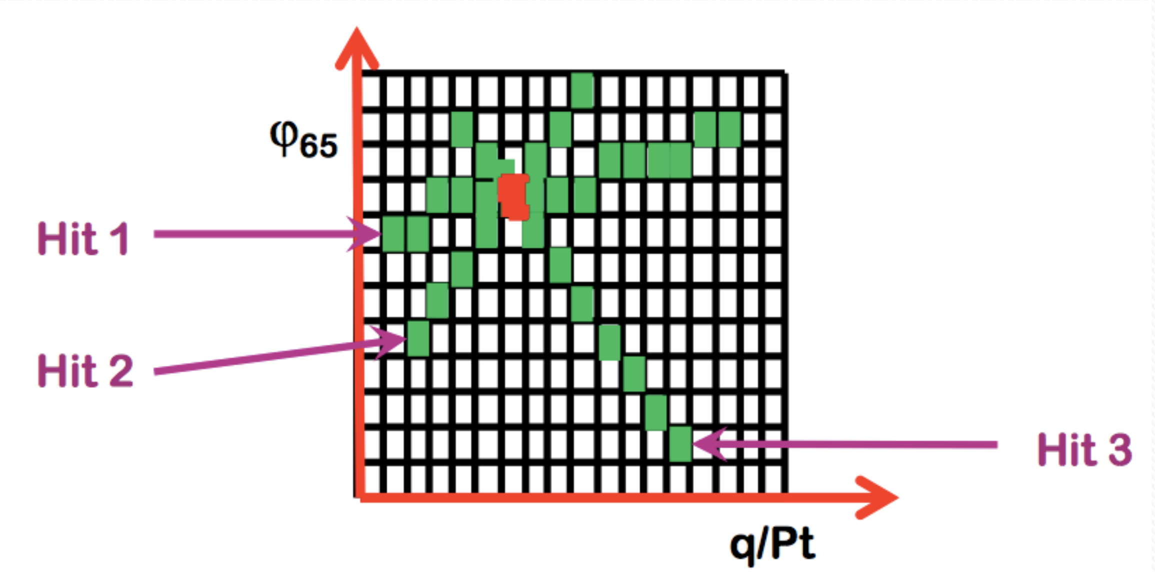


Linearized track fitting

- Including 5/6
- 42 (6x6) unique matrices for 6/6 and 252 (5x5) unique matrices for 5/6
- Total number of constants: 19800

Barrel $0 < \eta < 0.8$	Hybrid $0.8 < \eta < 1.6$	Endcaps $\eta > 1.6$
transverse 2 6x6 12 5x5 R-z 1 6x6 6 5x5	transverse 18 6x6 108 5x5 R-z 9 6x6 54 5x5	transverse 16 6x6 96 5x5 R-z 8 6x6 48 5x5
1100 constants	9900 constants	8800 constants

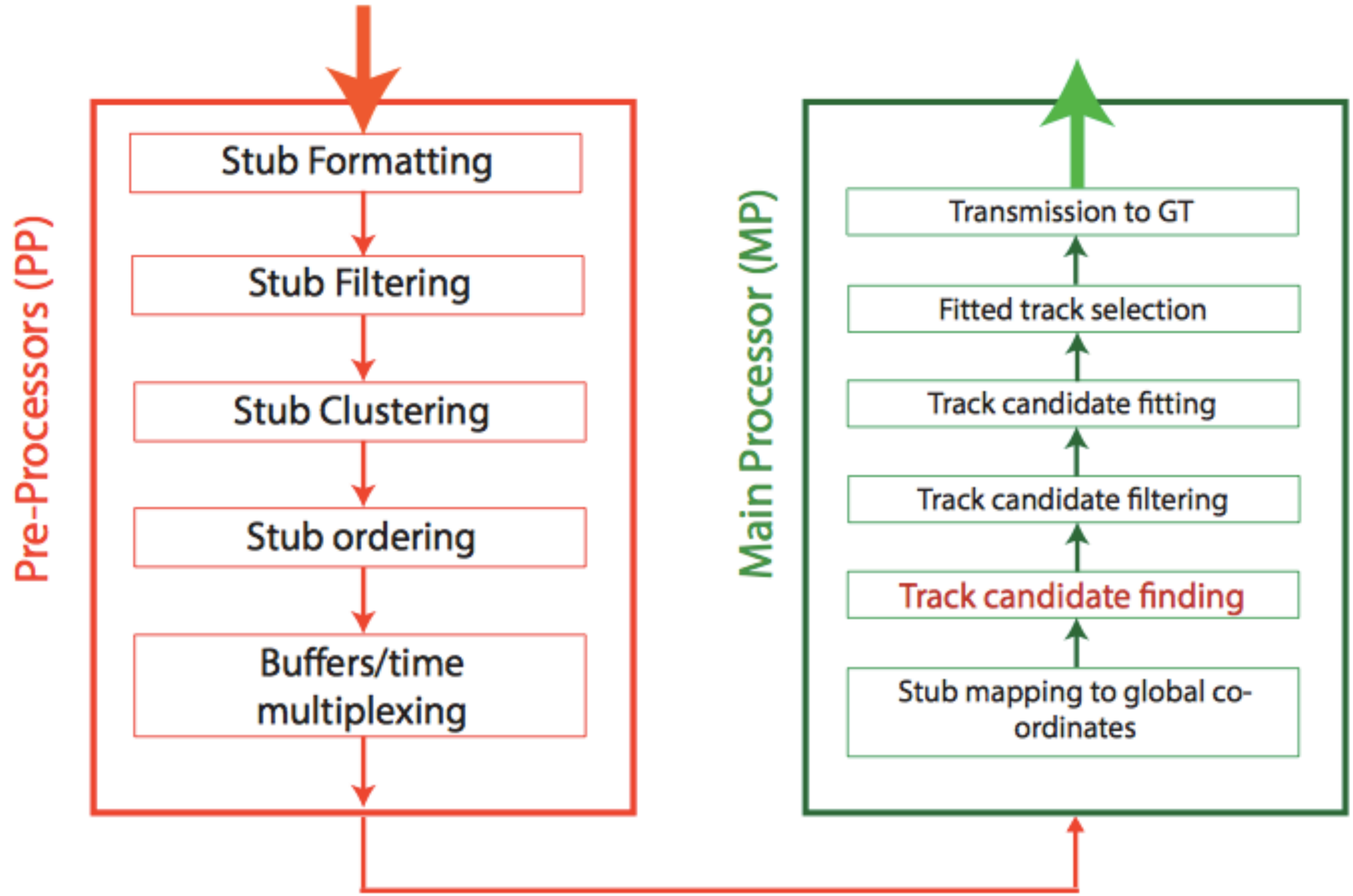
FM-TMT



- Track finding done using Hough Transformation (HT)
- 36 or 64 (2 implementations) φ sectors. Processed processed by independent HT
- Currently, each MP7 processes all (or many) ϕ sectors within a single η sector.
- First tracks showing up in hardware. ~ agree with simulation

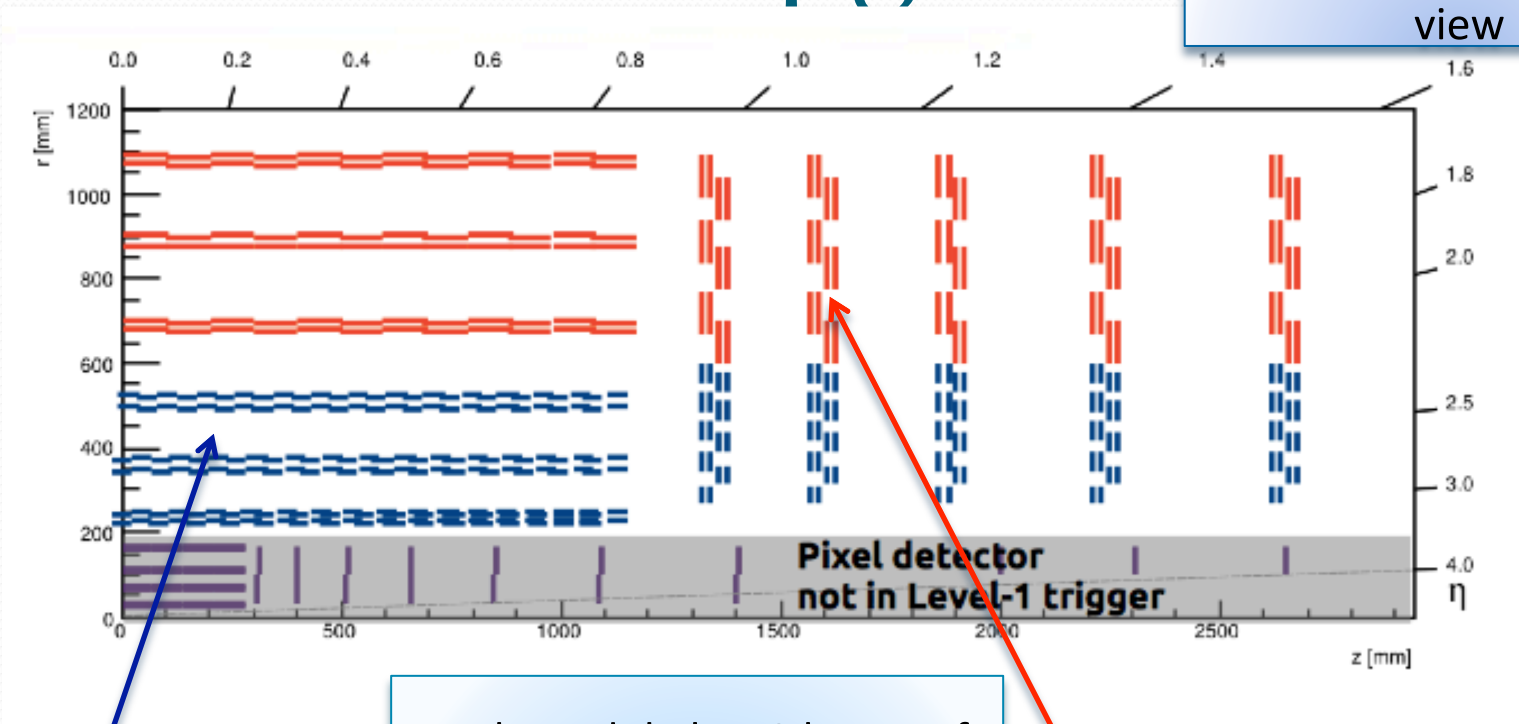
FM-TMT

Data Flow in PP and Track Finder

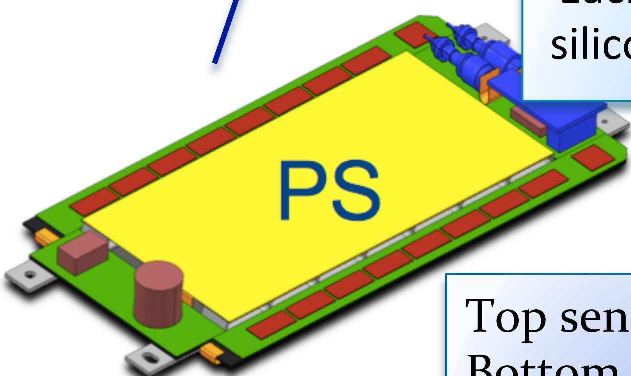


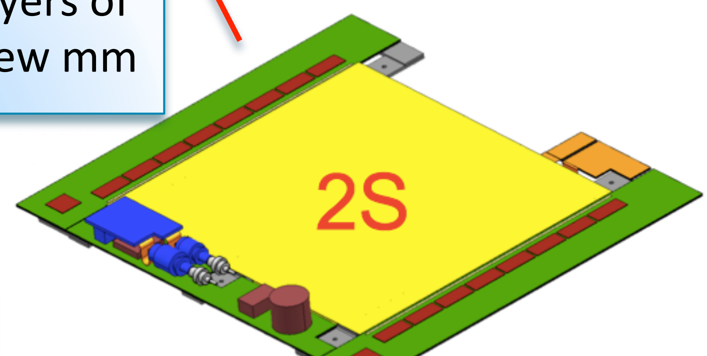
CMS Tracker Upgrade

One quadrant of the r-z view



Each module has 2 layers of silicon separated by few mm





Top sensor: 2x2.5 cm
Bottom sensor: 1.5mm

2x5cm long strips