How can Moore's Law help making better detectors?

Larger and cheaper detectors need smaller and more powerful chips.

A. Marchioro
CERN/PH-ESE

Topics

- How is microelectronics benefitting/changing other “instrumentation” fields
- Scaling and trends
  - Scaling revisited
  - Advanced CMOS technologies
  - Technologies around the corner
    - Finfet
    - Steep sub-threshold devices
- Where to use transistors in instruments and detectors
- Conclusions

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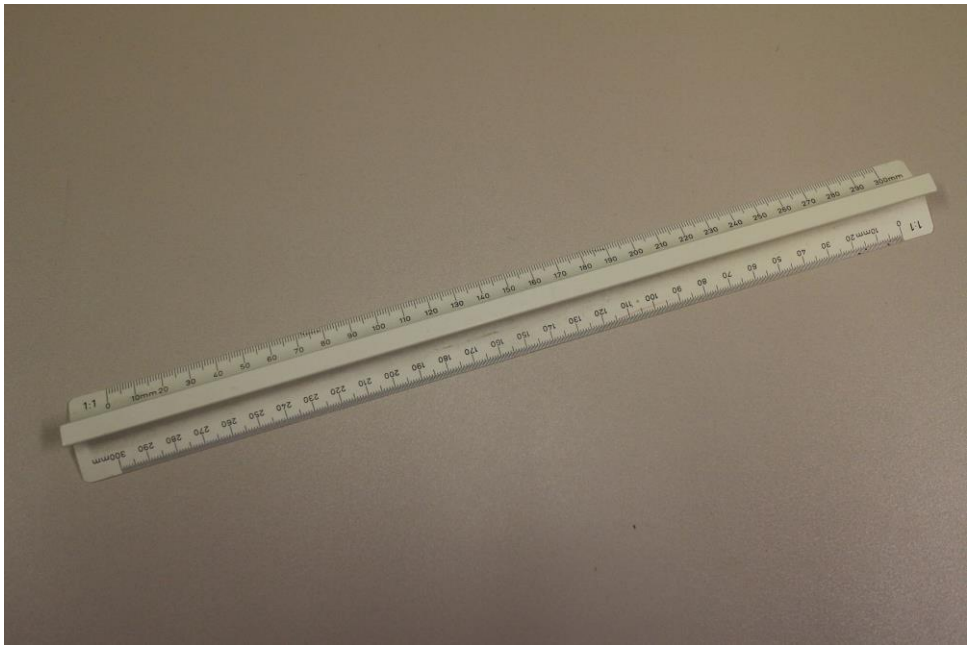
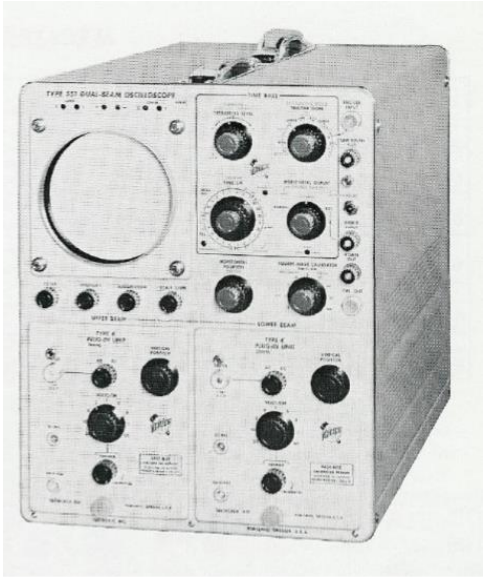
- Conclusions

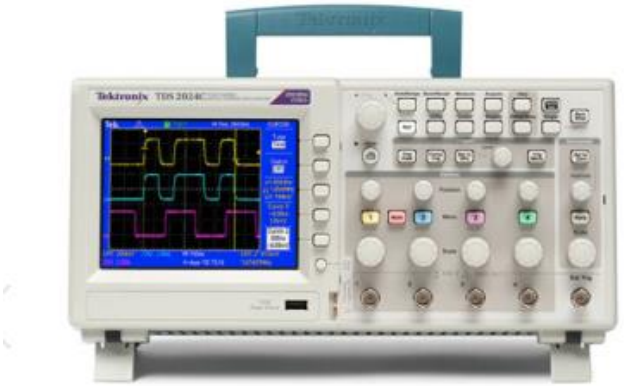
Simplest Instrument of all



Measurement accuracy: ± 1/16” (from Bosch online catalog).
TDC resolution < 10ps.
Very likely SPAD based optical receiver.
Much greater convenience for certain measurements.
…

Instrumentation





	1960 Price	1960 Adj Price	2015 Price
Type 551 dual beam 30 Mc scope	2,600$		
Preamplifier	400$		
Total 2 ch scope	3,400$	21,620$	
TDS2001C quad-ch			~1,000$

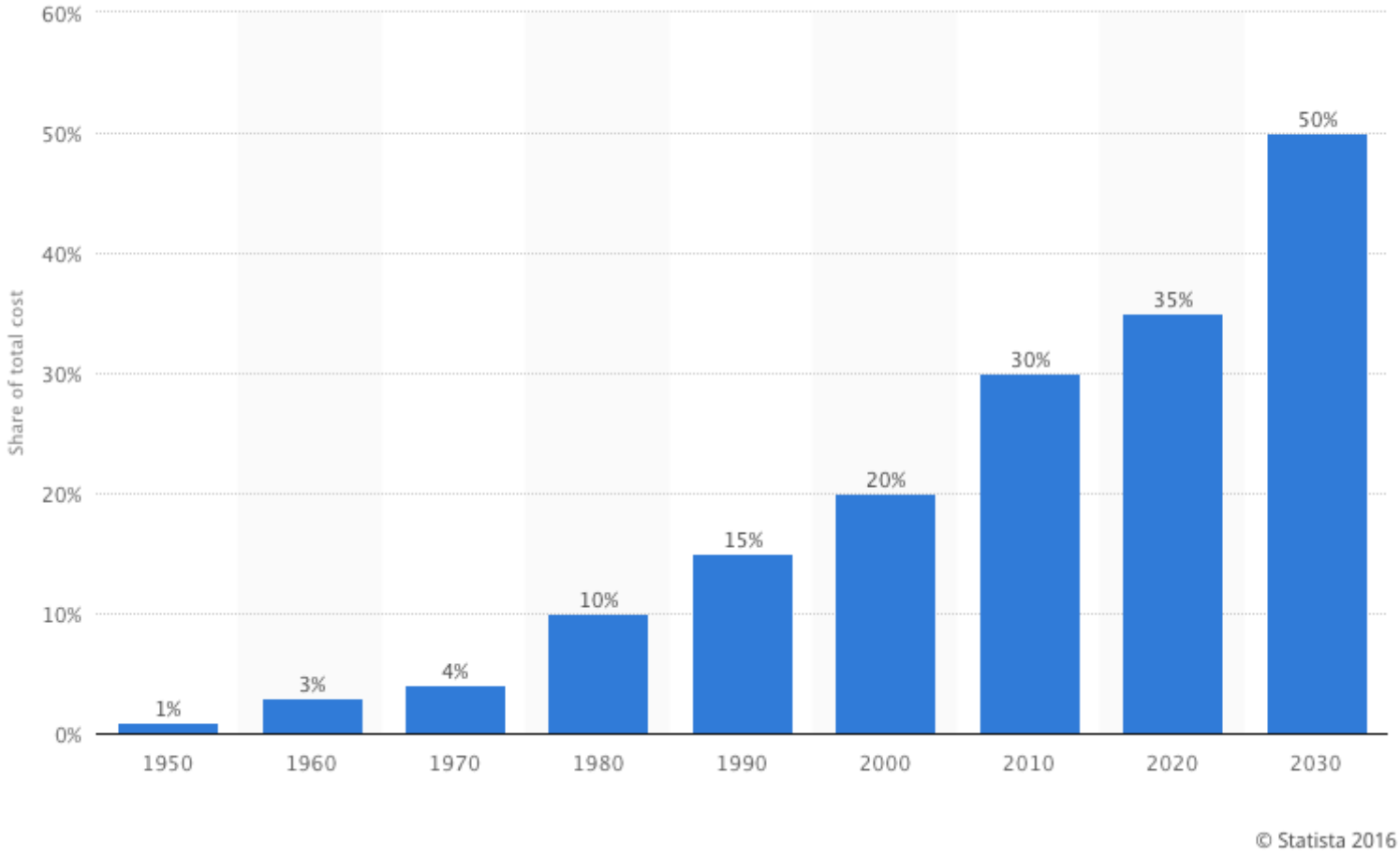
Electronics in cars

- 1965 Car
  - Ignition (really electronics…?)
  - ?

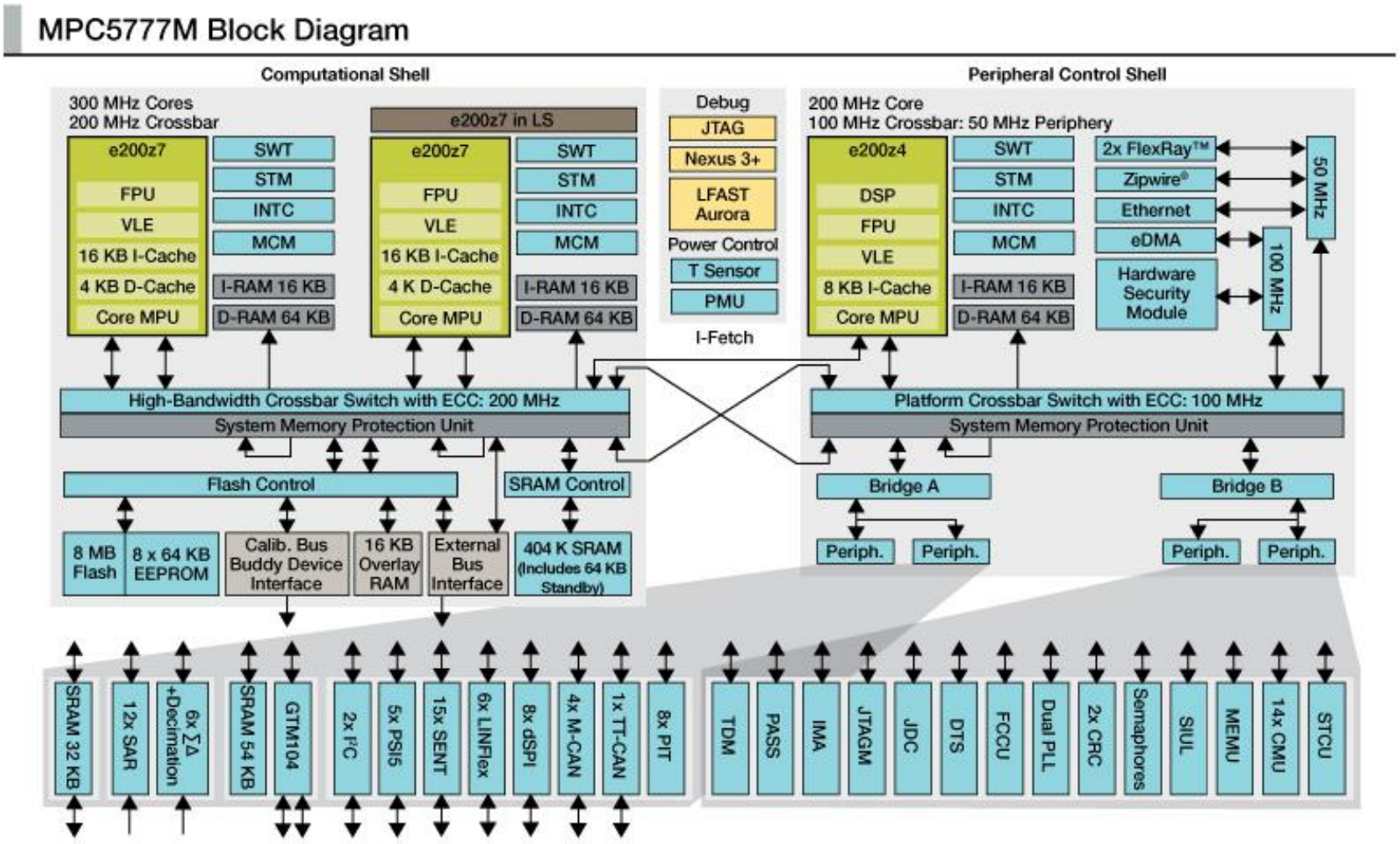
- 2015 Car
  - Engine
    - Fuel Injection
    - Emission control
    - Hybrid engine control
    - …
  - ABS
  - Safety
    - Air bags
    - Emergency brake
  - Transmission
  - Driver Assistance
  - Navigation
  - Cellular Phone
  - Entertainment
  - Audio

Target for 2030 is the full ADAS (Advanced Driver Assistance System), i.e. fully autonomous (co)pilot.

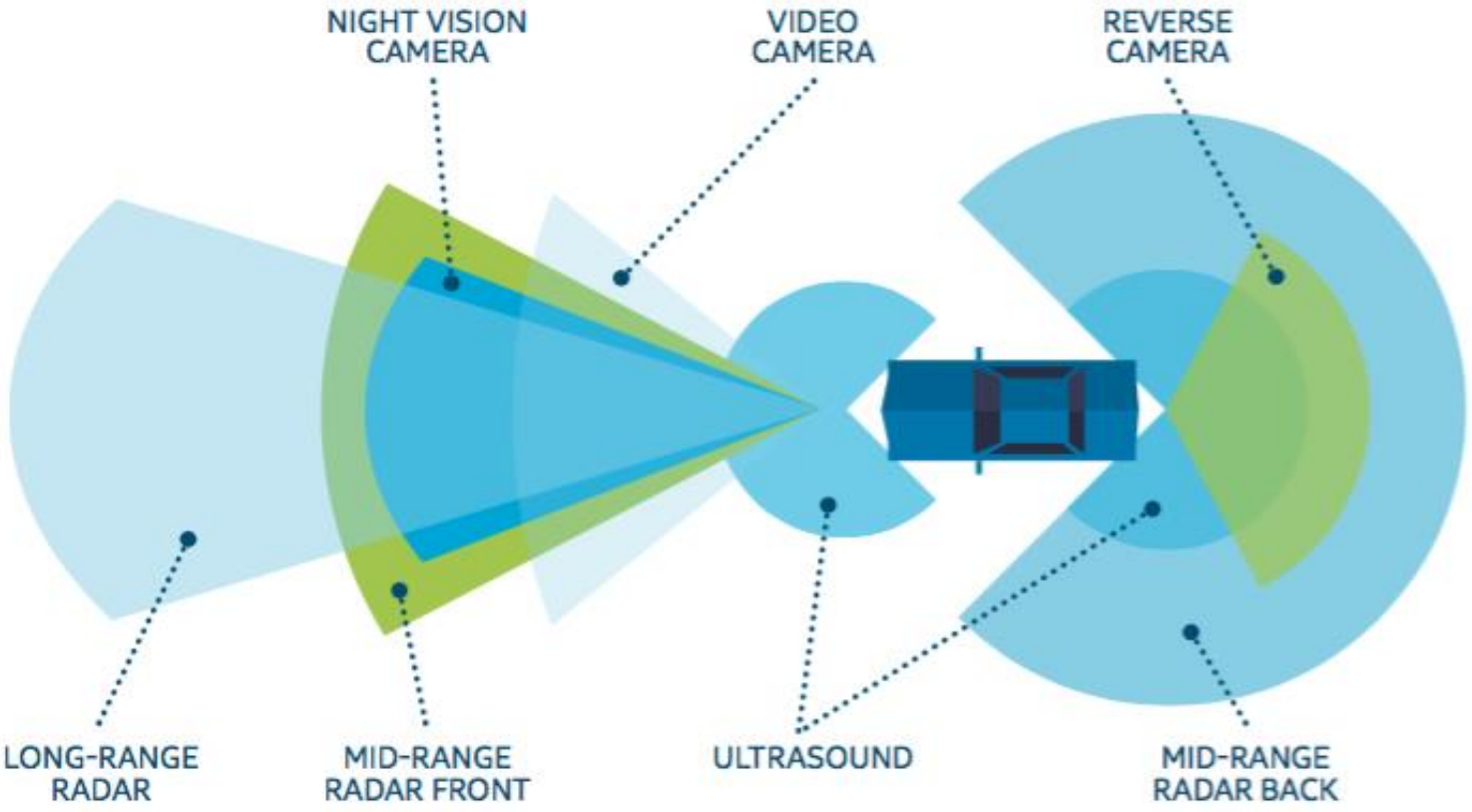
Value of Electronics in Cars



State-of-the-art processor for ADAS



Sensors in ADAS System



From Intel's White Paper: "Advanced Driver Assistant System"

Evolution of FE electronics

AN AMPLIFIER, TRIGGER AND MEMORY FOR SIGNALS FROM PROPORTIONAL WIRE CHAMBERS

J. C. TARLÉ and H. VERWEIJ

CERN, Geneva, Switzerland

Received 29 September 1969

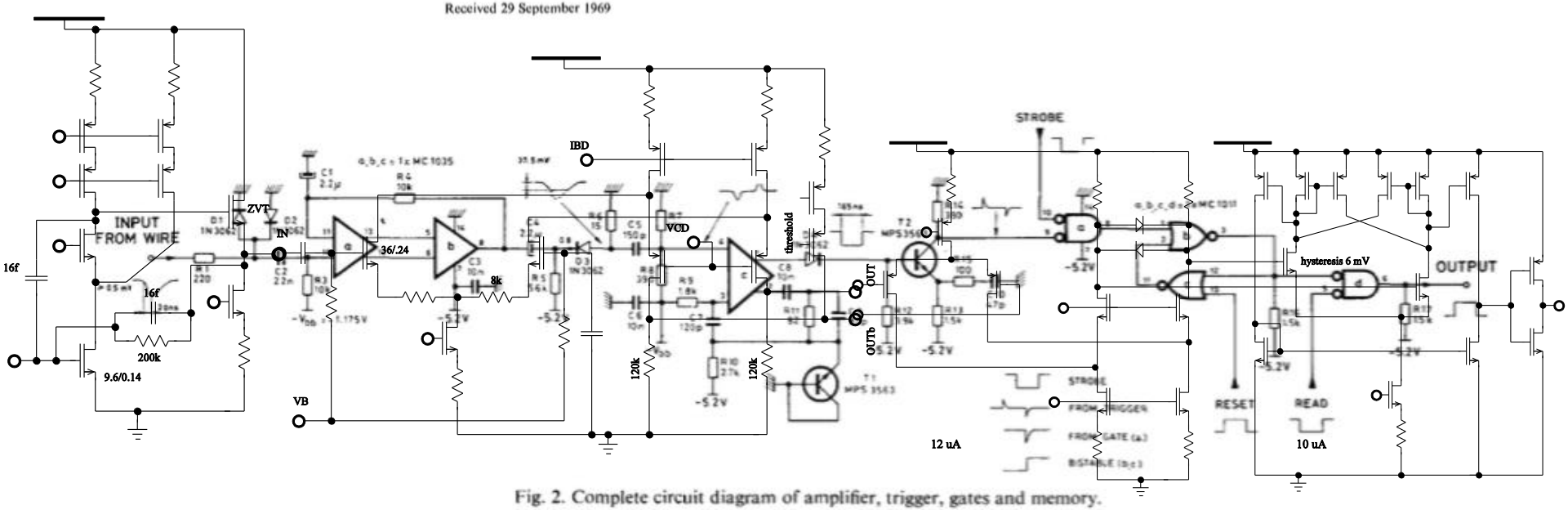
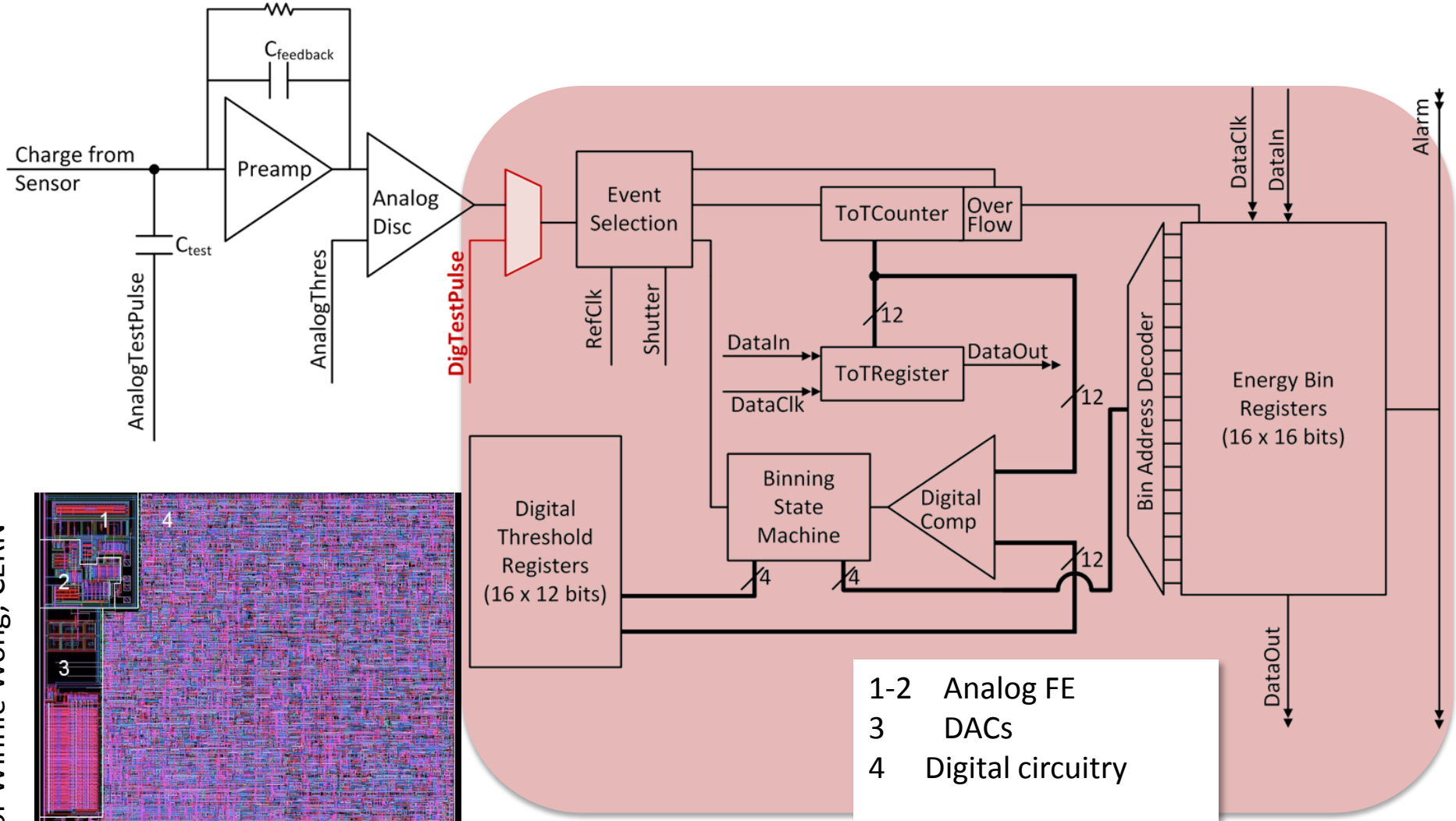


Fig. 2. Complete circuit diagram of amplifier, trigger, gates and memory.

Basically the electronic problem is simple: a current pulse of ≈ 500 nA (or ≈ 1 mV across 2 kΩ, $t_r \approx 20$ nsec, $t_f \approx 200$ nsec) has to be amplified to a level of ≈ 1.0 V, so that it can be conveniently processed. If the

Courtesy of J. Kaplon (CERN) :
Front-end for 2015 MPA chip for CMS

Complex Data Processing in DosePix



Courtesy of Winnie Wong, CERN

1-2 Analog FE
3 DACs
4 Digital circuitry

- 22K transistors/pixel
- 130 nm CMOS
- 8 metals (3 shown here)

Topics

- How is microelectronics benefitting/changing other "instrumentation" fields
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50th anniversary of G. Moore's paper

Electronics, Volume 38, Number 8, April 19, 1965

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 65,000 components on a single silicon chip

By Gordon E. Moore

Director, Research and Development Laboratories, Fairchild Semiconductor division of Fairchild Camera and Instrument Corp.

The future of integrated electronics is the future of electronics itself. The advantages of integration will bring about a proliferation of electronics, pushing this science into many new areas.

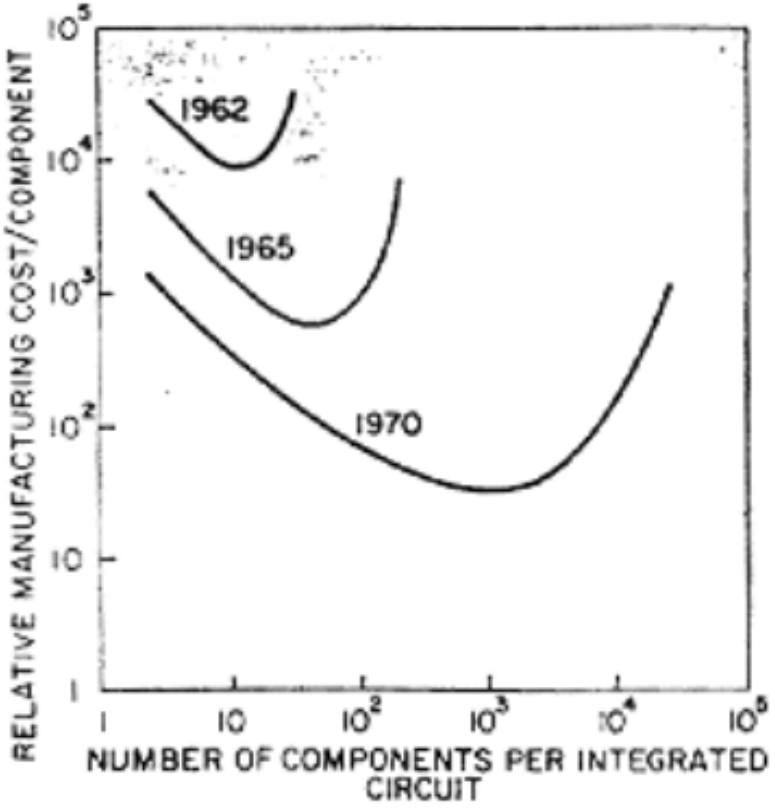
Integrated circuits will lead to such wonders as home computers—or at least terminals connected to a central computer—automatic controls for automobiles, and personal portable communications equipment. The electronic wristwatch needs only a display to be feasible today.

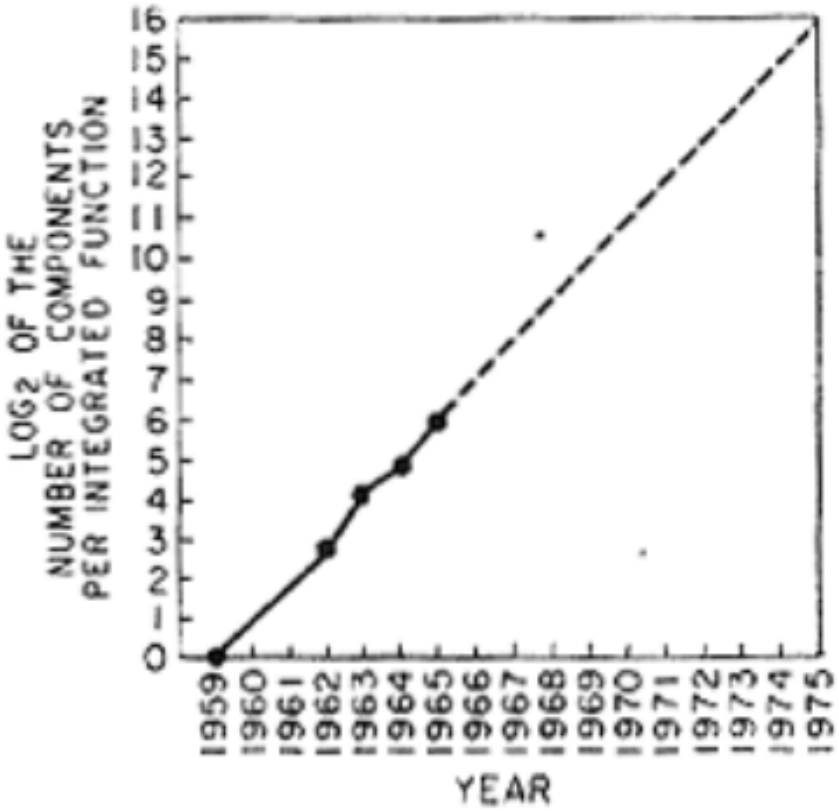
machine instead of being concentrated in a ce
addition, the improved reliability made possible
circuits will allow the construction of larger pro
Machines similar to those in existence today v
lower costs and with faster turn-around.

Present and future

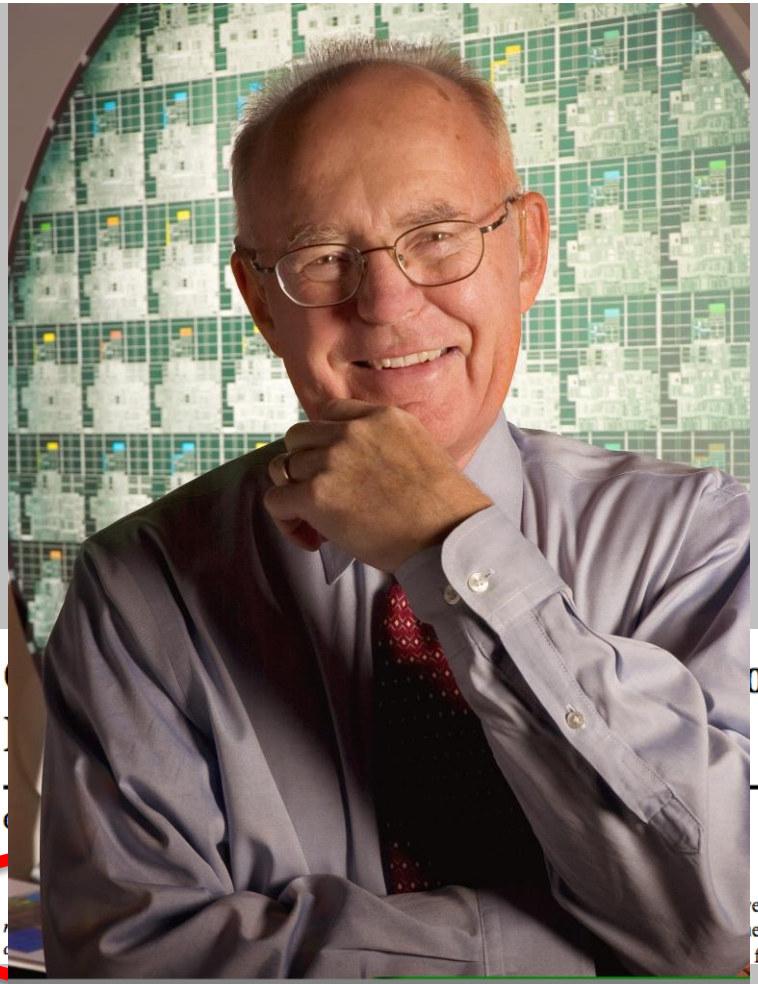
By integrated electronics, I mean all the
nologies which are referred to as microelectro
well as any additional ones that result in elec

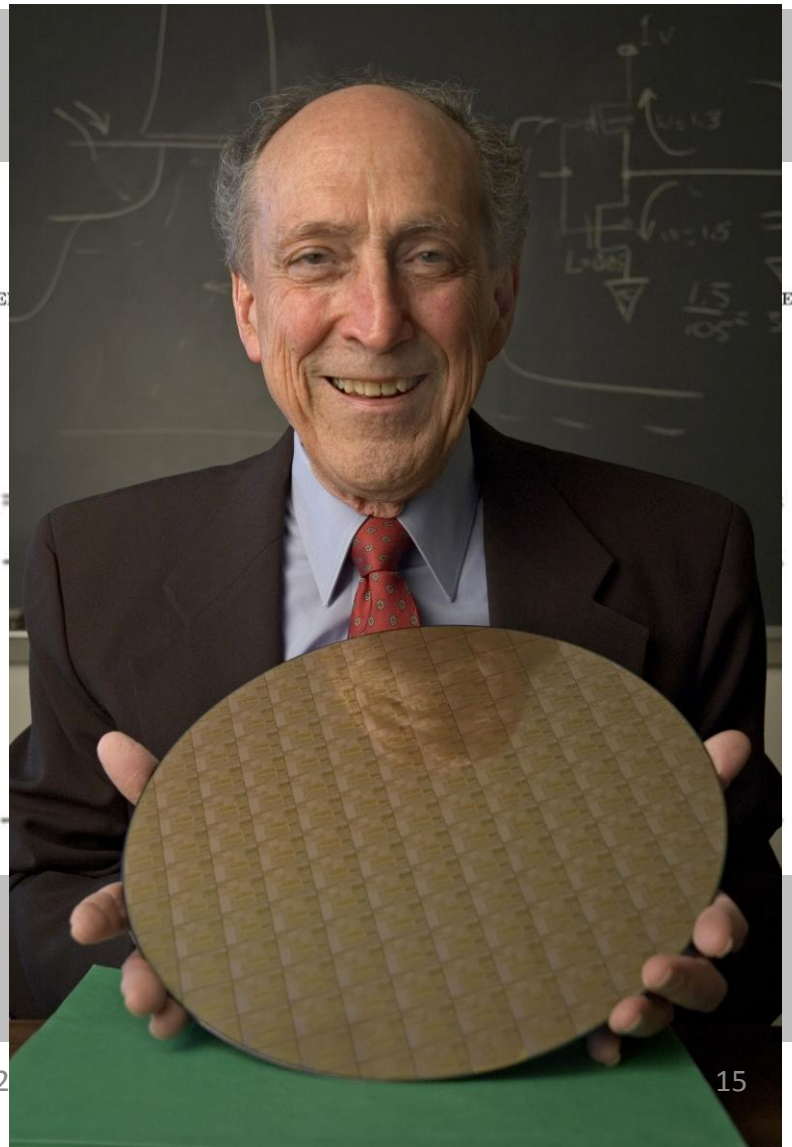
50th anniversary of G. Moore's paper



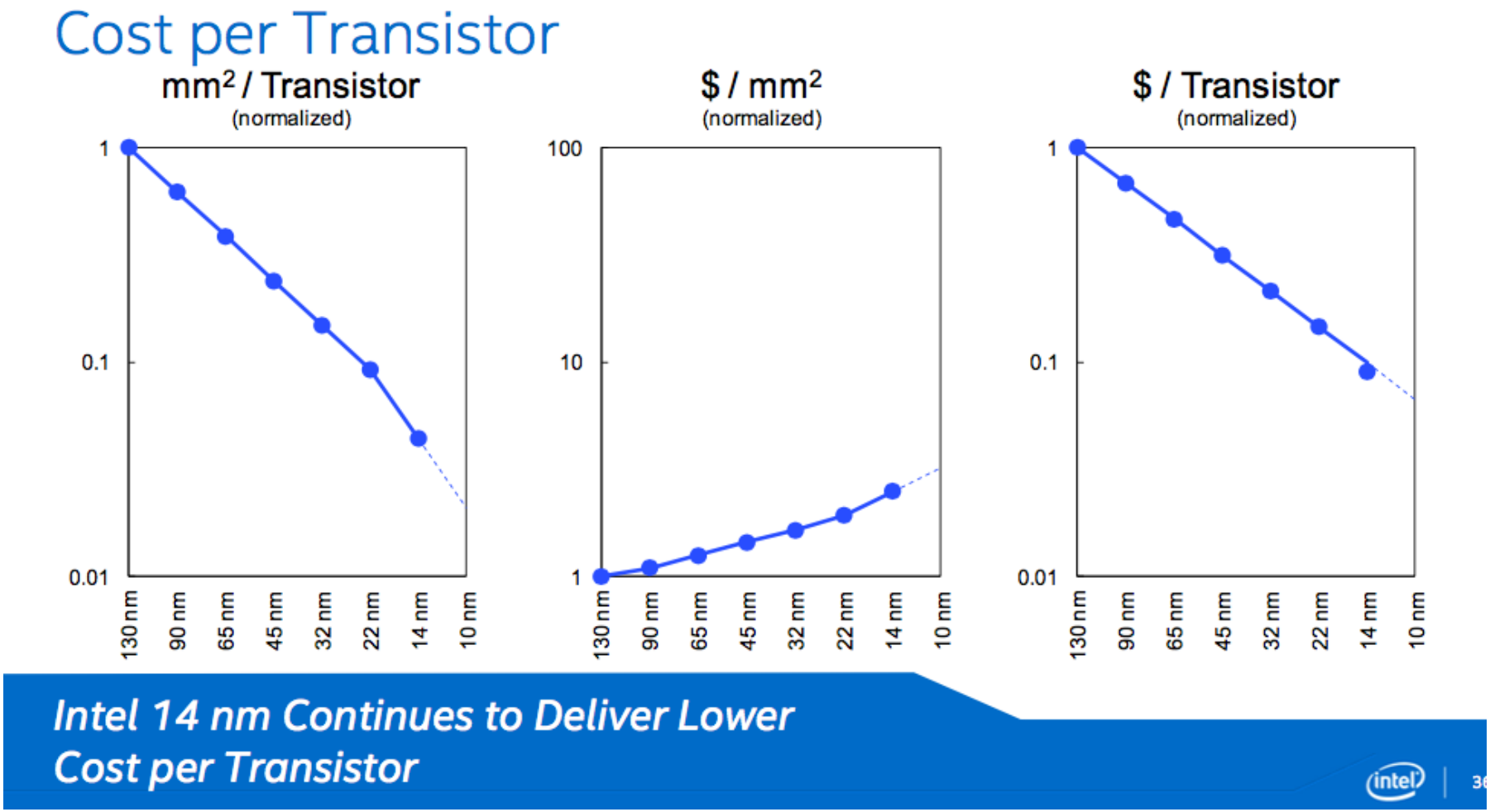


Who's scaling





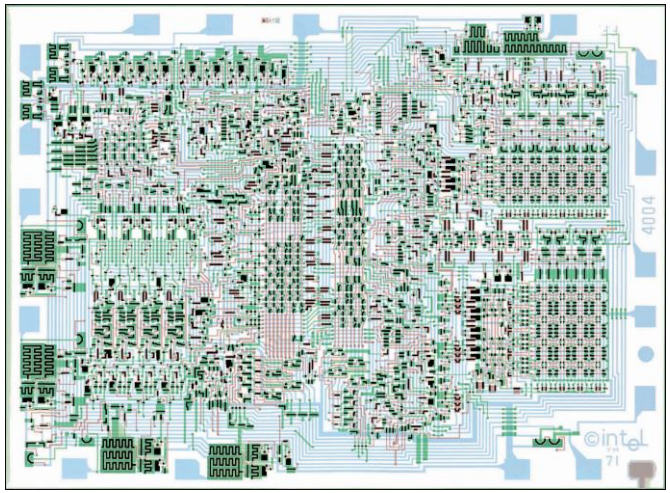
1965 statement still true in 2014

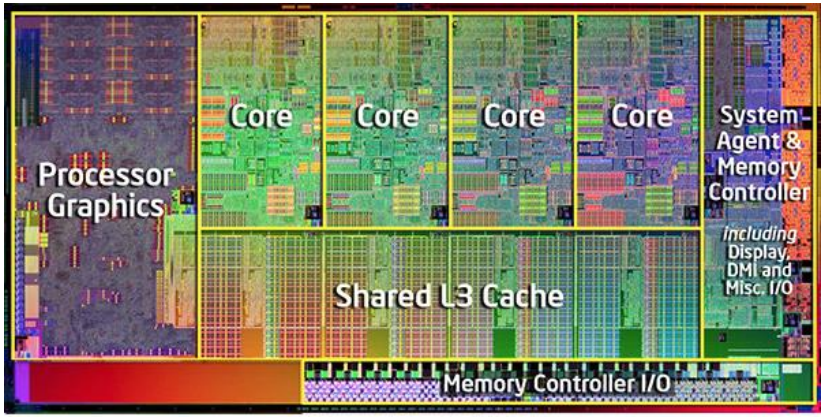


from M. Bohr, Intel IDF 2014

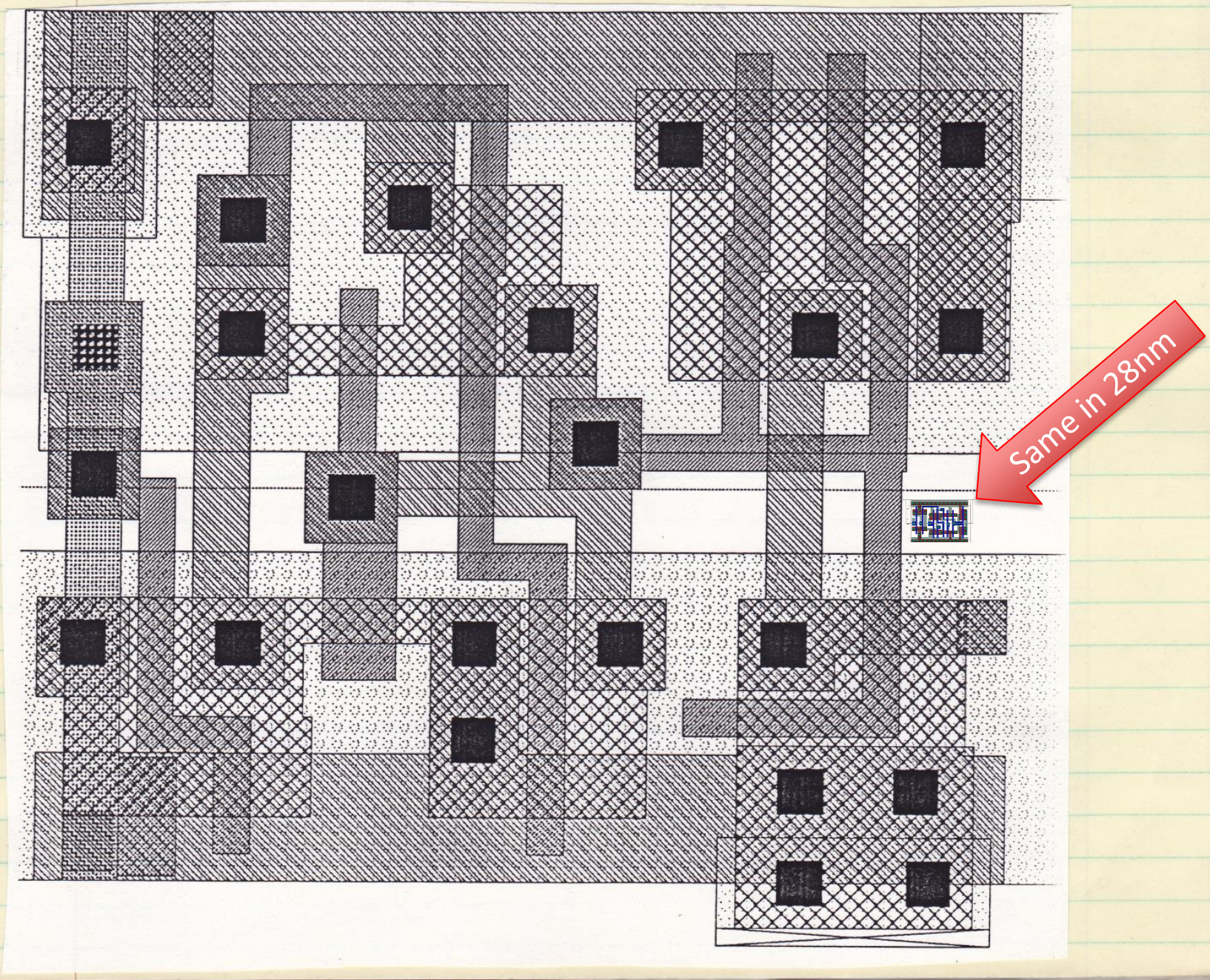
What scaling?

Feature	1970 [1]	2015 [2]	Ratio
Wafer Area	ϕ=4”	ϕ=12”	9 x
Lithography	10 um	14 nm	700 x
Performance	92 KHz	3 GHz	32,000 x
Price/Transistor			1/60,000 x
Energy/Computation	$(1/2\ C_1V_1^2)$	$(1/2\ C_2V_2^2)$	~1/50,000 x





[1] 1970 numbers are based on Intel 4004 processor
[2] 2015 numbers are based on Intel 14 nm technology


Same in 28nm

Scaling revisited

The fundamental objective that the microelectronics industry has pursued in the past 50 years may not have been:

"How to make transistors smaller and smaller at each new generation"

but rather:

"How to make transistors (i.e. functionality) cheaper and cheaper at each new generation"

Topics

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Why do we need advanced technologies?

Power used in (digital) integrated circuit:

$$P = P_{dyn} + P_{static}$$
$$= a \times N \times f \times C \times V_{dd}^2 + I_{leak} \times V_{dd}$$

with:

a : activity factor

N : number of transistors switching

f : operating frequency

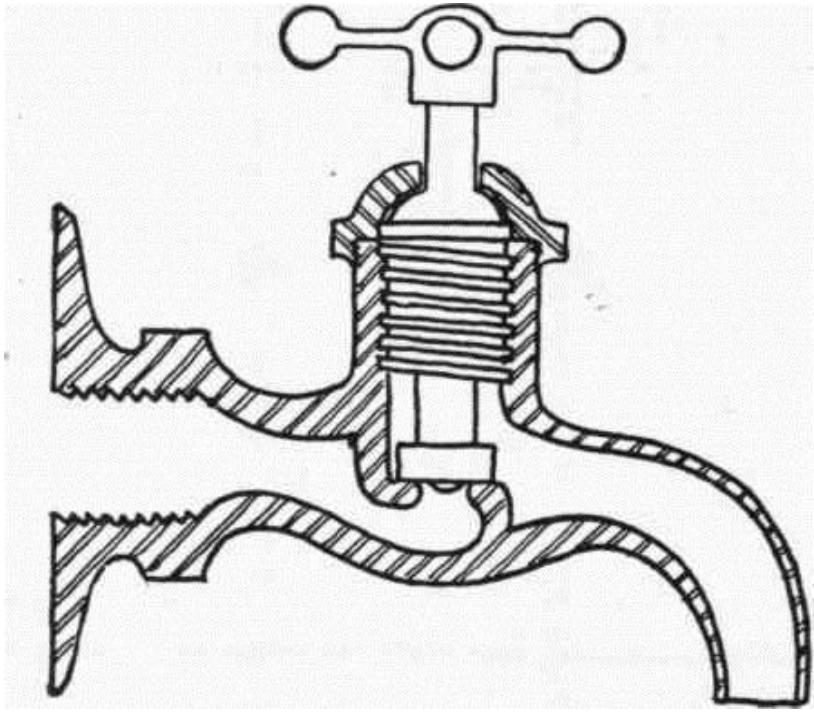
C : wire+transistor capacitance

V_{dd} : operating voltage

I_{leak} : leakage current (i.e. current when device is off)

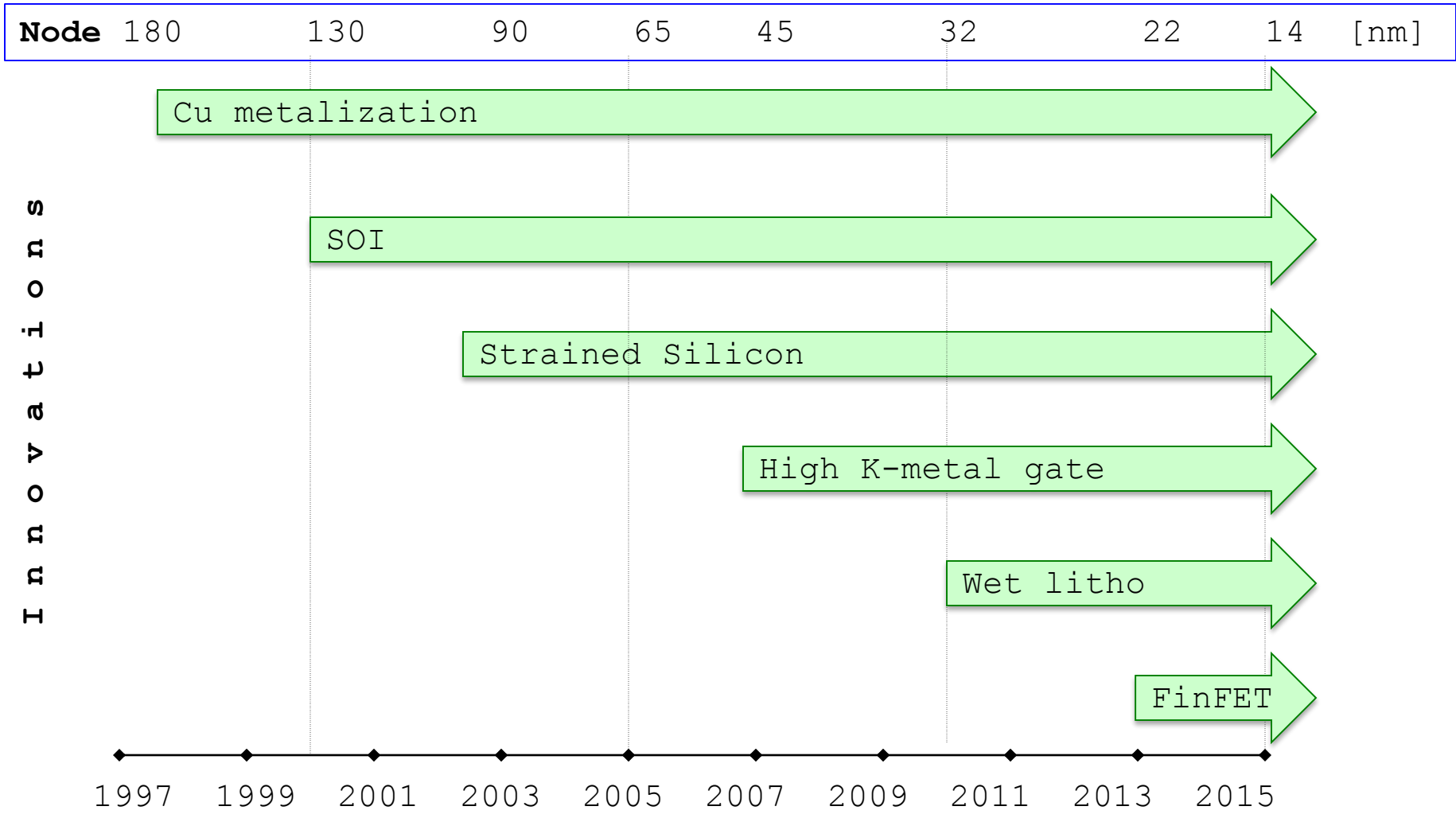
What do we want from a transistor anyway? (sorry engineers…)

- A transistor (a digital transistor) is a device that has to have the following characteristics:
  - to work as a switch (on or off)
  - make a transition between the two states in a time as short as possible
  - has no leakage current when off
  - has to deliver high current when on (to drive strongly the next stage).
    - Unfortunately this it is not uncorrelated from the previous requirement
  - make a transition between the two states with a voltage drive (Vg) as small as possible
  - control terminal should not be influenced by input/output terminal(s)
  - be physically small (otherwise other “parasitics” ruin the party)
  - Must have complementary type (i.e. a second type which is turned on when the first is turned off using the same “control”).



- Good “analog” characteristics are desirable but by far not necessary or even important for the the majority of applications.

Timeline of significant innovations



Technologies around the corner

- FinFet
- FDSOI
- TSVs
- Wafer-to-wafer stacking
- Truly 3D monolithic CMOS
- New materials (III-IV, Ge, GaN, SiC, etc.)
- New phenomena: non kT/q controlled thresholds slopes

Technologies around the corner

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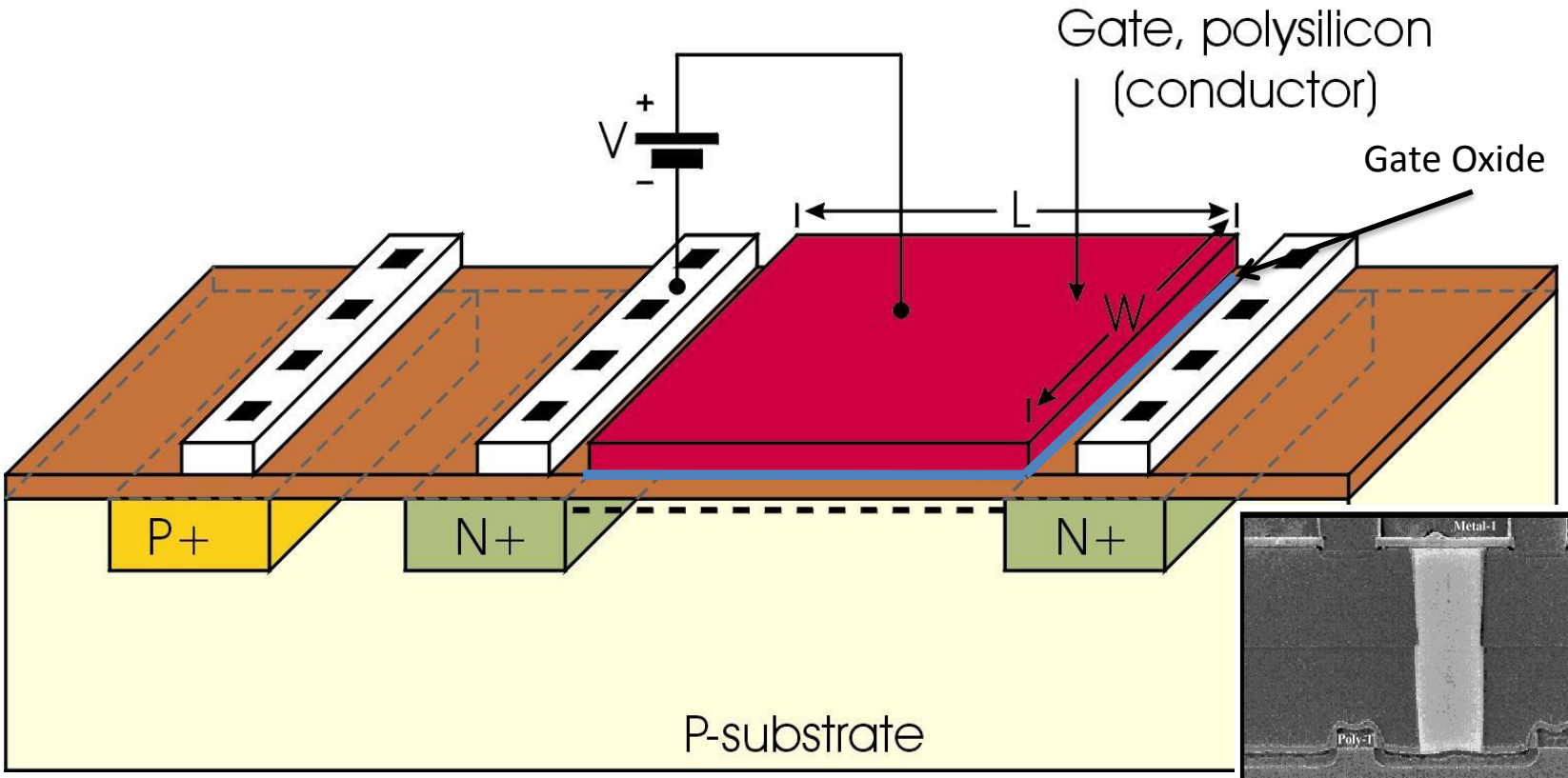
Refresher:
the classical planar transistor



FinFET: a new device with a long incubation

Solid-State Electronics Vol. 27, Nos. 8/9, pp. 827–828, 1984
Printed in Great Britain

0038-1101/84 $3.00 + .00
© 1984 Pergamon Press Ltd.

CALCULATED THRESHOLD-VOLTAGE CHARACTERISTICS OF AN XMOS TRANSISTOR HAVING AN ADDITIONAL BOTTOM GATE

(*Received* 30 *May* 1983; *in revised form* 24 *August* 1983)

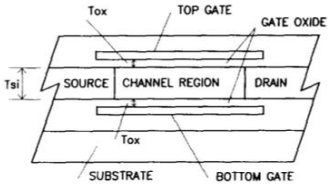


Fig. 1. Schematic cross-sectional structure of an XMOS transistor having an additional bottom gate which is symmetrically placed to a top gate with a channel region between them. "*X*" originates from Greek capital letter of xi as this structure resembles its shape.

Electronic Device Division, Electrotechnical Laboratory, Sakura-mura, Ibaraki, 305, Japan

T. SEKIGAWA and Y. HAYASHI

Hitachi(?)– 1984

NEW EFFECTS OF TRENCH ISOLATED TRANSISTOR USING SIDE-WALL GATES

K. Hieda, F. Horiguchi, H. Watanabe, K. Sunouchi, I. Inoue and T. Hamamoto

VLSI Research Center, Toshiba Corporation
Komukai, Saiwai-ku, Kawasaki, 210 Japan

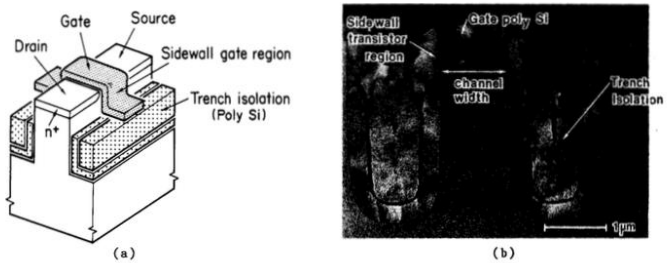


Fig. 1. (a) Schematic cross section of trench isolated transistor using side-wall gates (TIS). (b) SEM micrograph of the cross section along the direction of gate width.

Toshiba– 1987

IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 38, NO. 6, JUNE 1991 1419

Impact of the Vertical SOI "DELTA" Structure on Planar Device Technology

Digh Hisamoto, *Member, IEEE*, Toru Kaga, *Member, IEEE*, and Eiji Takeda, *Senior Member, IEEE*

***Abstract*—A fully depleted lean channel transistor (DELTA) with its gate incorporated into a new vertical ultra-thin SOI structure is presented. In the deep-submicrometer region, selective oxidation produces and isolates an ultra-thin SOI MOSFET that has high crystalline quality, as good as that of conventional bulk single-crystal devices. Experiments and three-dimensional simulations have shown that this new gate structure has effective channel control, and that the vertical ultra-thin SOI structure provides superior device characteristics: reduction in short-channel effects, minimized subthreshold swing, and high transconductance.**

is required. Moreover, it is evident that these st
are difficult to contact to the substrate, and thus suf
a substrate floating effect.

The second concept makes the device thickness
than the depletion-layer width to intentionally dep
channel. This can be done with thin-film SOI tech
such as SIMOX and recrystallization [7], [8]. T
cept is ideal because the structure has the same n
conventional MOSFET's, however, it requires
ultra-thin SOI substrates, a difficult task. Still, a

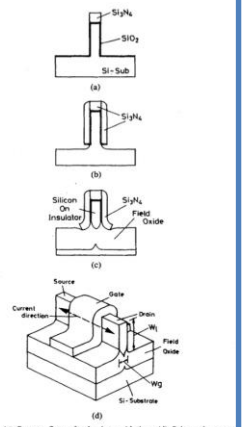


Fig. 1. (a)–(c) Process flow of selective oxidation. (d) Schematic cross section of DELTA.

Hitachi – 1991

Monte Carlo Simulation of a 30 nm Dual-Gate MOSFET: How Short Can Si Go?

D. J. Frank, S. E. Laux and M. V. Fischetti

IBM Research Division, T. J. Watson Research Center
P.O. Box 218, Yorktown Heights, NY 10598

Conclusions

In summary, it appears that high performance Si MOSFETs can be scaled down to gate lengths of order 30 nm. Such devices are still suitable for digital circuitry, and may have transconductances as high as 2300 mS/mm and ring oscillator speeds near 1 ps. The technology needed to do this includes thickness control of very thin layers, dual gate alignment, very abrupt doping profiles and gate work function control. A high thermal conductivity method of removing heat from such devices would also need to be found.

References

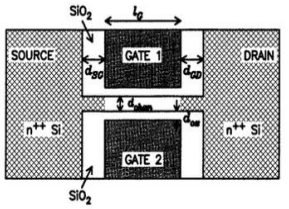
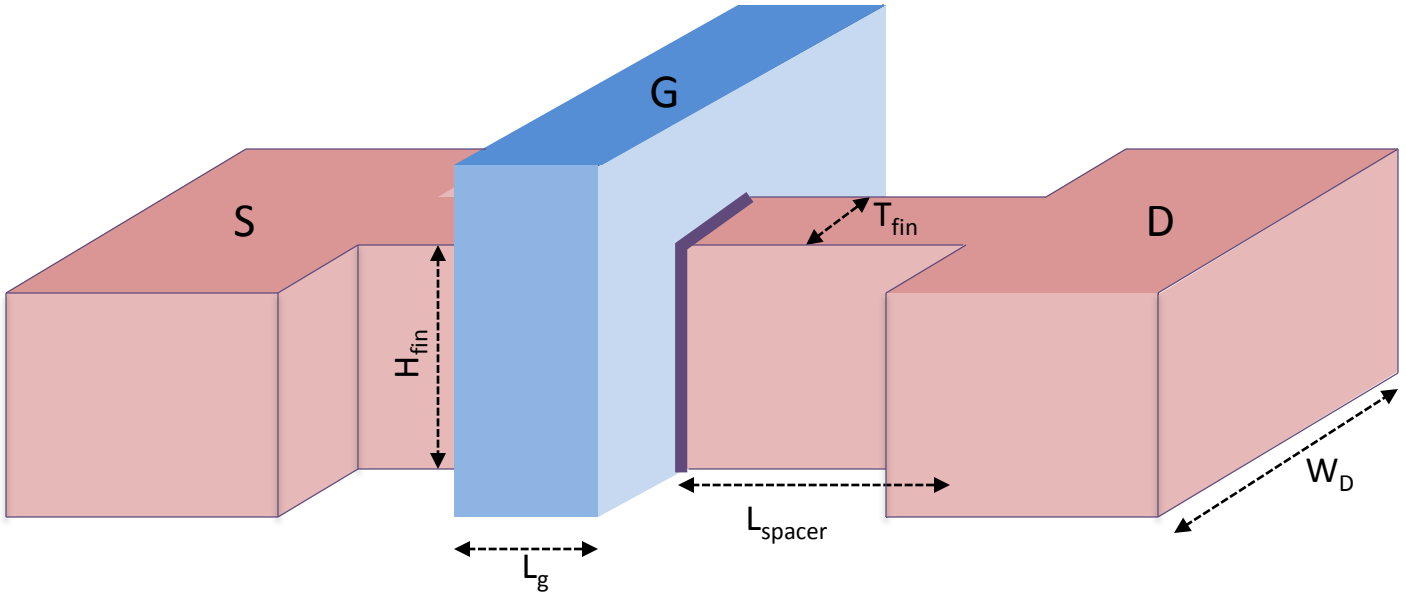


Fig. 1. Dual-gate MOSFET cross-section. Our simulations all use $d_{ox} = 3$ nm, $d_{SD} = d_{GD} = 0.3 \times l_G$, and 10^{20} cm^{-3} n-type source and drain doping.

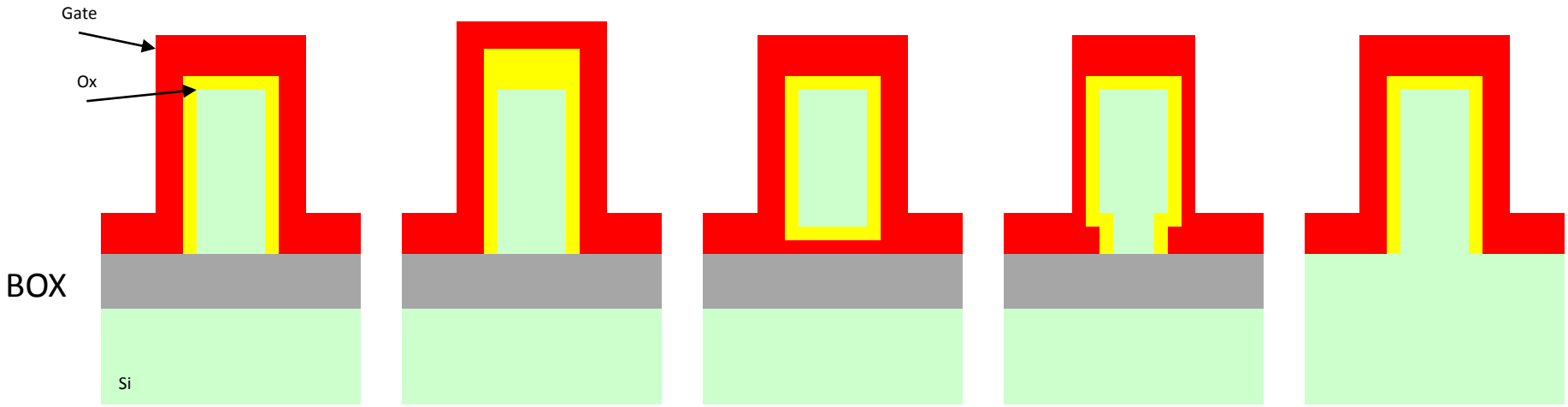
IBM – 1992

FinFET Detail

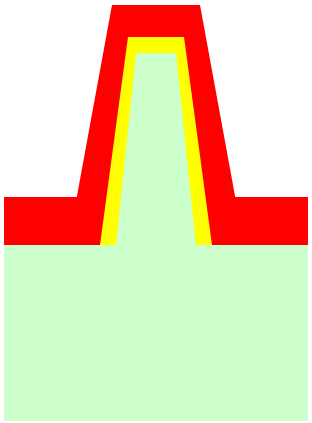


- L_g same for all devices
- $H_{fin} >> T_{fin}$
- Top Ox same as Lateral Ox -> Tri-Gate,
  - if >> Lateral Oxide -> FinFET
- $W_{fin} = 2 * L_{fin} (+T_{fin})$
- $W_{S,D} >> T_{fin}$

Multi-Gate variations

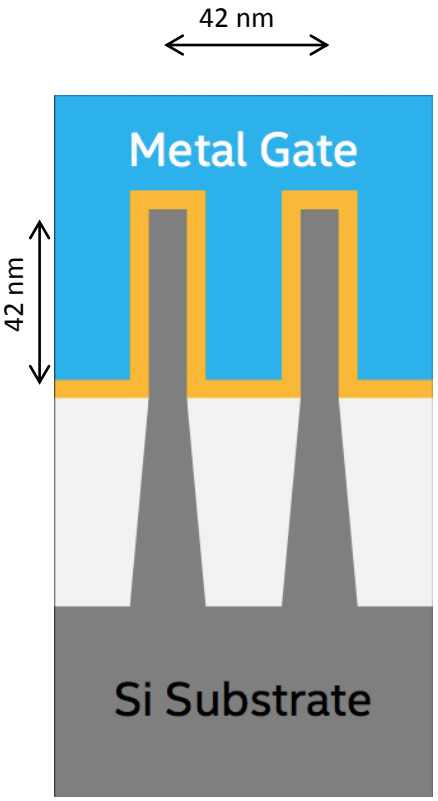


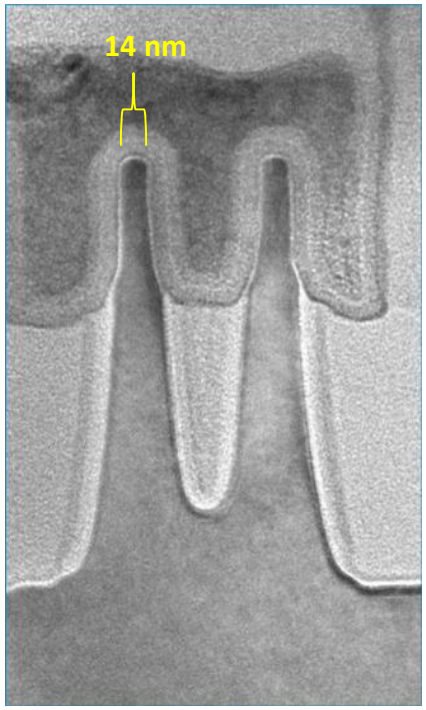
SOI tri-gate | SOI two-gate | Gate-All-Around | Omega-gate | Si-bulk tri-gate

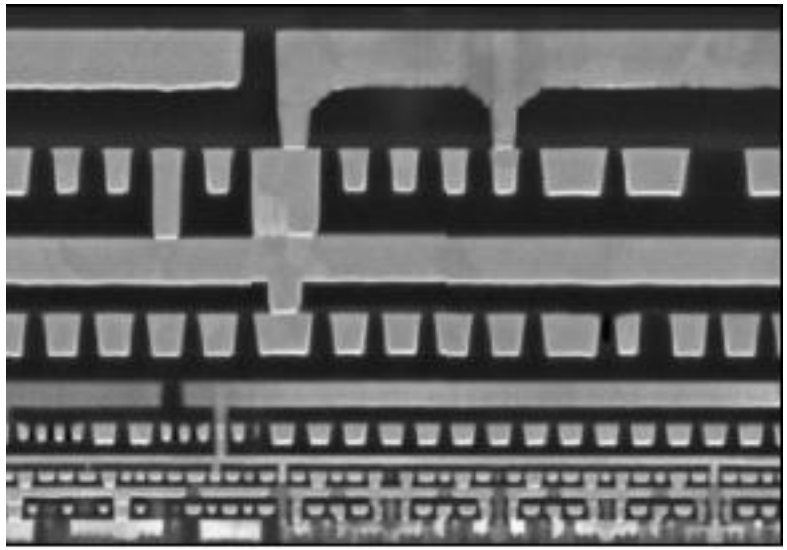


Intel's tri-gate

Intel TRI-Gate







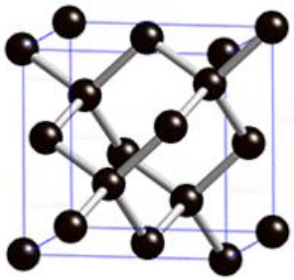
Metalization detail

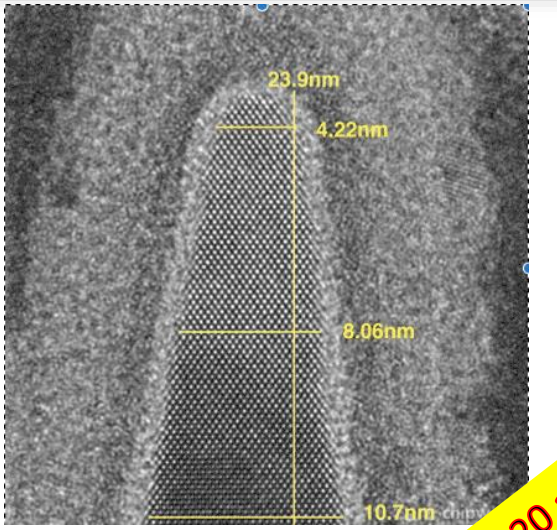
Source: Intel

Typical FinFET dimensions

From the ITRS 2011 report

Year of Production	*2013*	*2015*	*2017*	*2019*	*2021*	*2023*	*2025*	*2028*
FinFET Fin Width (new) (nm)	**7.6**	**7.2**	**6.8**	**6.4**	**6.1**	**5.7**	**5.4**	**5.0**



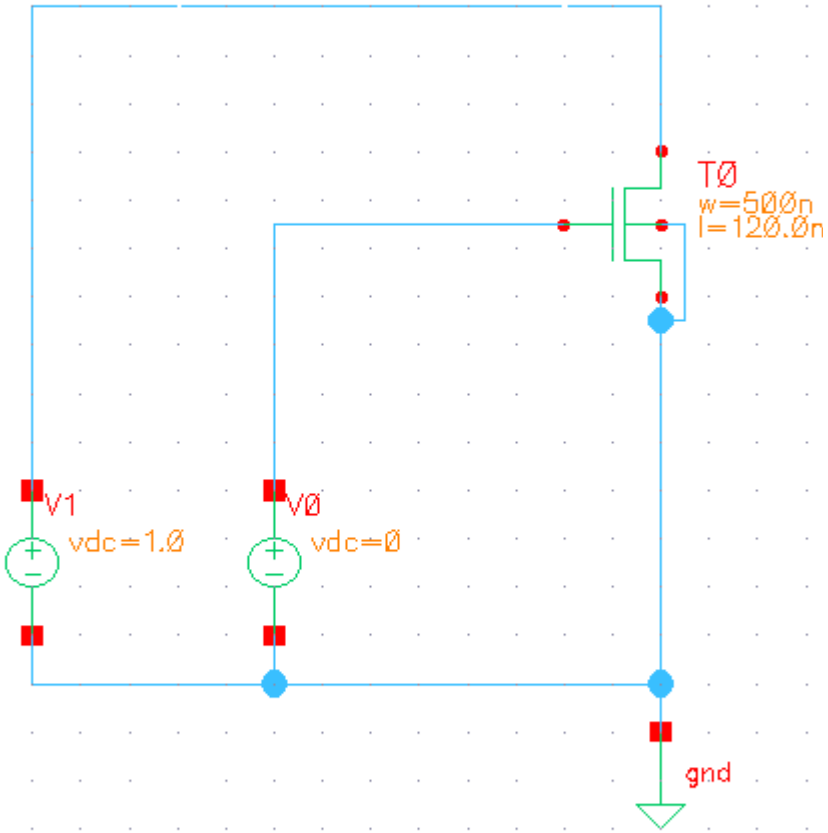


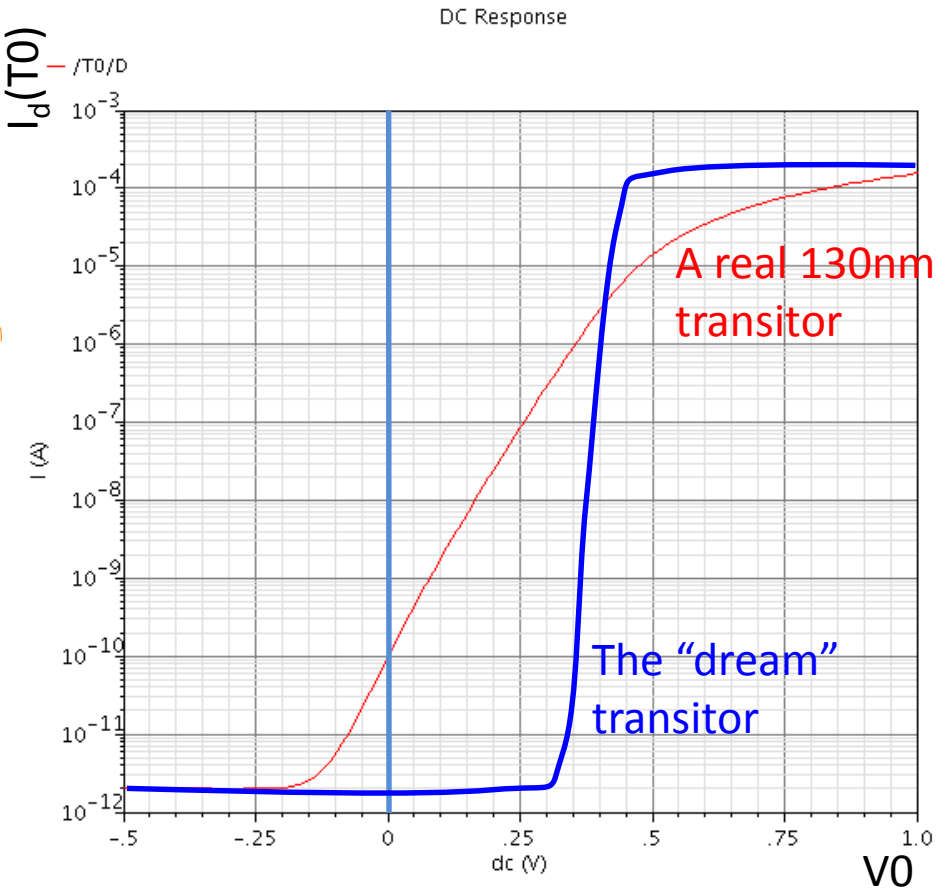
This FinFET has EXACTLY 20 atoms across at half-height

Technologies around the corner

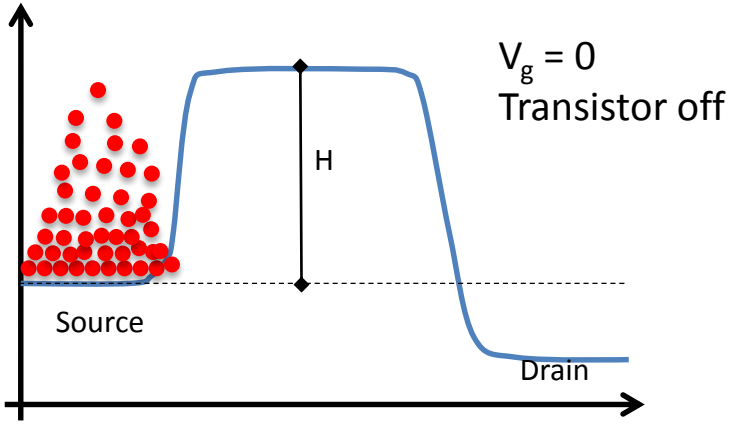
- FinFet
- FDSOI
- TSVs
- Wafer-to-wafer stacking
- Truly 3D monolithic CMOS
- New materials (III-IV, Ge, GaN, SiC, etc.)
- New phenomena: non kT/q controlled thresholds slopes

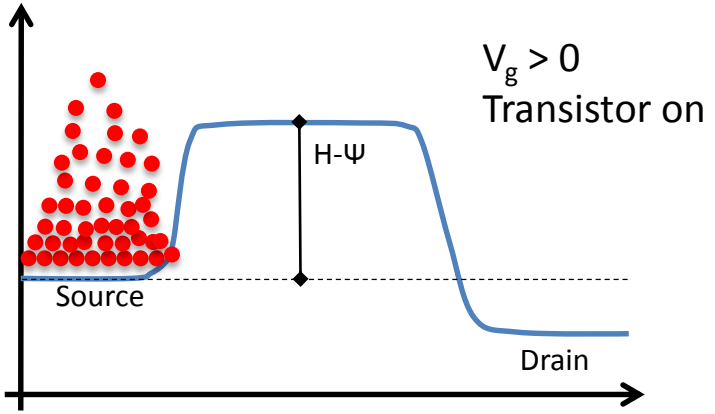
Intro: about switching transistors





The kT/q limit, or the "Boltzmann tyranny"





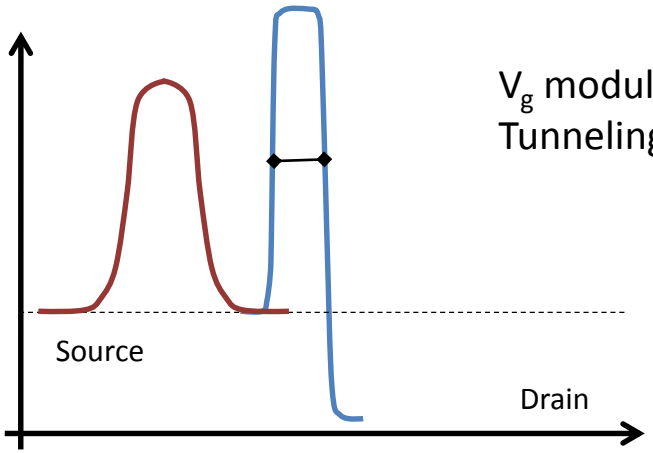
To change the current in a MOS transistor by one order of magnitude, it turns out that the gate voltage has to be changed by:

$$SS = \ln(10)\frac{kT}{q}$$

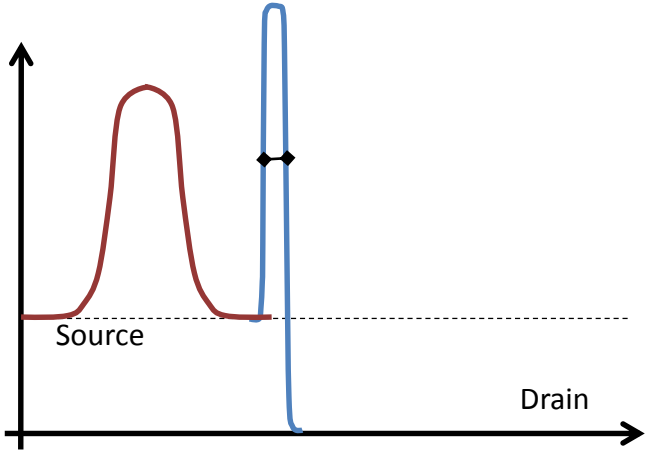
If the static leakage in a multi-million transistor chip has to be $\frac{I_{off}}{I_{on}} < 10^{-6}$ then the transistion region between off and on will have to span at least:

$$V_{TRAN} = 6 \times \ln(10)\frac{kT}{q} \gg 360mV$$

Quantum tunneling devices



V_g modulates the Tunneling width



It turns out that certain devices can actually be built with atomic dimensions where band-to-band tunneling can be achieved with SS < 60 mV/decade.

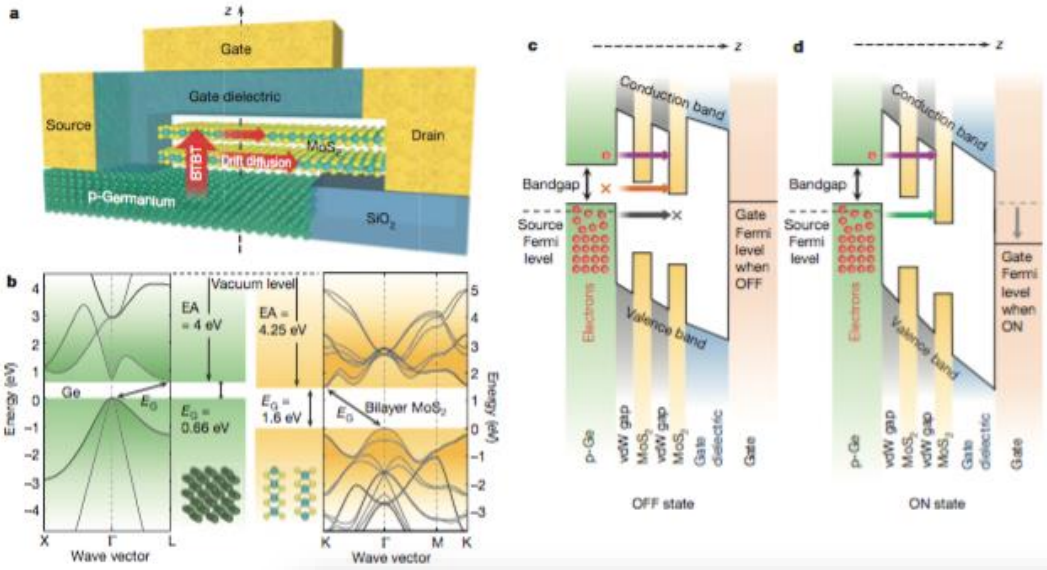
Sub 60mV/decade FETs

LETTER

doi:10.1038/nature15387

A subthermionic tunnel field-effect transistor with an atomically thin channel

Deblina Sarkar[1], Xuejun Xie[1], Wei Liu[1], Wei Cao[1], Jiahao Kang[1], Yongji Gong[2], Stephan Kraemer[3], Pulickel M. Ajayan[2] & Kaustav Ban



threshold swing, such as band-to-band tunnelling[10–16]. Here we demonstrate band-to-band tunnel field-effect transistors (tunnel-FETs), based on a two-dimensional semiconductor, that exhibit steep turn-on; subthreshold swing is a minimum of 3.9 millivolts per decade and an average of 31.1 millivolts per decade for four decades of drain current at room temperature. By using highly

Scaling summary:
Is scaling really finished in industry?

- If one calls “scaling” only the (2D) miniaturization of transistors, then definitively Dennard’s scaling is closer to saturation than Moore’s.

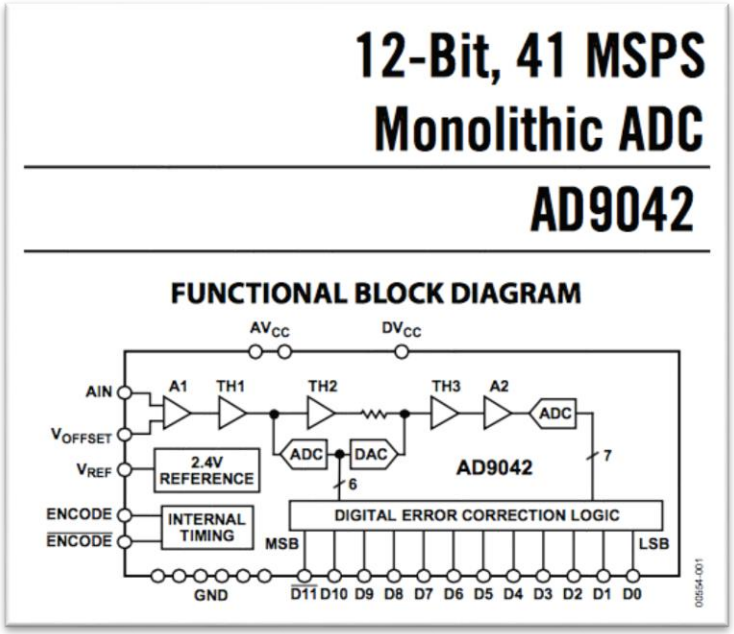
- If instead one calls scaling the reduction in cost (somehow) of the $/transistor on a chip, then several more generations are ahead of us.

Topics

- How is microelectronics benefitting/changing other “instrumentation” fields
- Scaling and trends
  - Scaling revisited
  - Advanced CMOS technologies
  - Technologies around the corner
    - Finfet
    - Steep sub-threshold devices
- Where to use transistors in instruments and detectors
- Conclusions

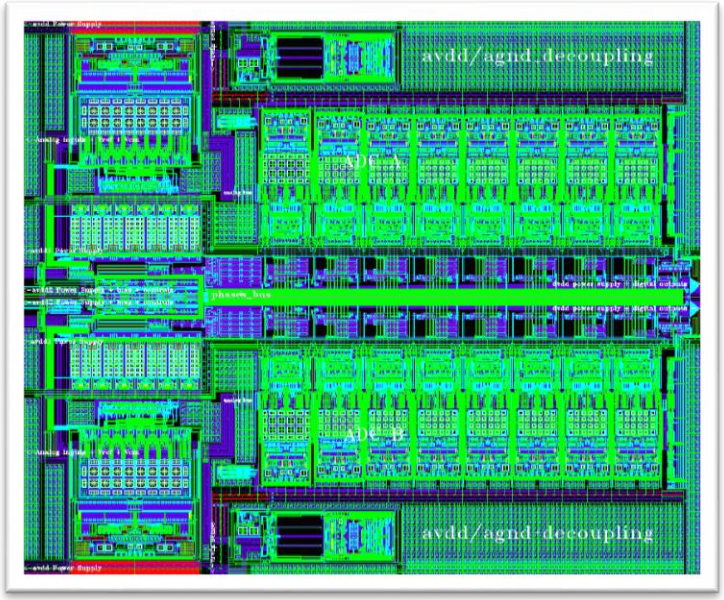
RH ADCs, circa 2002

Commercial



- Bipolar tech
- 595 mW, one channel
  - FOM: 7.2 pJ/conv

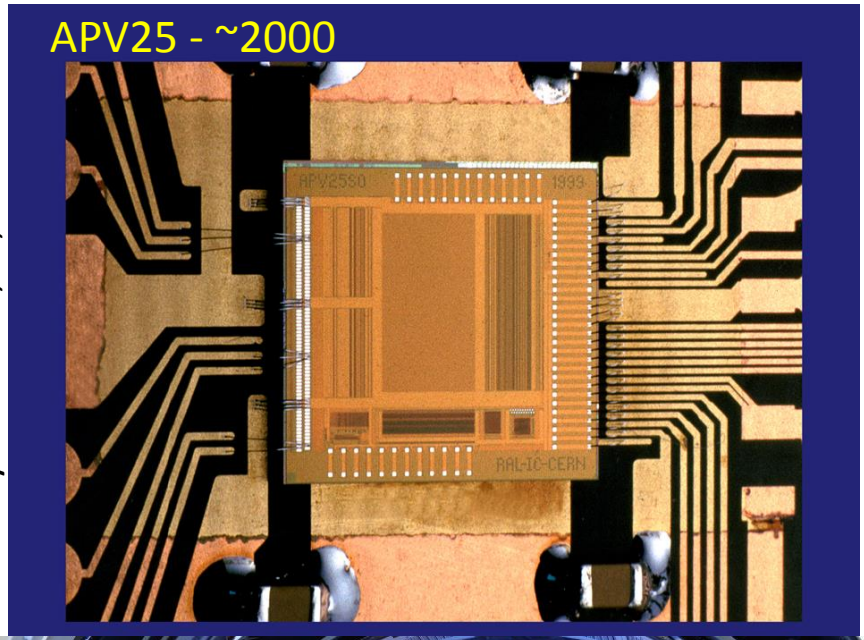
Custom (designed for CMS)



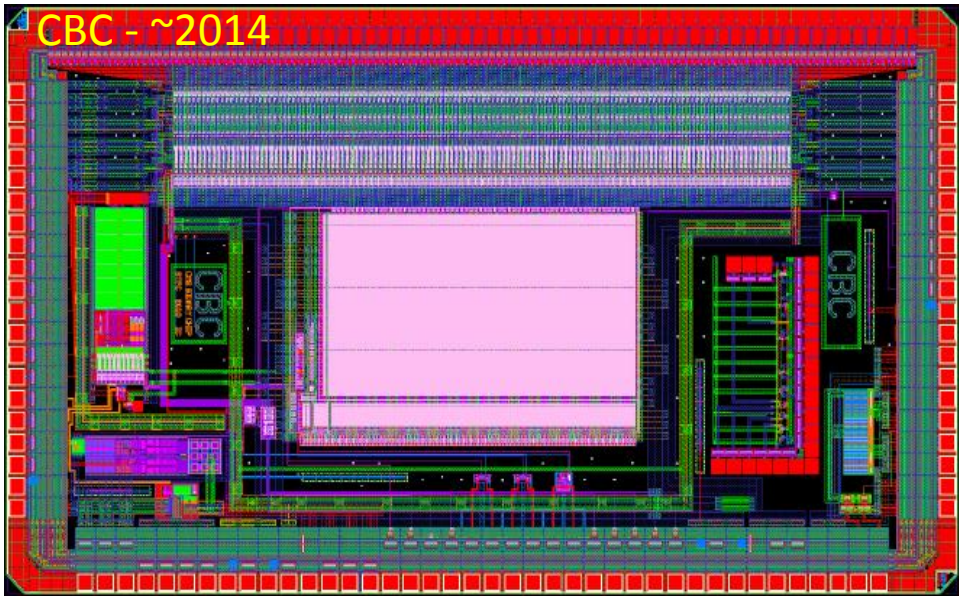
- CMOS
- 120 mW / channel:
  - FOM: 1.4 pJ/conv
- No need for input and output

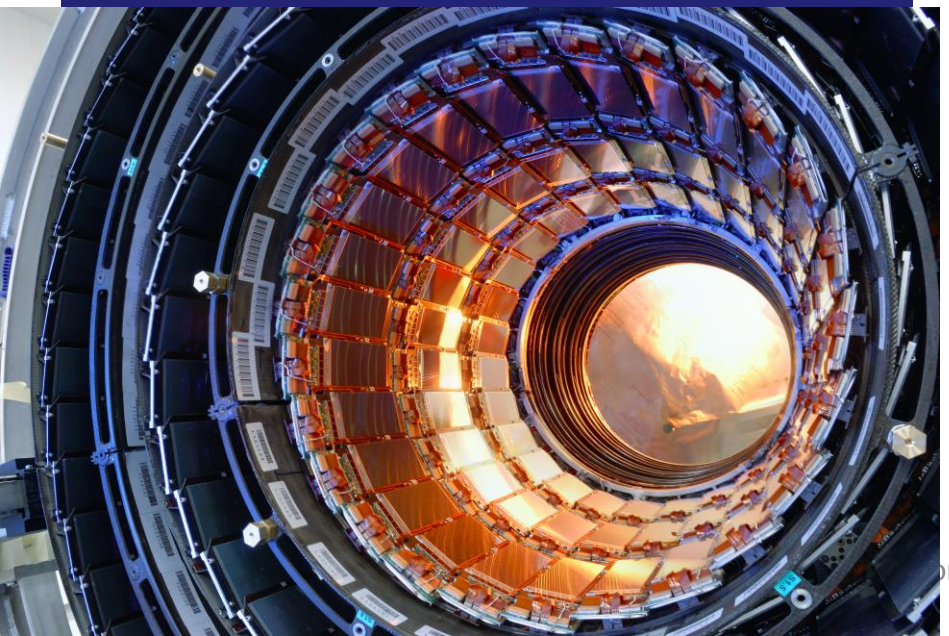
2015 State-of-the-art published ADC FOM: ~ 0.01 pJ/conv

Tracker FE chips: APV



Courtesy of G. Hall, IC, UK



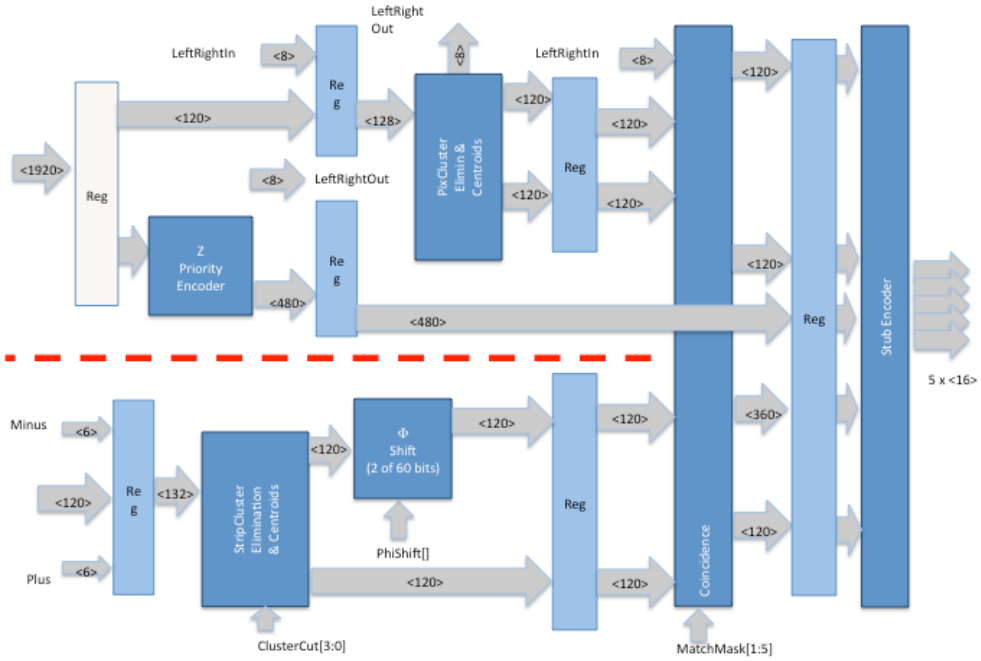


CBC key features

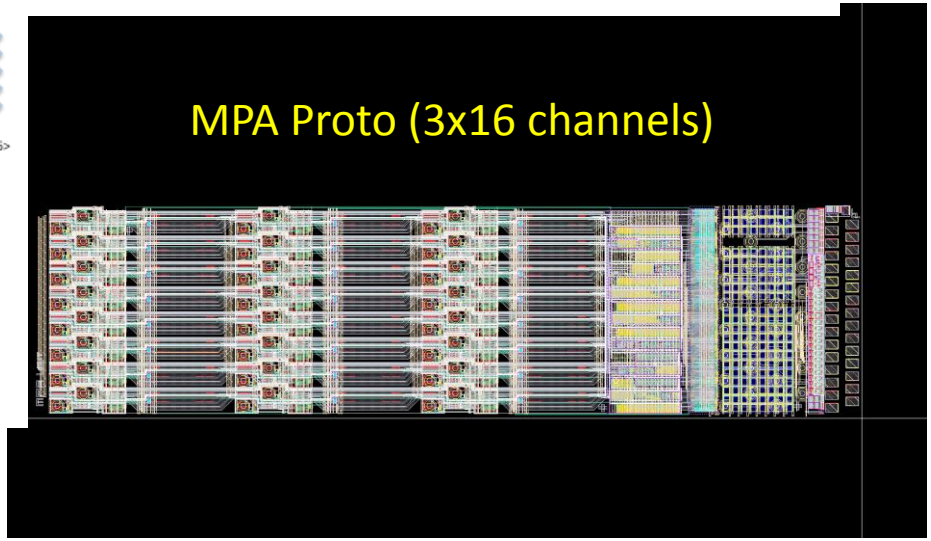
- 130 nm CMOS
- 256 channels
- 300 uW/ch on ~ 5 pF sensor
  - previous generation > 675 uW/ch (normalized on 5pF)
- noise ~ 850 e^-
- Built-in Logic to form trigger primitives

High complexity FE for trackers: the MPA

- Functionality
  - two layers sensor to find promptly "stiff" tracks through prompt combinations of hits in FE chips



- One macro pixel (1500x100 um) contains:
  - normal analog FE for amp/shaping/discriminating
  - clustering logic
  - re-alignment logic
  - pixel-strip trigger logic
  - storage for L1 2,000 logic gates + 512 bit SRAM/pixel
  - periphery with 3,000 gates common logic/pixel



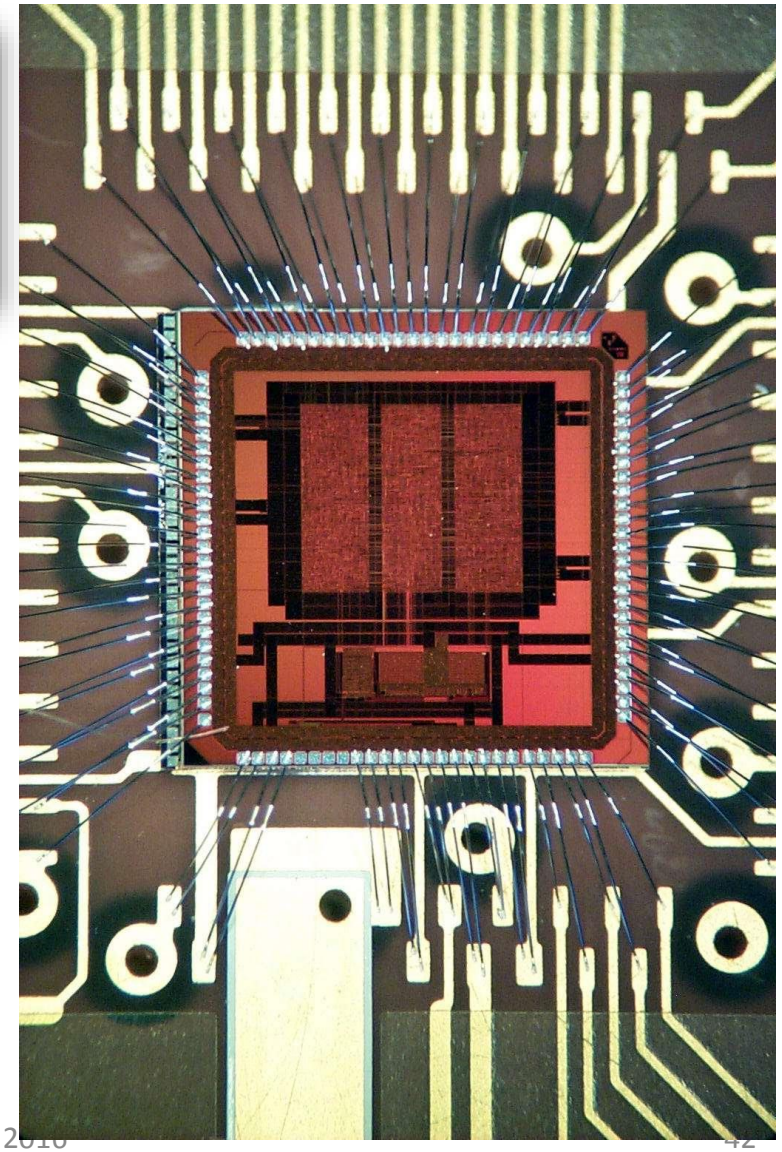
From talk by D. Ceresa @ TWEPP 2015

High Speed Links: The GOL {$}

A 1.25Gbit/s Serializer for LHC Data and Trigger Optical Links

P. Moreira[1], J. Christiansen, A. Marchioro,
E. van der Bij, K. Kloukinas, M. Campbell and G. Cervelli

CERN-EP/MIC, Geneva Switzerland



High density, low power CMOS allowed not only to implement a high speed serializer in a chip, but actually three to combat SEU effects

Serializer FOM: ~ 200 pJ/bit

{$} Paper presented at LEB 1999

2016 Links

SESSION 3 **Monday February 1st, 1:30 PM**

Ultra-High-Speed Transceivers

Session Chair: ***Hyeon-Min Bae,*** *KAIST, Daejeon, Korea*
Associate Chair: ***Ajith Amerasekera,*** *Texas Instruments, Dallas, TX*

1:30 PM

3.1 A 25Gb/s ADC-Based Serial Line Receiver in 32nm CMOS SOI
S. Rylov[1], T. Beukema[1], Z. Toprak-Deniz[1], T. Toiff[2], Y. Liu[3], A. Agrawal[1], P. Buchmann[2], A. Rylyakov[4], M. Beakes[1], B. Parker[1], M. Meghelli[1]
[1]IBM T. J. Watson Reseach Center, Yorktown Heights, NY
[2]IBM Zurich Research Laboratory, Rüschlikon, Switzerland
[3]now with Shanghai Jiao Tong University, Shanghai, China
[4]now with Coriant Advanced Technology Group, New York, NY

2:00 PM

3.2 A 320mW 32Gb/s 8b ADC-Based PAM-4 Analog Front-End with Programmable Gain Control and Analog Peaking in 28nm CMOS
D. Cui[1], H. Zhang[1], N. Huang[1,2], A. Nazemi[1], B. Catli[1], H. G. Rhew[1], B. Zhang[1], A. Momtaz[1], J. Cao[1]
[1]Broadcom, Irvine, CA; [2]now with Apple, Cupertino, CA

2:30 PM

3.3 DS1 A 25Gb/s Multistandard Serial Link Transceiver for 50dB-Loss Copper Cable in 28nm CMOS
T. Norimatsu[1], T. Kawamoto[1], K. Kogo[1], N. Kohmu[1], F. Yuki[1], N. Nakajima[2], T. Muto[2], J. Nasu[2], T. Komori[2], H. Koba[2], T. Usugi[2], T. Hokari[2], T. Kawamata[2], S. Umai[2], M. Tsuge[2], T. Yamashita[2], M. Hasegawa[2], K. Higeta[2]
[1]Hitachi, Tokyo, Japan; [2]Hitachi, Kanagawa, Japan

Break 3:00 PM

3:15 PM

3.4 A 40/50/100Gb/s PAM-4 Ethernet Tr… nm CMOS
K. Gopalakrishnan[1], A. Ren[1], A. Tan[1], A… Ravur[1], B. Helal[1], C-F. Loi[2], C. Jiang[1], H. Cirit[1], I. Quek[2], J. Rian… Wu[1], J. Pernillo[1], L. Tse[1], M. Le[3], M. Ranjbar[1], P-S. Wong… R. Narayanan[1], R. Mohanavelu[1], S. Herlekar[2], S. Bhoja[1], V. St…
[1]Inphi, Santa Clara, CA; … Singapore; [3]Inphi, Irvine, CA

…45 PM

3.5 DS1 A 56Gb/s NR… …7mW/lane Serial Link Transceiver in 28nm…
T. Shibas… T. Ogata[1], Y. Sakai[1], H. Miyaoka[2], F. Terasawa[2], M. Kudo[2], H. Kano[2], A… S. Kawai[2], T. Arai[2], H. Higashi[2], N. Naka[2], H. Yamaguchi[1], T. Mori[1], Y. Ko…nagi[1], H. Tamura[1]
[1]Fujitsu Laboratories, Kawasaki, Japan; [2]Socionext, Yokohama, Japan

4:15 PM

3.6 A 45Gb/s PAM-4 Transmitter Delivering 1.3V_{ppd} Output Swing with 1V Supply in 28nm CMOS FDSOI
M. Bassi[1], F. Radice[2], M. Bruccoleri[2], S. Erba[3], A. Mazzanti[1]
[1]University of Pavia, Pavia, Italy; [2]STMicroelectronics, Cornaredo, Italy
[3]STMicroelectronics, Pavia, Italy

4:45 PM

3.7 DS1 A 40-to-64Gb/s NRZ Transmitter with Supply-Regulated Front-End in 16nm FinFET
Y. Frans, S. McLeod, H. Hedayati, M. Elzeftawi, J. Namkoong, W. Lin, J. Im, P. Upadhyaya, K. Chang
Xilinx, San Jose, CA

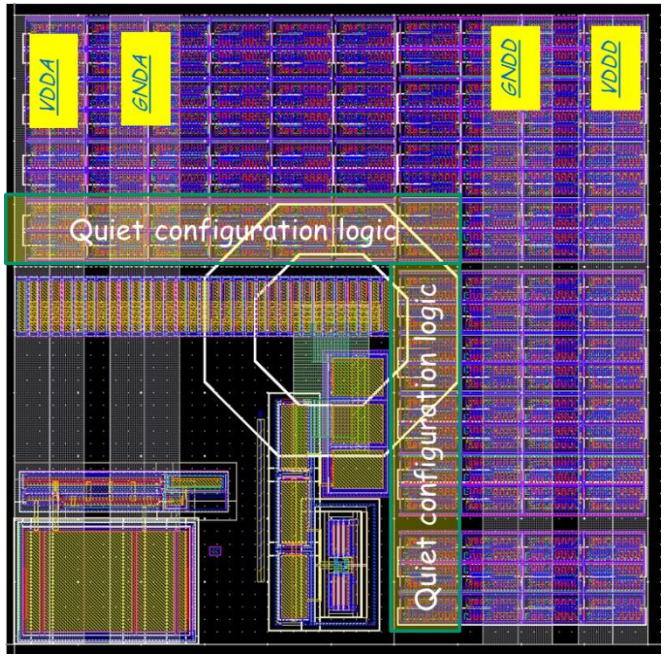
Conclusion 5:15 PM

Serializer FOM: ~ 2-5 pJ/bit

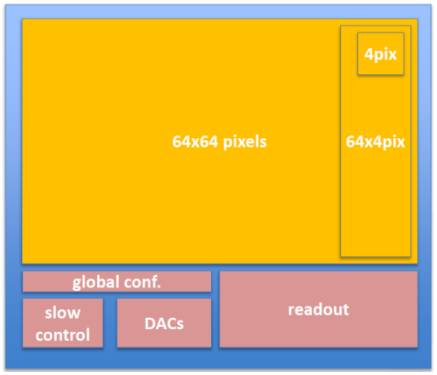
15

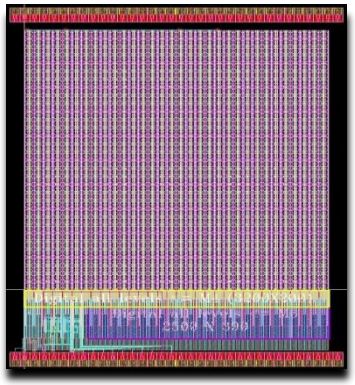
High density pixel design: RD53 pixel

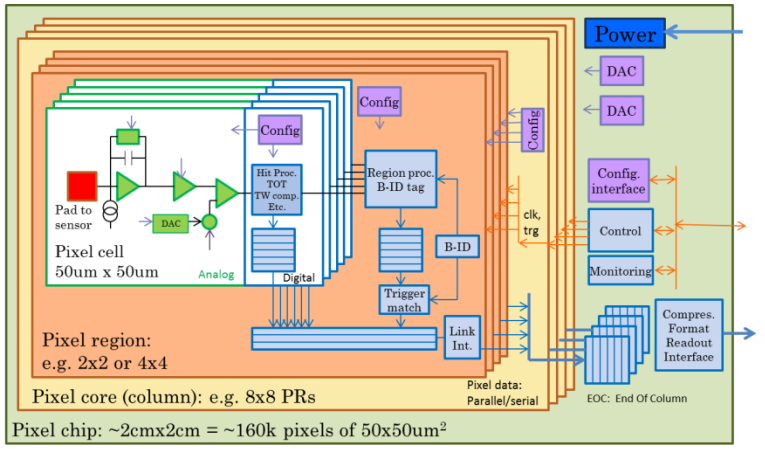
- Architecture and floor-plan for large pixel chip
  - Memory size:
    - 2x2 macro-pixel -> 8 hits buffer
    - 4x4 macro-pixel -> 16 hits buffer
  - Memory size is the critical issue for a 50x50 um pixel
  - Benefits from higher density technology in:
    - Power
    - Buffer sizes
    - Logic implementation, triplication



RD53A







from J. Christiansen, RD53 Collaboration

SRAM Density Comparison

Node	SRAM Cell Area [um2] {$}	KBits/mm2	Relative Density Gain
130nm	1.2	814	1.0
65nm	0.55	1776	2.2
28nm [bulk]	.1	~10K	12
14nm [Finfet]	0.05	~20K	25

{$} From various published sources

FE memory with FinFET

TSMC Finfet Based SRAM @ IEDM 2014

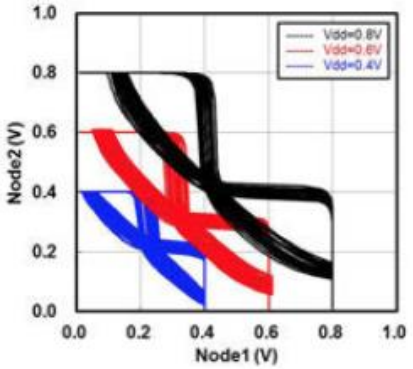


Fig.9 SNM of 0.07um^2 HD SRAM cell is illustrated down to 0.4V.

Cell size: 0.07 um2

Min Operating Voltage: 0.45V

Access time @1V is 0.6ns

from Shien-Yang Wu et al: An Enhanced 16nm CMOS Technology Featuring 2nd Generation FinFET Transistors and Advanced Cu/low-k Interconnect for Low Power and High Performance Applications, IEDM 2014

Application example:

If trigger latency @HL-LHC taken to 25 us, the tracker F-E would need a 1K memory per channel, i.e.

a 128Kbit buffer:

$128\ 10^3 * 0.07\ um^2 = 8.9\ 10^3\ um^2$

=> 94x94 um only !

(~ 100 x 100 um^2 is the area of a bonding pad!)

Operation @ 0.5V => ¼ of the power

Topics

- How is microelectronics benefitting/changing other “instrumentation” fields
- Scaling and trends
  - Scaling revisited
  - Advanced CMOS technologies
  - Technologies around the corner
    - Finfet
    - Steep sub-threshold devices
- Where to use transistors in instruments and detectors
- Conclusions

Conclusions

- Innovation in building new scientific instruments is not limited by the availability of electronic technologies!

- Advanced technologies are nevertheless complex and require strong engineering teams, i.e. more collaboration and coordination in our small community.
  - Only workable model:
    - Ride carefully well established commercial mainstream technologies
    - Stay with a single supplier: partnership is mandatory
    - Join forces: foster support of libraries of high level, well constructed, truly portable IPs
    - Be professional: demand strictly controlled and documented design flows

- Production cost is NOT dominated by the ICs themselves but by other elements, often our “boutique-like” assembly procedures
- Making more “disposable” detectors?
  - Already done in some detectors: can we extend the idea?

THANK YOU