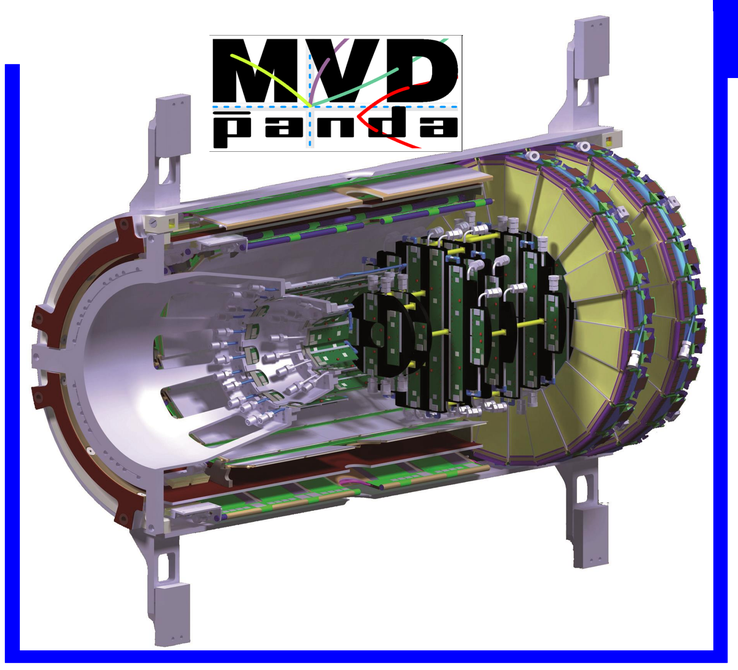
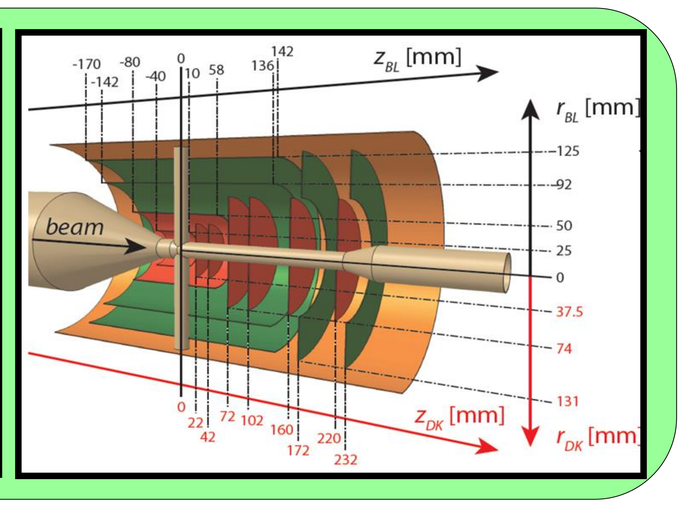
VCI 2016, February 15-19, 2016, Vienna

Overview of the Micro Vertex Detector for the PANDA experiment

D. Calvo (INFN-Torino) on behalf of the PANDA MVD group



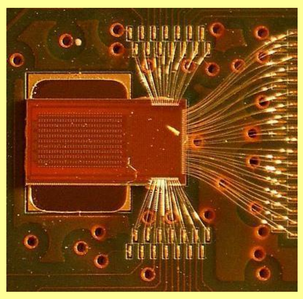
- Spatial resolution (tens of μm in ρϕ, <100 μm in z)
- Time resolution (< 10 ns)
- Continuous readout at ~ 10^7 interactions /s (clock signal @160 MHz)
- Limited material budget $X/X_o \leq 1$ % / layer
- Radiation tolerance < 10^{14} $n_{1\ MeV\ eq}$ cm^{-2}
- ≥ 4 hits per track
- Room temperature operation
- Routing and services backwards only

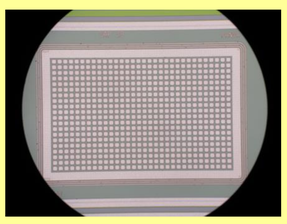


Two inner cylindrical layers around the interaction point, composed of **hybrid pixel detectors** and **two outer cylindrical layers** of **double sided silicon strip detectors.**
Six forward disks composed of **pixel detectors** and **two external rings** of **strip detectors. Total readout channels: 10.3 · 10^6 -pixel part and 2 · 10^5 –strip part**

Prototypes

- **ToPix_4:**
- ASIC size: 3 mm x 6 mm, clock frequency: 160 MHz
- 130 nm CMOS technology
- Pixel matrix: 640 cells, 2x2x128 and 2x2x32 columns
- Time over Threshold technique implemented, 12 bits dynamic range
- Compatible with the sensor of previous version (ToPix_v3)
- Hamming encoding and TMR pixel logic protection
- Leading and trailing edge registers with DICE -protected latches
- SEU protected EoC
- Serial data output (SDR and DDR)
- GBT compatible SLVS I/O

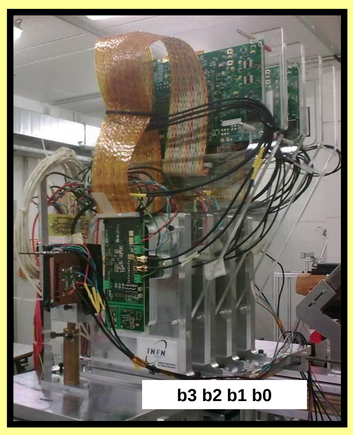


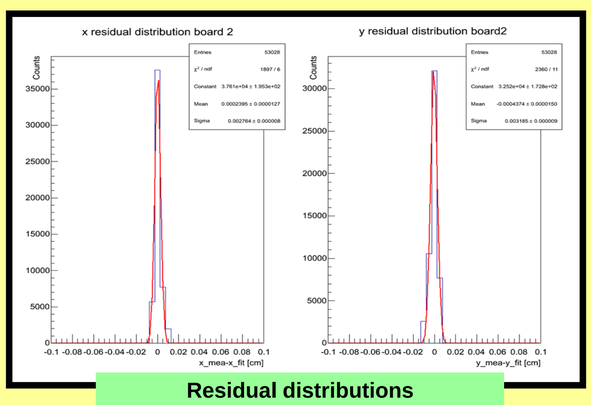


- Epitaxial silicon wafer by ITME (Varsaw)
  ρ_{epi} ~ 1500 Ω·cm
- Pixels @ FBK (Trento)
  100μm x 100μm
- Cz thinning + Bump bonding @ IZM (Berlin)
  Sn-Pb bumps
  Bump bonding yield of the tested assemblies: ~ 99.5 %

Thin Cz layer is the ohmic contact for the sensor biasingv

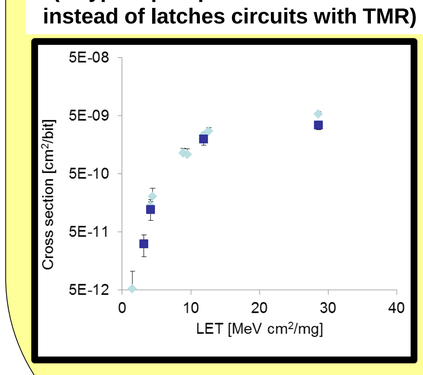
4 sigle-chip assemblies under test @ FZJ with 2.9 GeV/c proton beam

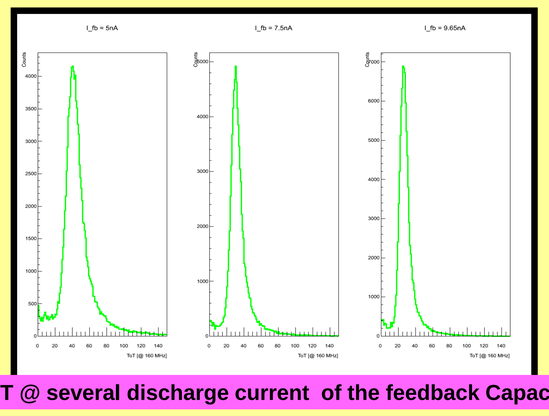




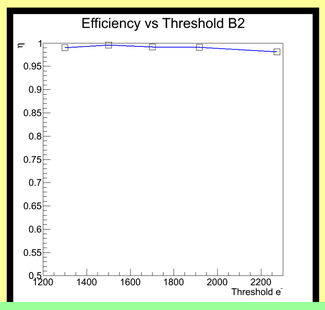
Residual distributions

SEU tests of ToPix_4 with ion beams @ LNL-INFN. Study of the configuration registers inside the pixels.
SEU cross section lower of an order of magnitude with respect ToPix_3 (D type flip-flops circuits with TMR instead of latches circuits with TMR)



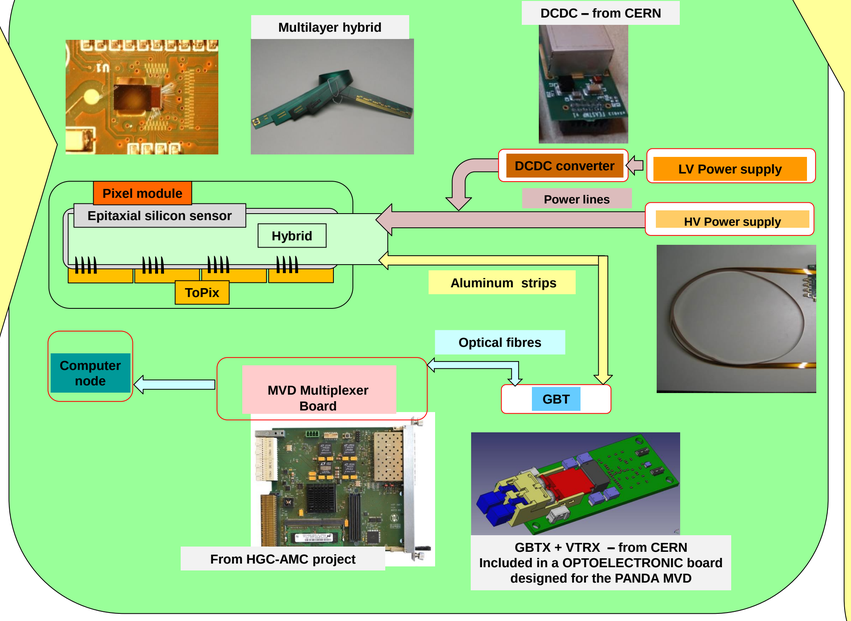


ToT @ several discharge current of the feedback Capacitor

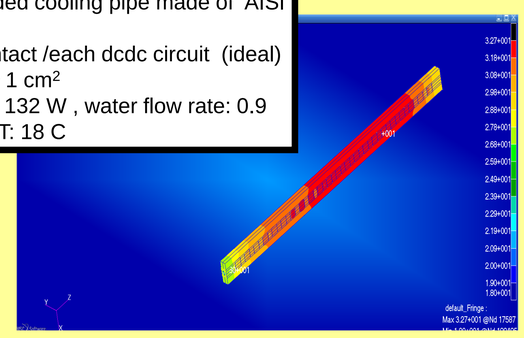


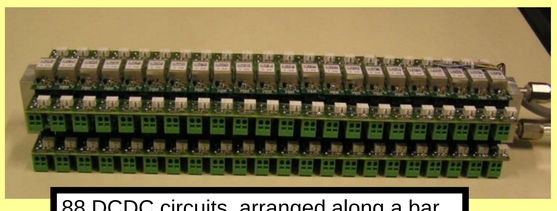
Efficiency vs threshold

Pixel readout chain

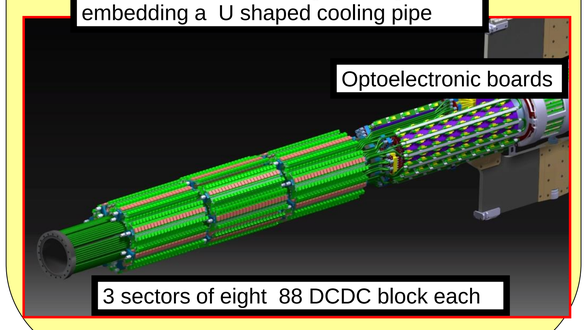


Thermal simulation of:
- One bar made of Al-Alloy (175 W /m·K) with embedded cooling pipe made of AISI 316
- Thermal contact /each dcdc circuit (ideal) obtained by 1 cm^2
- Total power: 132 W , water flow rate: 0.9 l/min, water T: 18 C

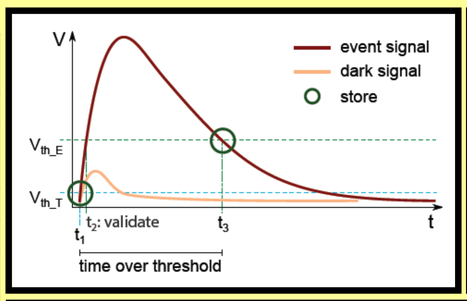


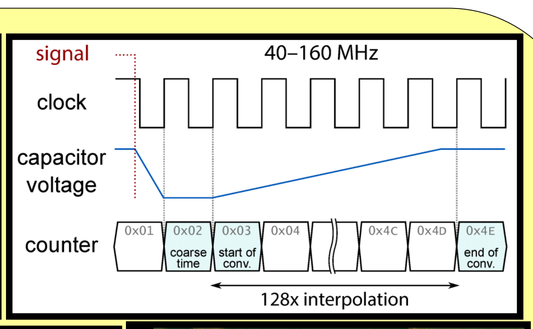


88 DCDC circuits arranged along a bar embedding a U shaped cooling pipe

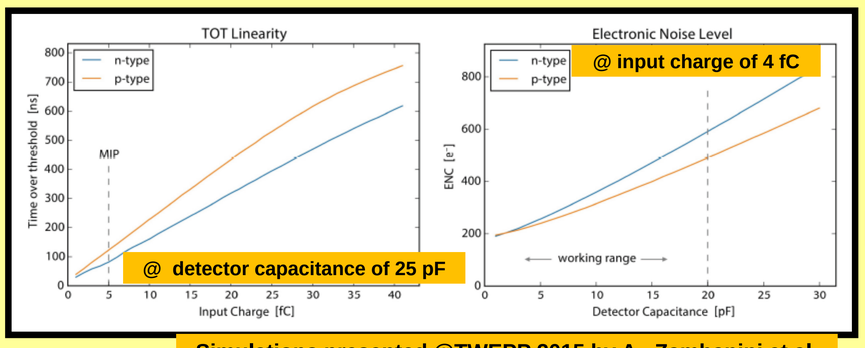


Key features	Value
Channels	64
Input pitch	63 μm
Clock frequency	160 MHz
Rate capability	100kHz/ch
Power consumption	< 4 mW/ch
Front-end noise	< 600 e-
Time bin width	50-400 ps
Charge resolution	8 bit (dyn. range)
Radiation tolerance	100 kGy

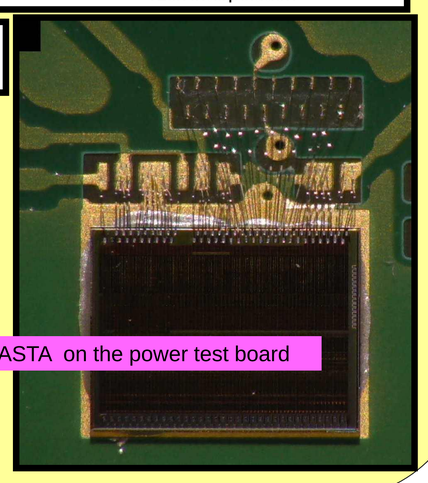




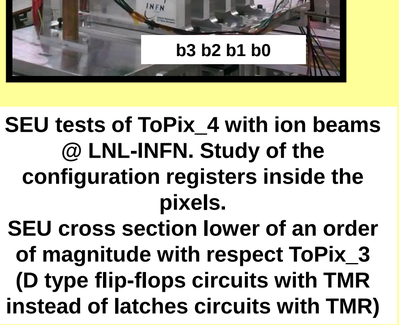
PASTA, triggerless ASIC for the strip readout
Developed in 110 nm CMOS technology (UMC)



Simulations presented @TWEPP 2015 by A. Zambanini et al.



PASTA on the power test board

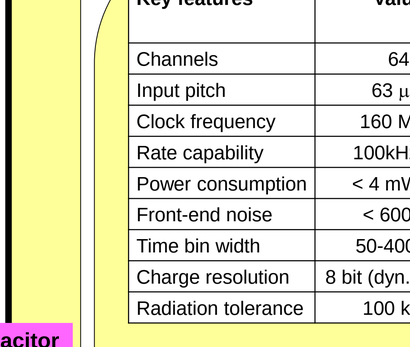


Strip sensor under test @ FZJ with 2.9 GeV/c proton beam

Double sided silicon strip detectors

- **Thickness**
  - 285 μm
- **Strip sensor shape**
  - rectangular for the barrel
  - trapezoidal for the disk
- **Readout: pitch/ stereo angle**
  - 130 μm / 90° for the barrel
  - 70 μm / 15 ° for the disk

Hit map for a strip square sensor



Signal to noise ratio vs bias voltage

Strip readout chain

Conclusion

MVD design is in progress with parallel software development to check physics performance
The prototyping phase is underway with challenge aspects