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Graphical processors for HEP trigger systems

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General-purpose computing on GPUs is emerging as a new paradigm in several fields of science, although so far applications have been tailored as accelerator in offline computation. With the steady reduction of GPU latencies, and the increase in link and memory throughputs, the use for real-time applications in high-energy physics data acquisition and trigger systems is becoming ripe. We will discuss the use of online parallel computing on GPU for synchronous low level trigger, focusing on tests performed on CERN NA62 experiment trigger system. All the components of the latency have to be analyzed. The networking results the most critical one. Our envisioned solution to this issue is NaNet, an FPGA-based PCIe Network Interface Card (NIC) to enable GPUDirect connection. The use of GPU in higher trigger system is also considered. In particular we discuss how specific trigger algorithms can be parallelized and thus benefit from the implementation on the GPU architecture, in terms of the increased execution speed. Such improvements are particularly relevant for the foreseen LHC luminosity upgrade where highly selective algorithms will be crucial to maintain a sustainable trigger rates with very high pileup. We will give details on how these devices can be integrated in a typical LHC trigger system. As a study case, we will consider the Atlas experimental environment and propose a GPU implementation for a typical muon selection in a high-level trigger system.

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