

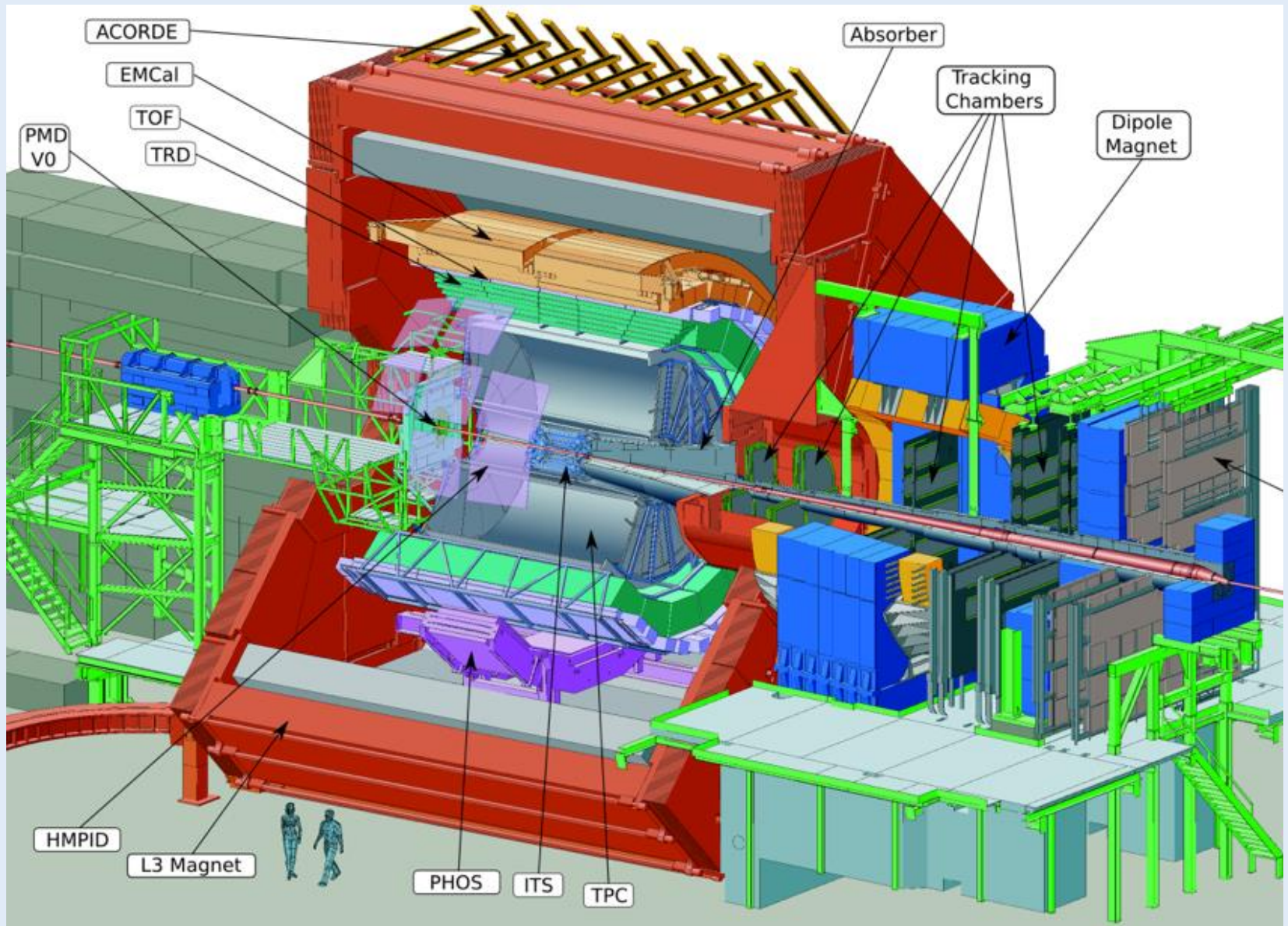
ALICE upgrade overview

A. Kluge, March 18, 2014

For the ALICE collaboration

- **Upgrade specifications**
- **Upgrade overview**
- **Upgrade architecture**
- **Slides taken from:**
H. Äppelshauser, J-P. Cachemiche, A. Kluge, G. Martinez,
P. Moreira, L. Musa, W. Riegler, W. Trzaska

ALICE & run 1/2



Upgrade strategy



- High precision measurements of rare probes at low p_t
- Cannot be selected with a trigger
- Require a large sample of events recorded
- Target
 - Pb-Pb $\rightarrow \geq 10 \text{ nb}^{-1} \rightarrow 8 \times 10^{10}$ events
 - pp (@5.5 TeV) $\rightarrow \geq 6 \text{ pb}^{-1} \rightarrow 1.4 \times 10^{11}$ events
- Gain factor 100 in statistics

Upgrade strategy

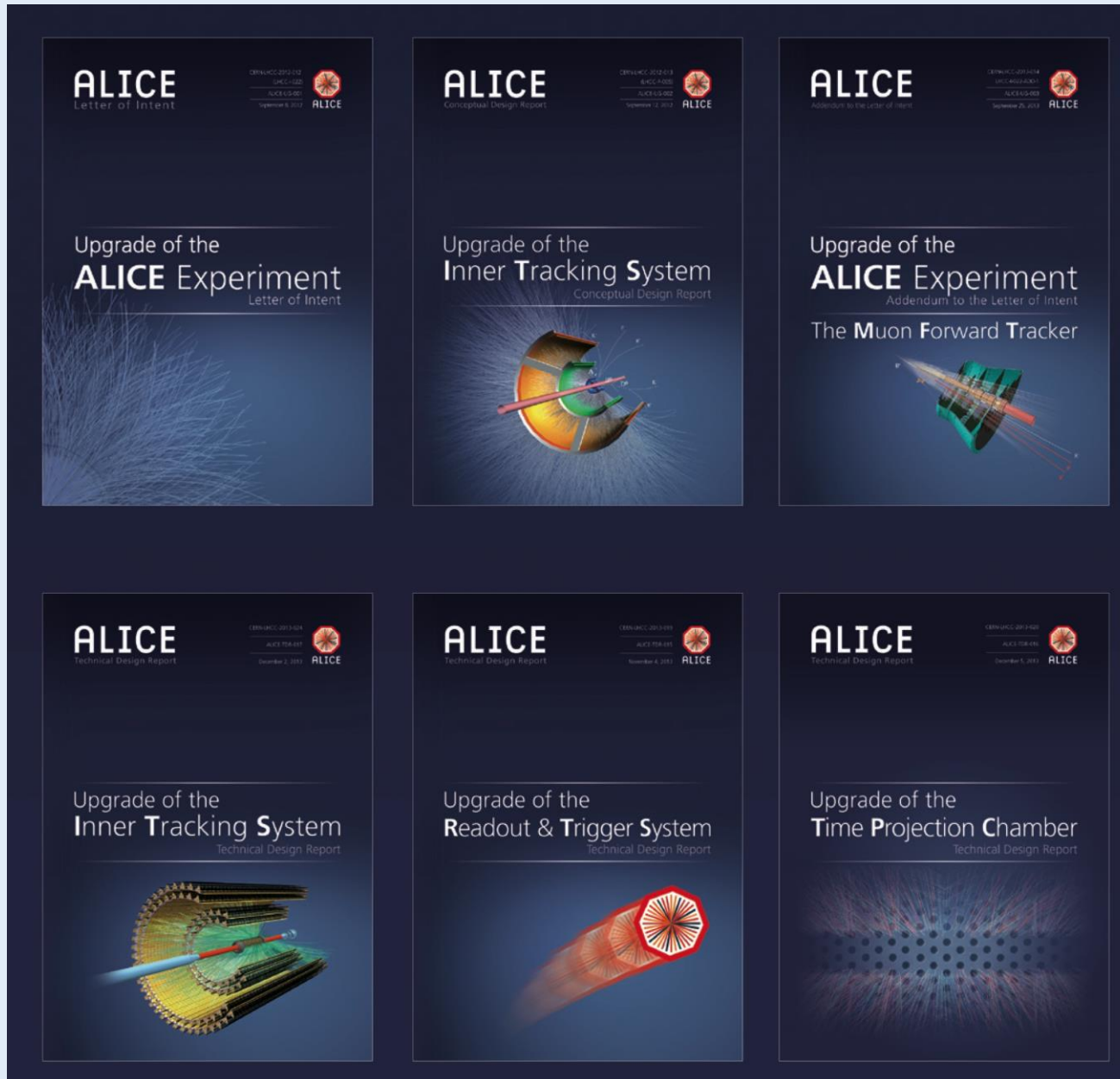


- **Upgrade ALICE read-out and online systems**

Upgrade in LS2 2018/19

- **Read-out all Pb-Pb interactions at**
 - 50 kHz ($L = 6 \times 10^{27} \text{ cm}^{-1}\text{s}^{-1}$) with min bias trigger
- **Online data reduction ← no filtering**
 - Reconstruction of clusters and tracks
- **Improve vertexing and tracking at low p_t**
 - **New inner tracking system**

LoI & TDR



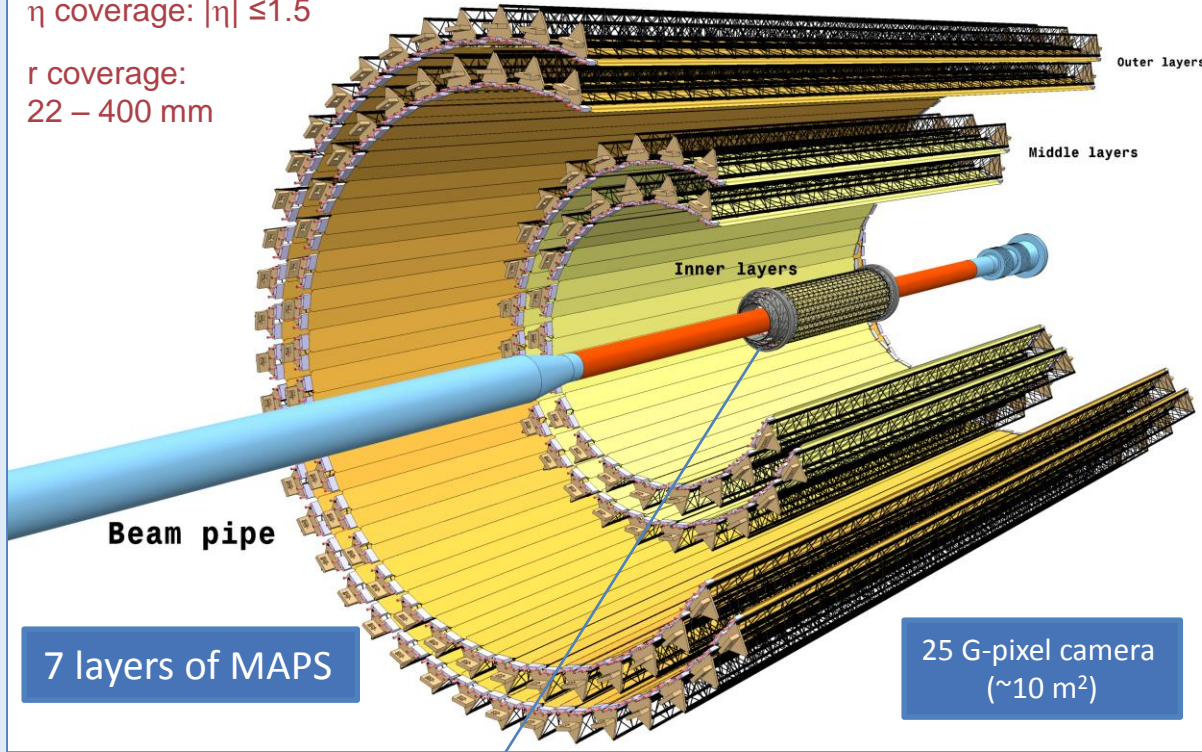
Inner tracking system



New ITS Layout

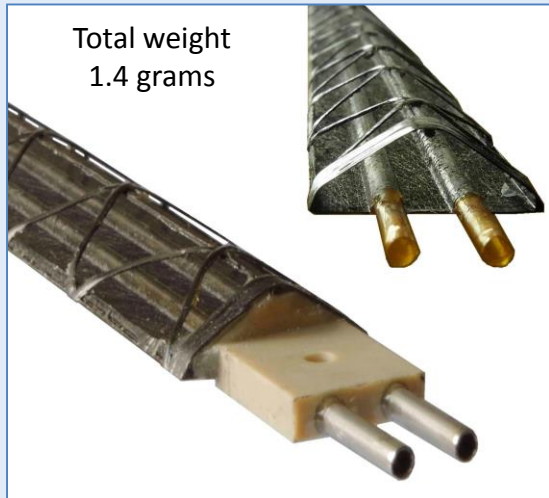
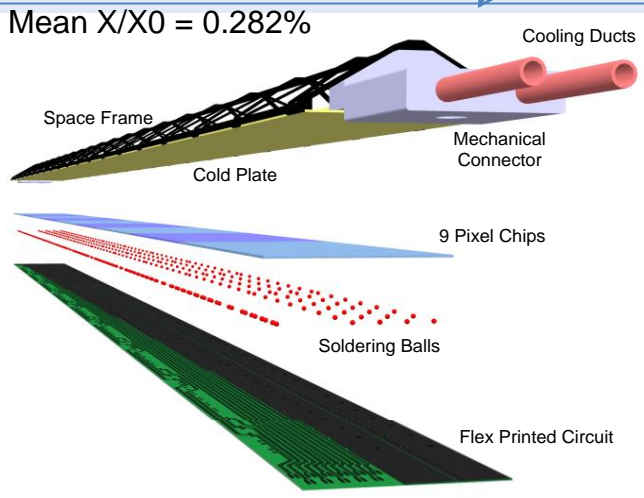
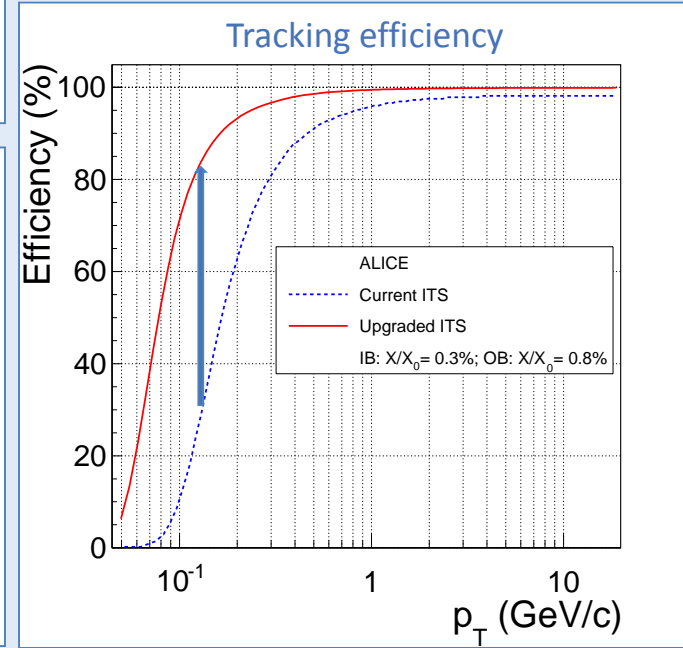
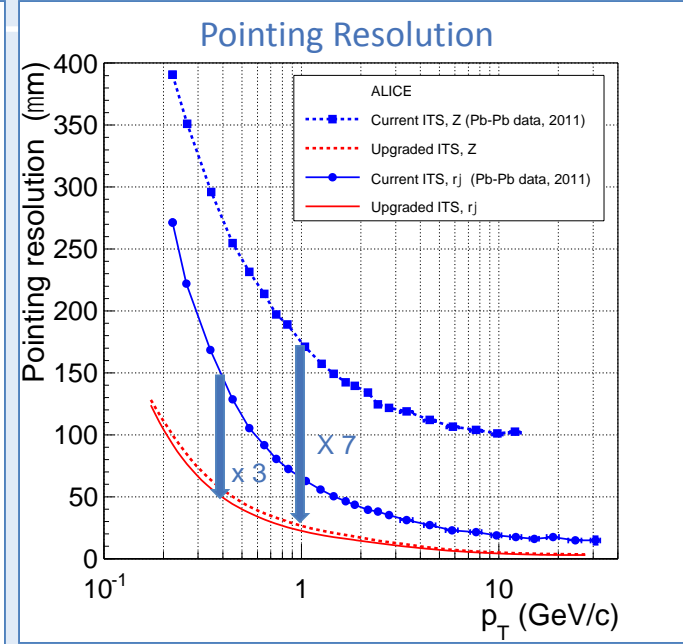
η coverage: $|\eta| \leq 1.5$

r coverage:
22 – 400 mm



7 layers of MAPS

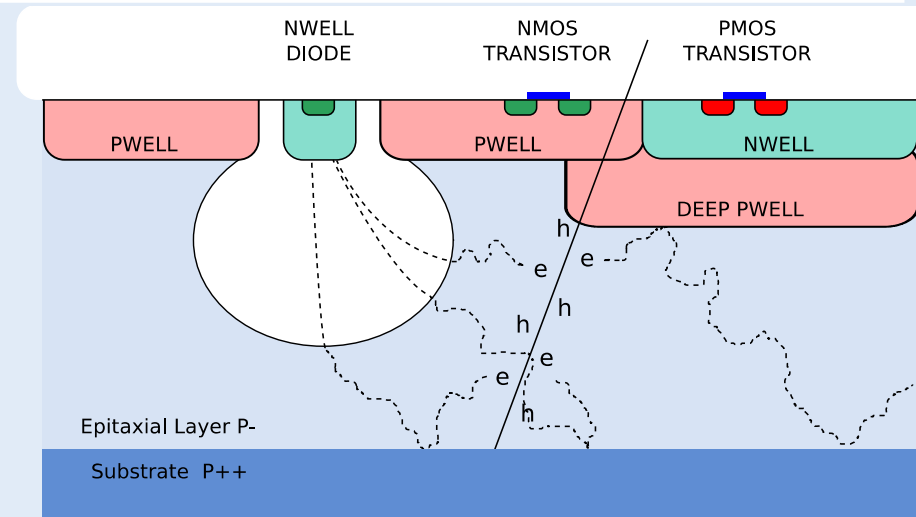
25 G-pixel camera
(~10 m²)



PIXEL Chip - technology

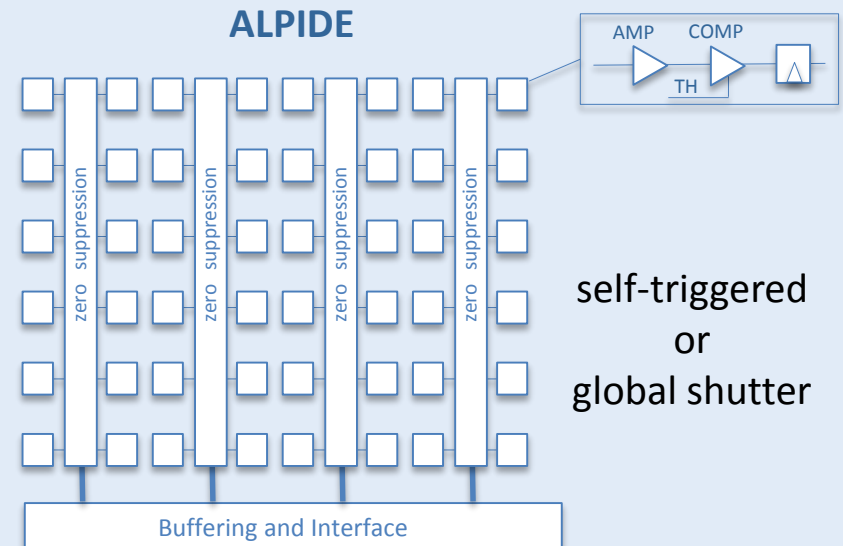
Monolithic PIXEL chip using Tower/Jazz 0.18 μm technology

- feature size 180 nm
- gate oxide < 4nm
- metal layers 6
- high resistivity epi-layer
 - thickness 18-40 μm
 - resistivity 1-6 k $\Omega \times \text{cm}$
- “special” deep p-well layer to shield PMOS transistors (allows in-pixel truly CMOS circuitry)
- Several prototype architectures
 - ALPIDE self-triggered or global shutter
 - MISTRAL/ASTRAL rolling shutter



Schematic cross-section of CMOS pixel sensor
(ALICE ITS Upgrade TDR)

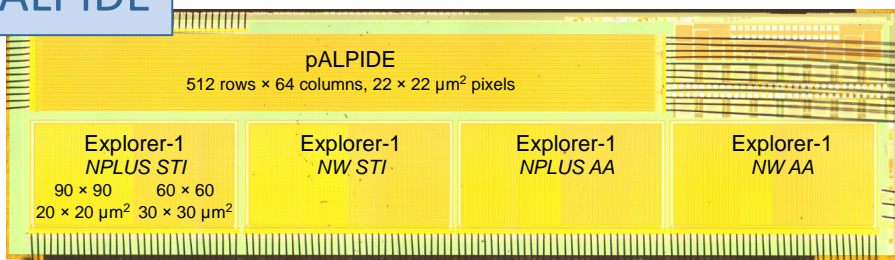
Power density < 50 mW/cm²



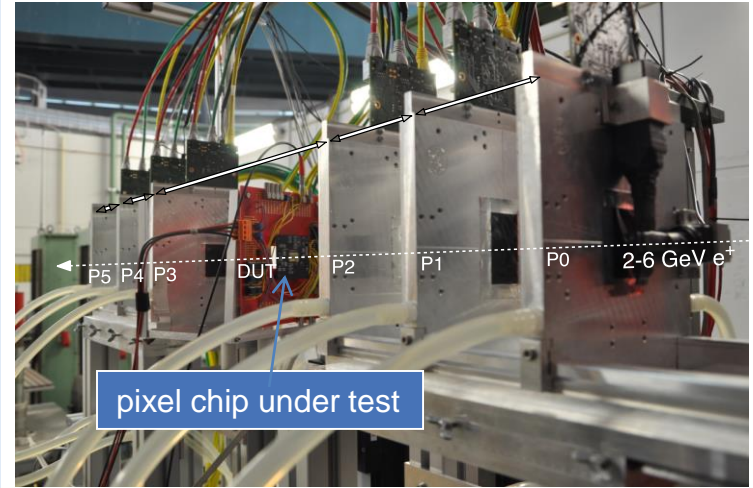
New ITS – pixel prototype chips & experimental results



ALPIDE

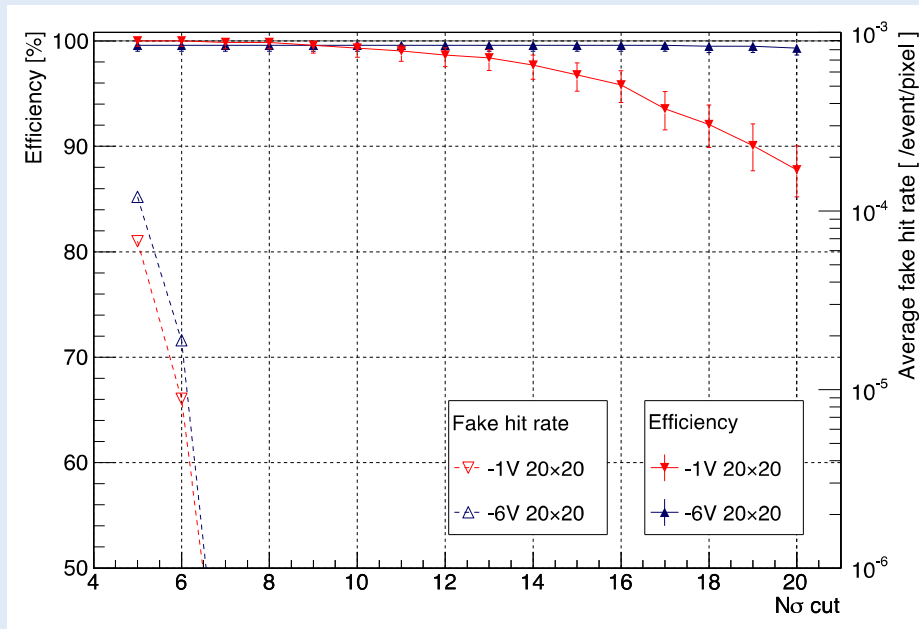


pALPIDE: sizeable prototype of final chip (digital output)
Explorer: prototype chip with analogue output



Measurements at DESY test beam (4.4 GeV electron beam) – Sep 2013

Explorer chip, performance of pixel chip
from analogue output, pixel size: 20 x 20 μm²



pALPIDE chip, performance of pixel chip
from digital output, pixel size: 22 x 22 μm²

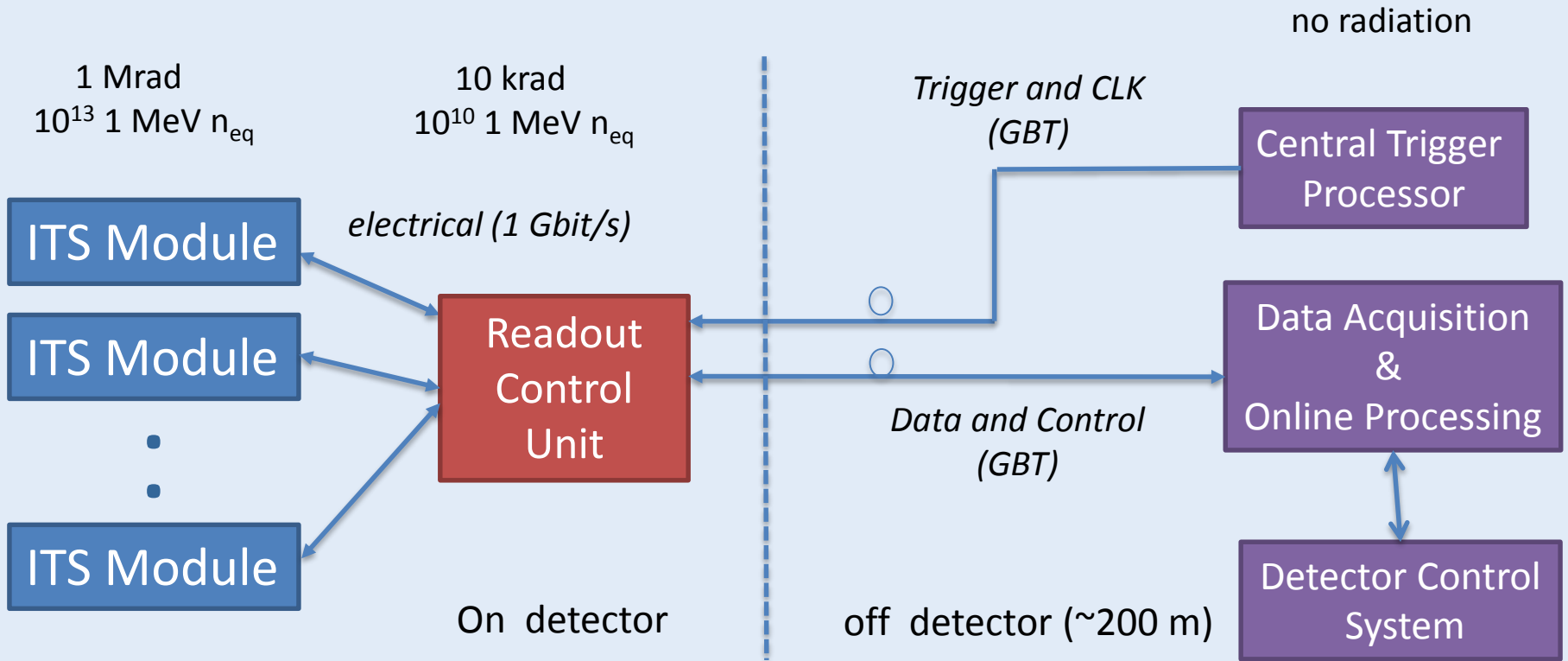
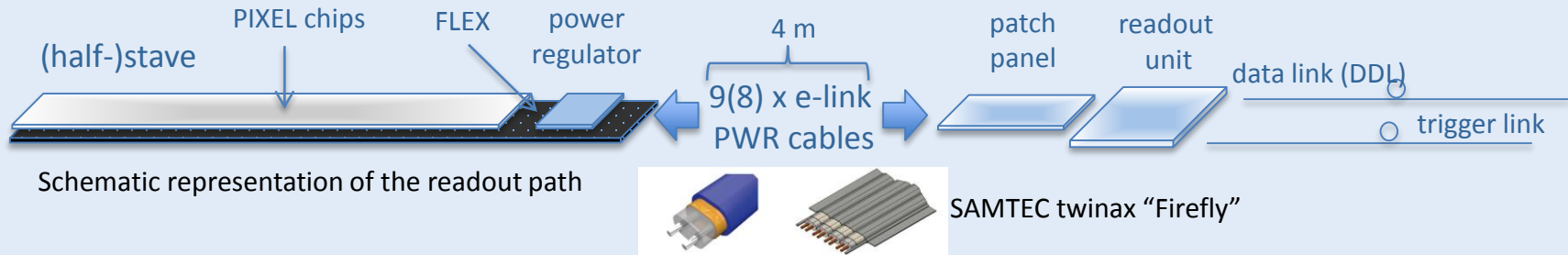
Threshold / Noise: 20

Detection efficiency: 99.7%

Fake hit rate < 10⁻⁸

Spatial resolution ~ 5 μm

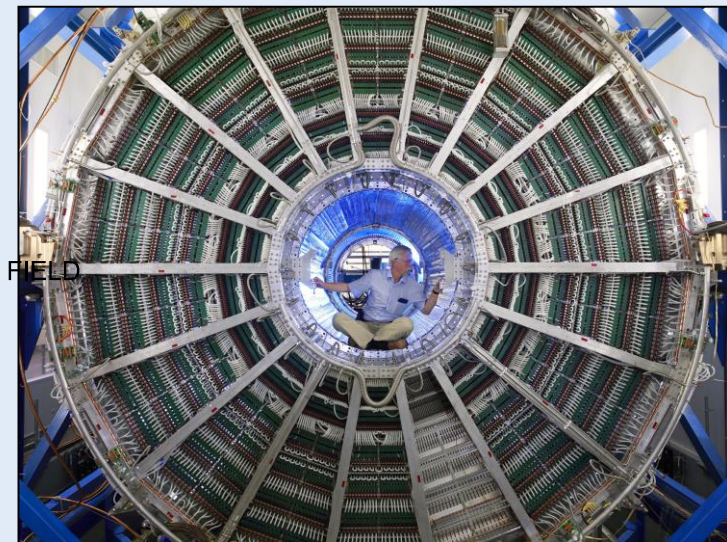
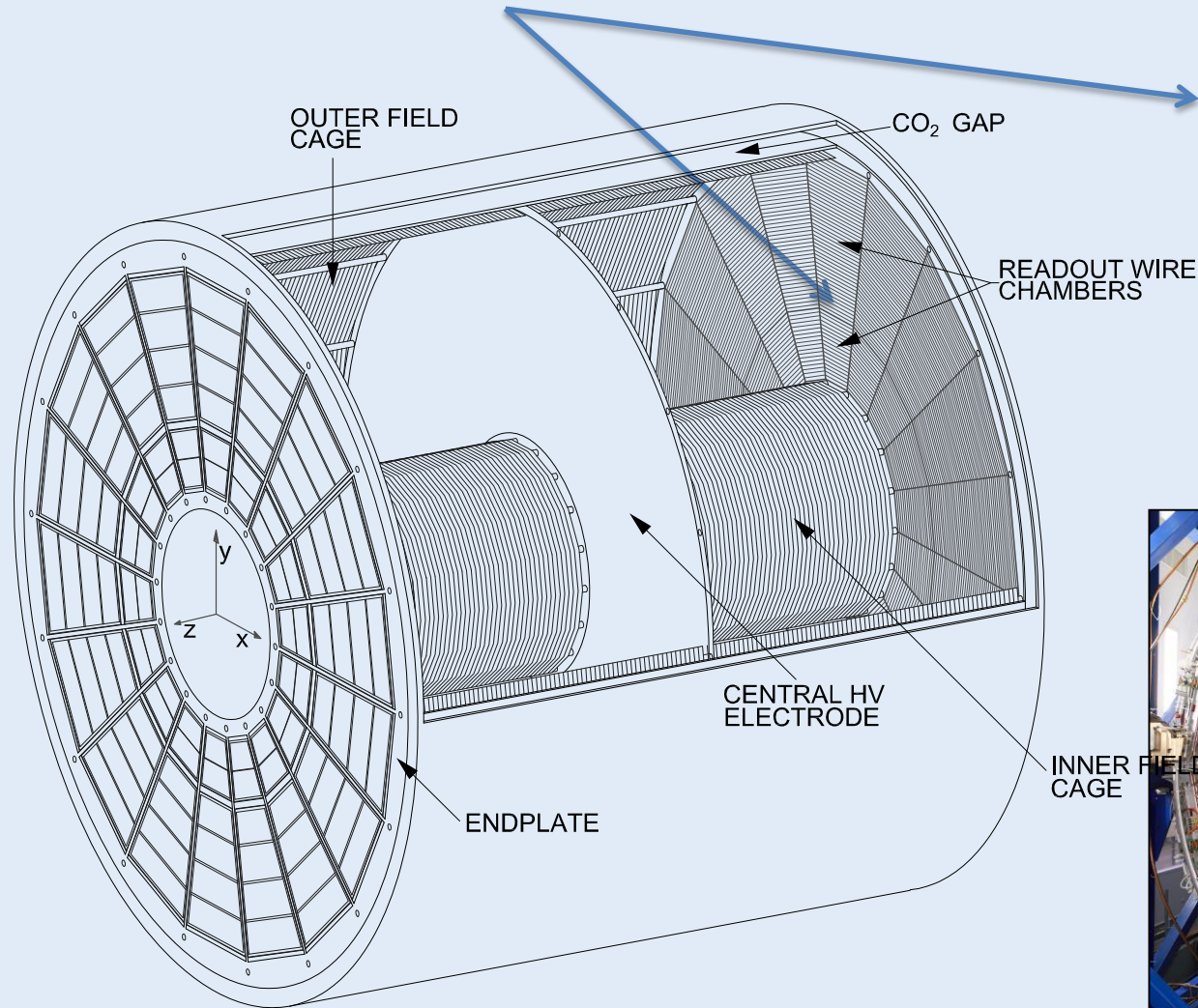
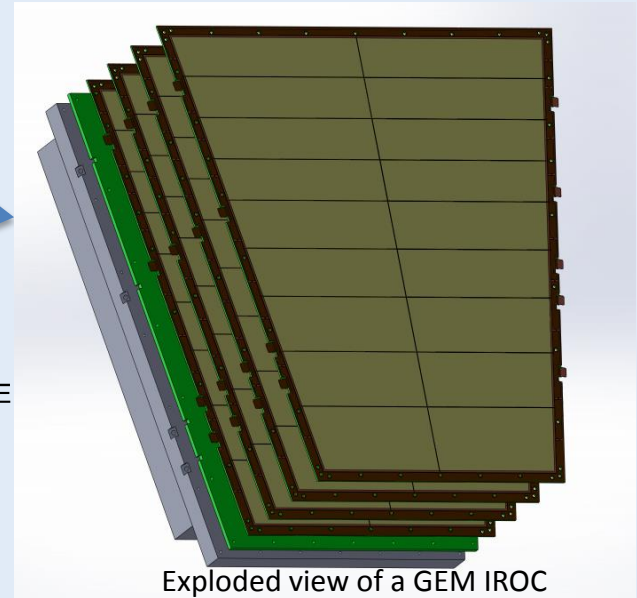
Readout – general scheme and data throughput



TPC

TPC upgrade

Replace wire chambers
With quadruple-GEM chambers

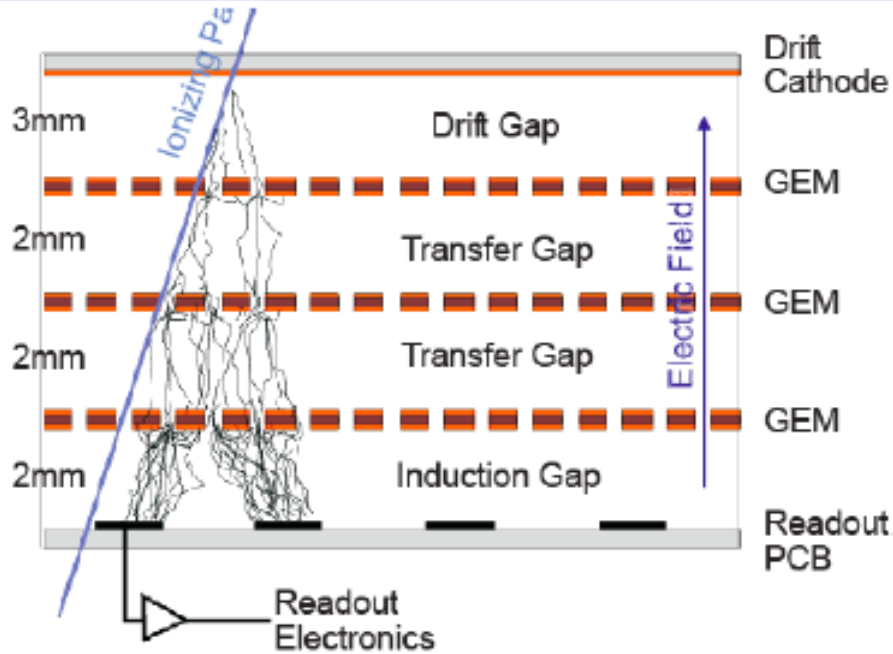


TPC-present limitation & upgrade

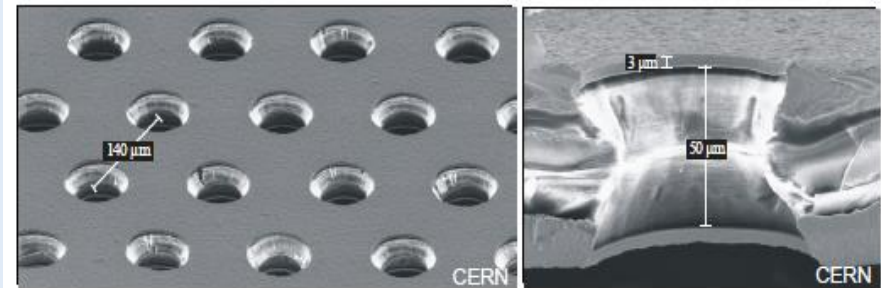


- drift time (electrons) = 100 μs
- after gating grid closed until 280 μs
 - to prevent back drifting ions into drift region
 - and space charge distortion
- **→ total time 280 μs → 3.5 kHz read-out rate**
- avg. interaction rate 50 kHz → 20 μs
- drift time = 100 μs →
- **pile-up → continuous trigger-less read-out**

multiple GEM principle

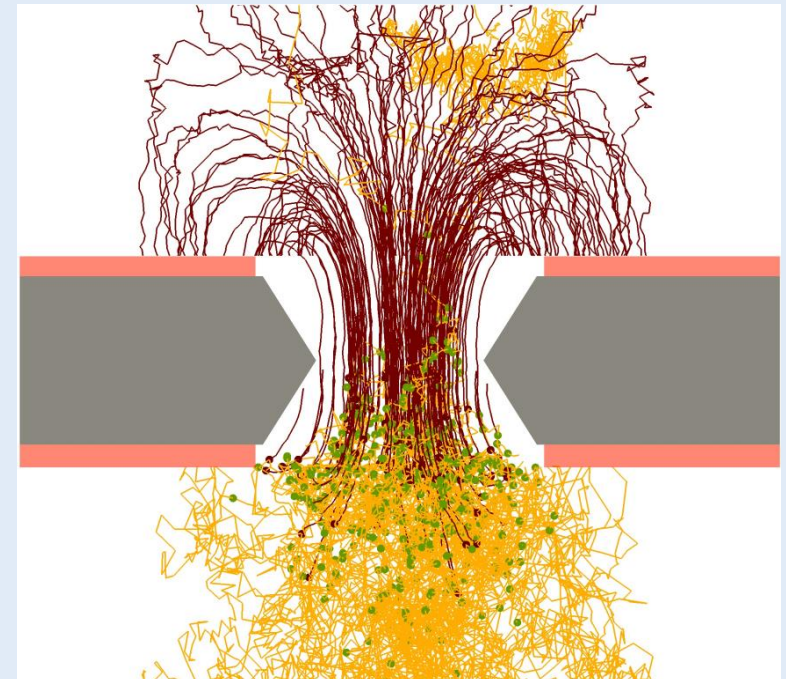


GEMs are made of a copper-kapton-copper sandwich, with holes etched into it

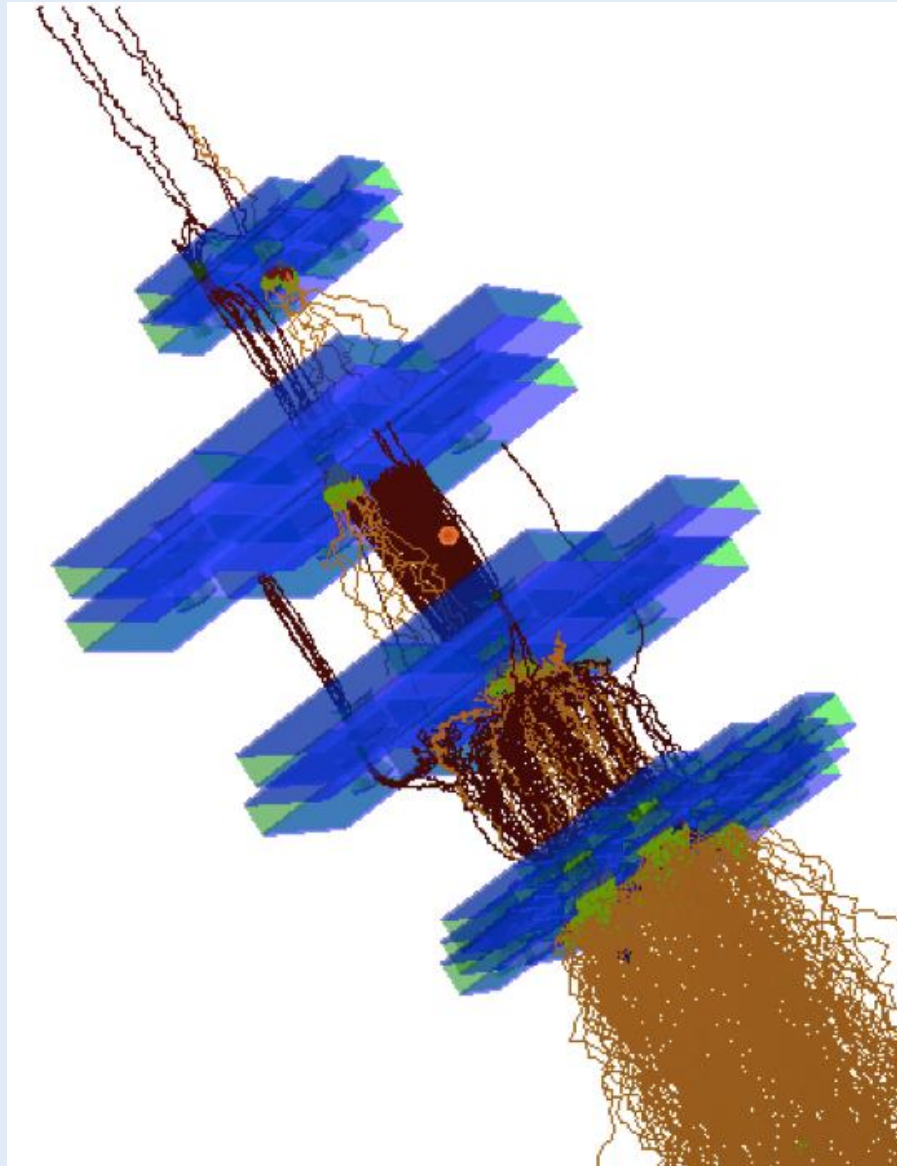


Electron microscope photograph of a GEM foil

- Fast **electron** signal (polarity!)
- no “ion tail”
- No “coupling to other electrodes”
- ➔ Gas gain about a factor 3 lower than in MWPC

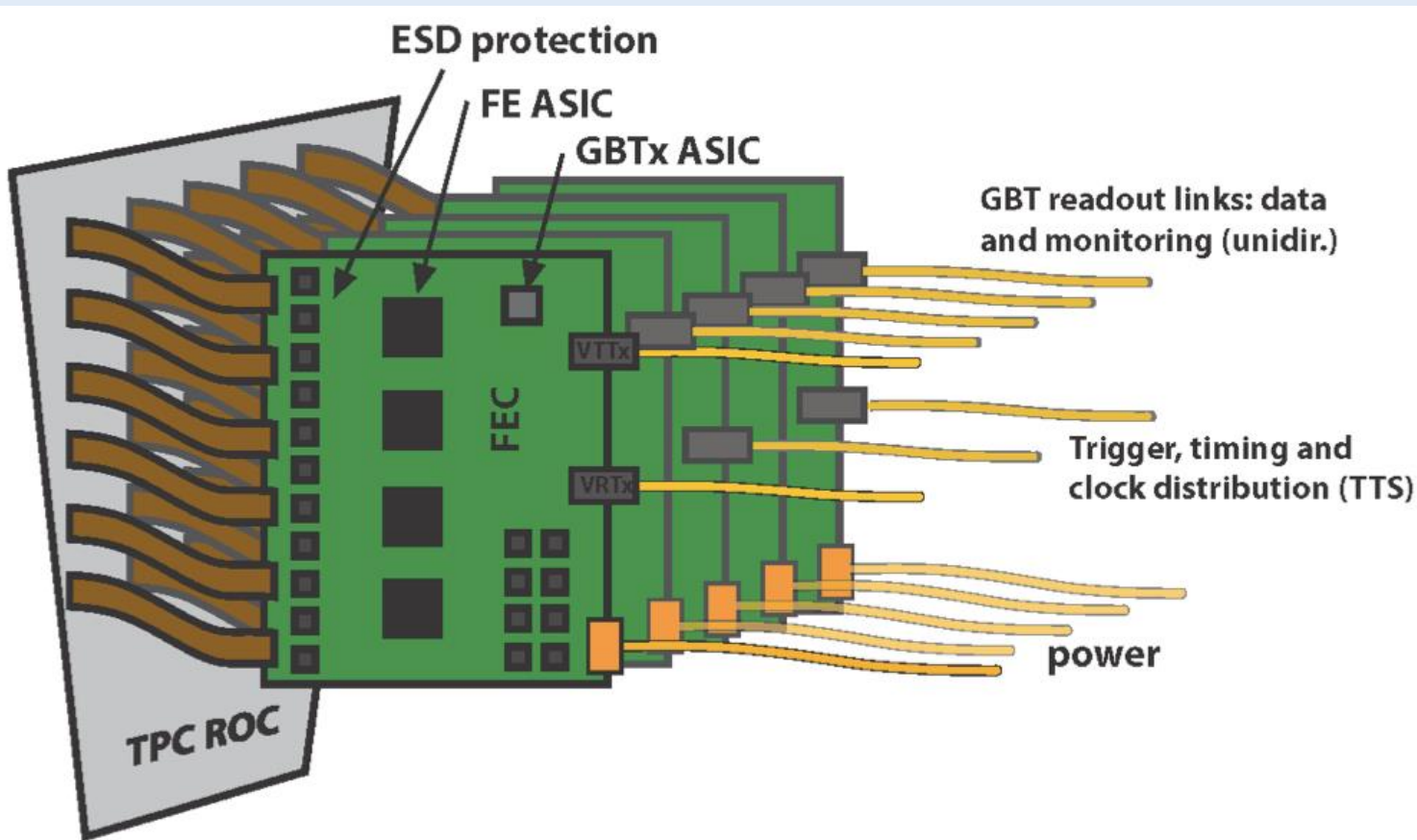


4 GEM simulation



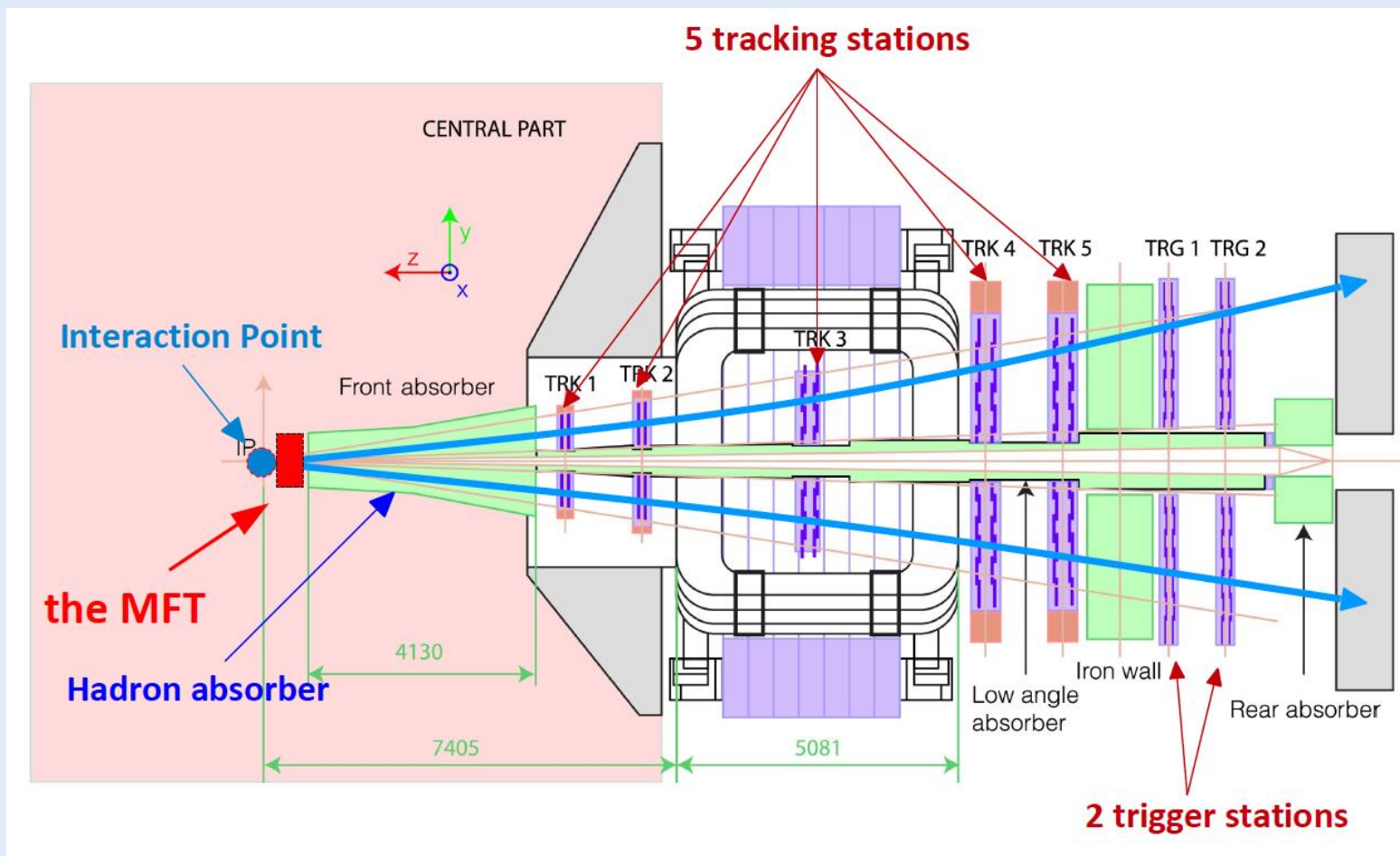
TPC front-end card

- ~ 500.000 channels @ 50 kHz read-out rate
- 3400 front-end cards & ~ 17.000 SAMPA ASICs



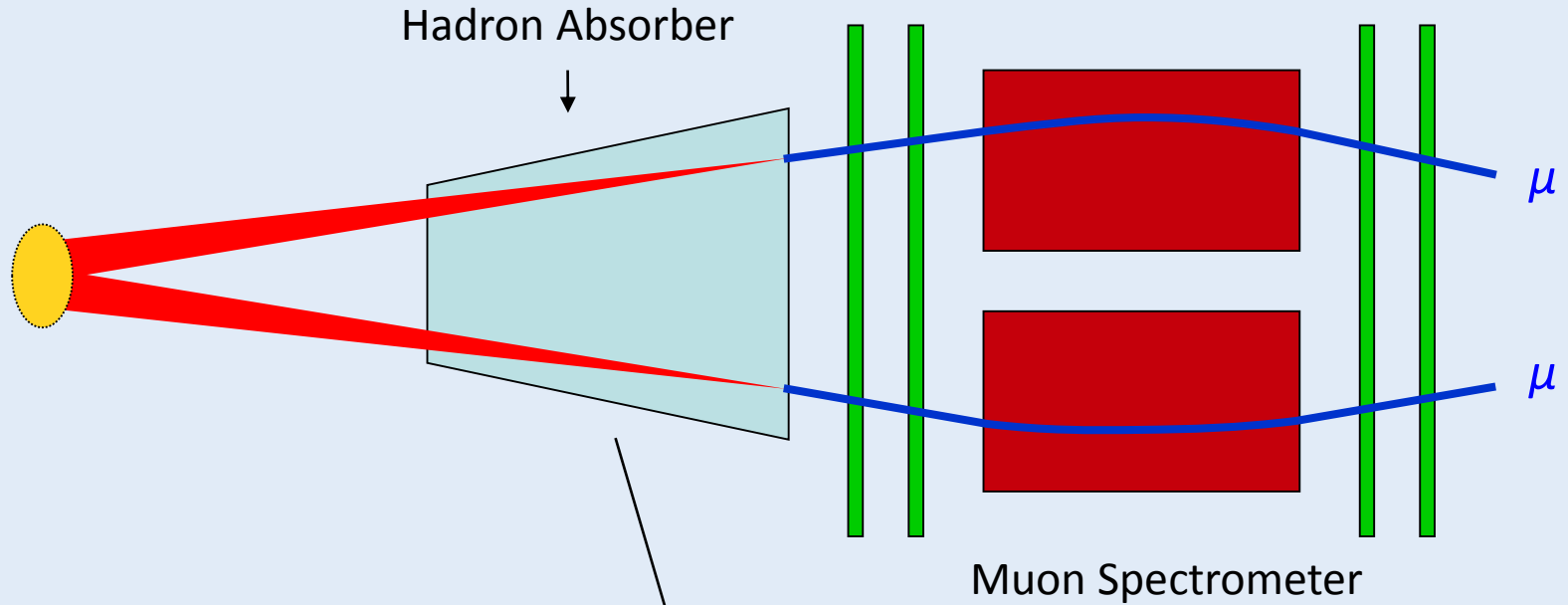
Muon Forward Tracker - MFT

MFT and Muon-Spectrometer



**Silicon pixel tracker in acceptance of Muon Spectrometer
between Interaction Point and Hadron Absorber**

MFT concept

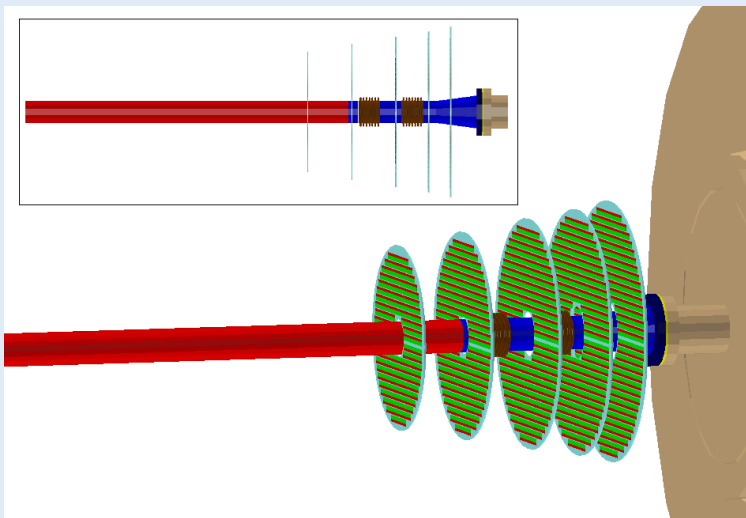
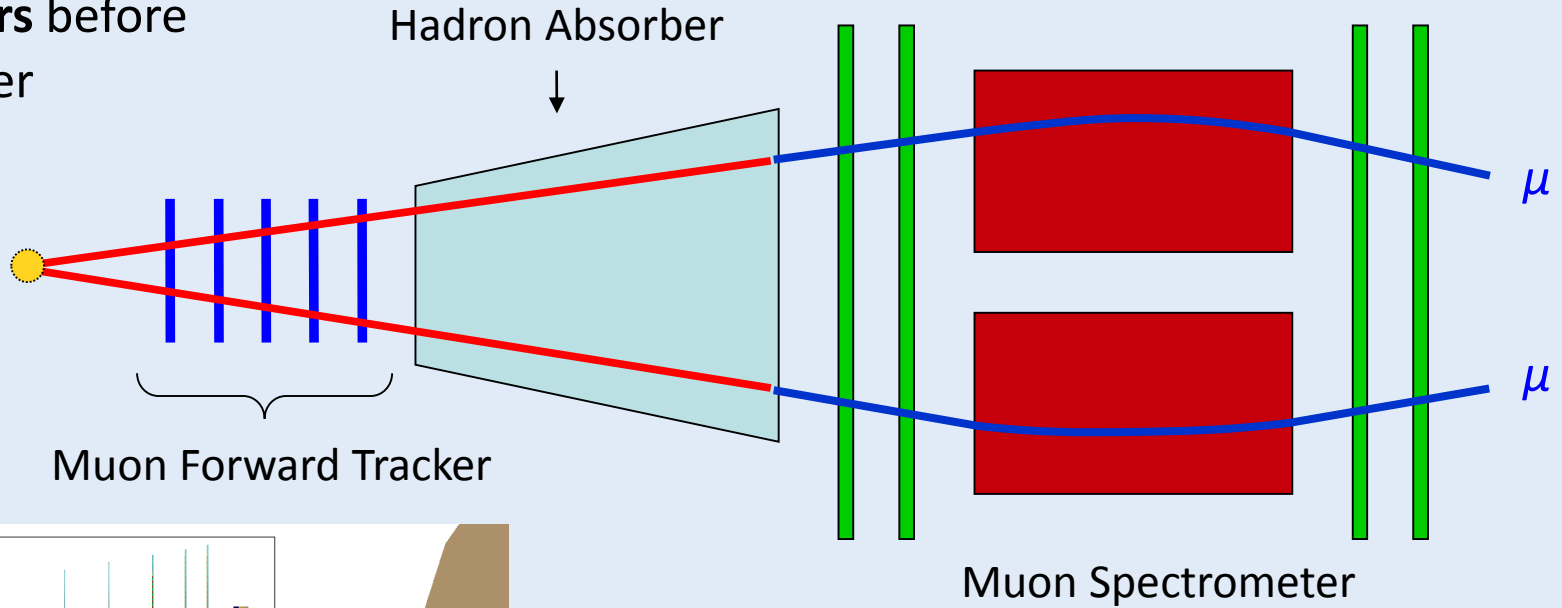


Extrapolating back to the vertex region
degrades the information on the kinematics

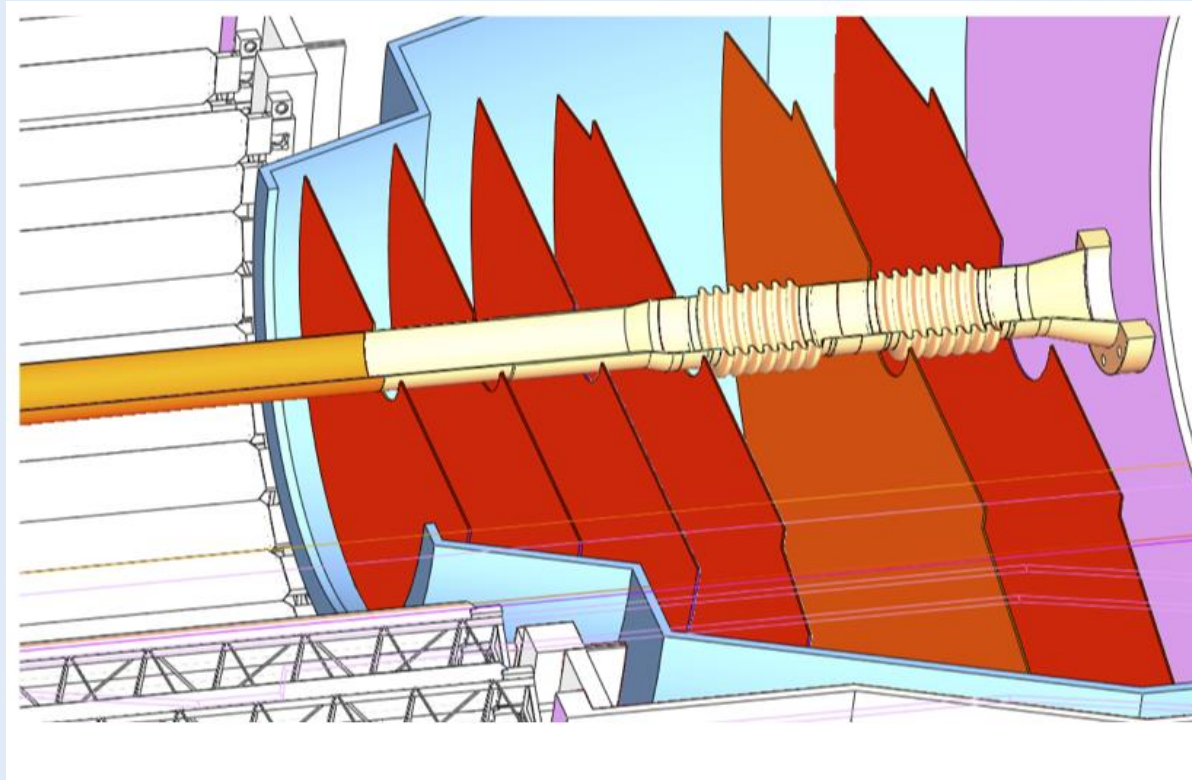
MFT concept

Muon tracks are extrapolated and “**matched**” to the **MFT clusters** before the absorber

High pointing accuracy gained by the muon tracks after matching with the MFT clusters



MFT layout

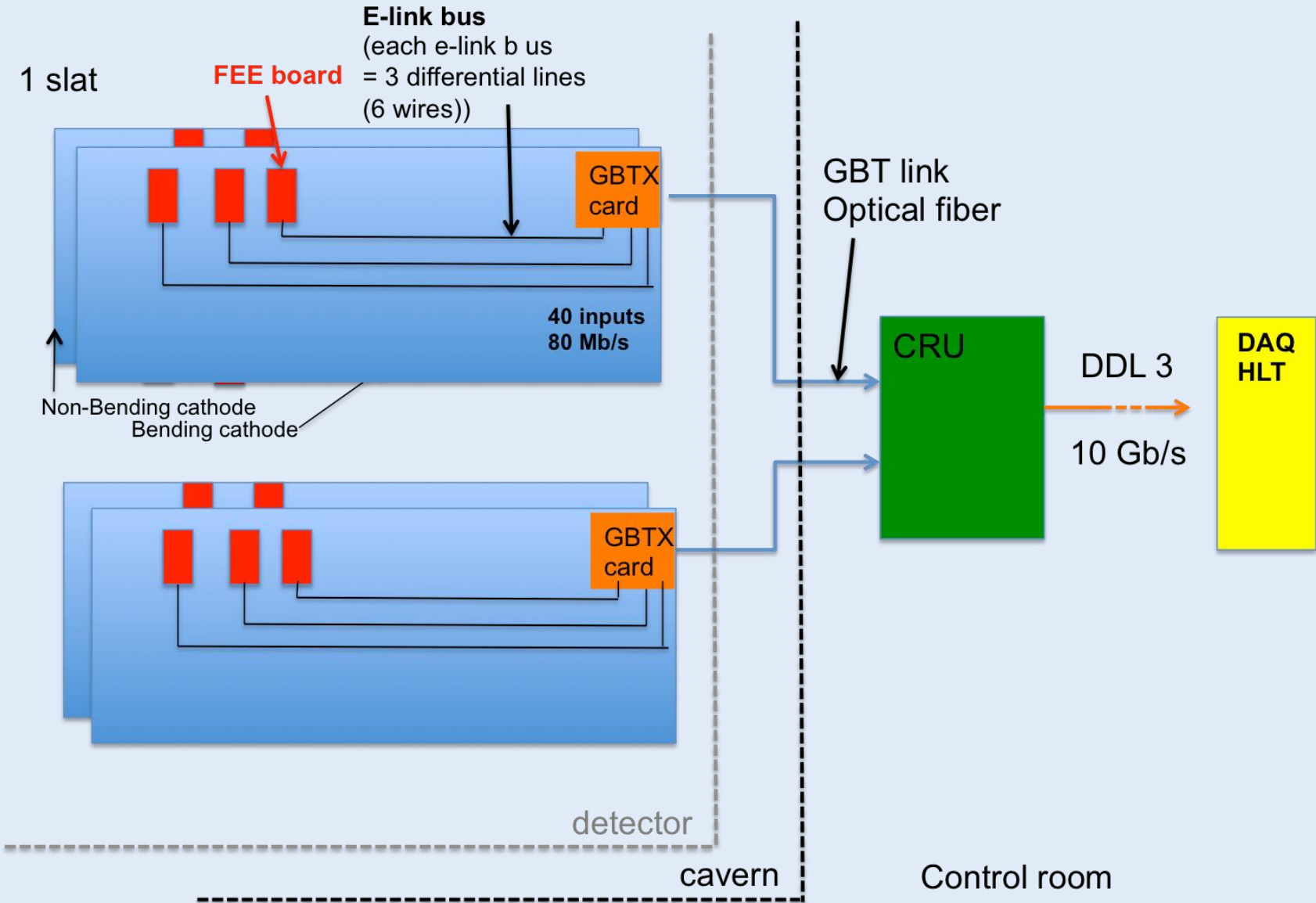


- **Based on MAPS: common development with ITS**
- **Read-out based on GBT links**

Muon chambers - MCH

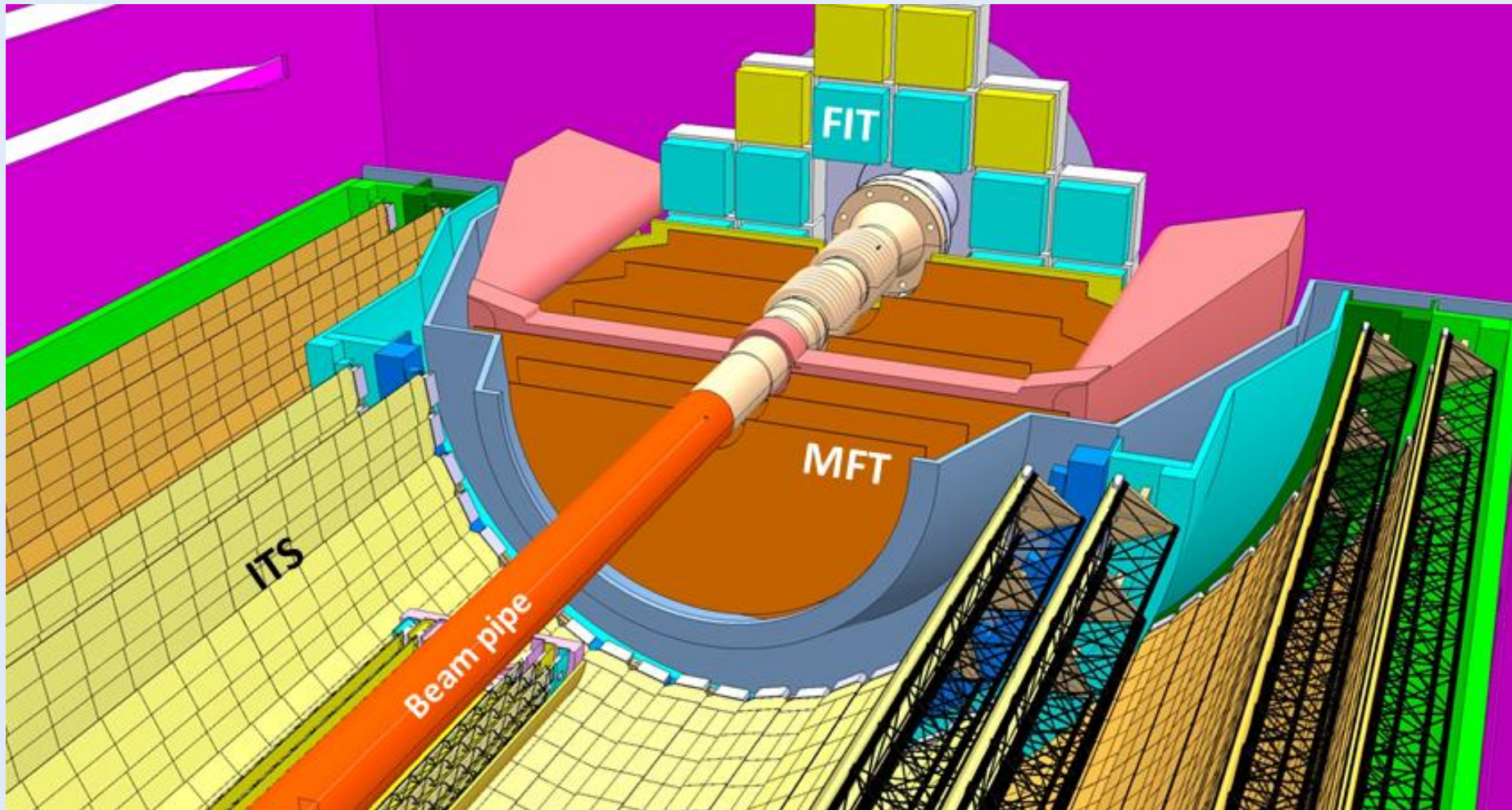
- **~1.000.000 MWPC**
- **upgrade to continuous read-out @ 100 kHz hit rate**
- **Replacement of the front-end by ~ 33.000 SAMPA ASIC**
- **Replacement of active patch panels (first level of data concentration)**
 - **based on GBTs or electrical e-links**
- **Replacement of data concentrator by CRUs**

muon chamber



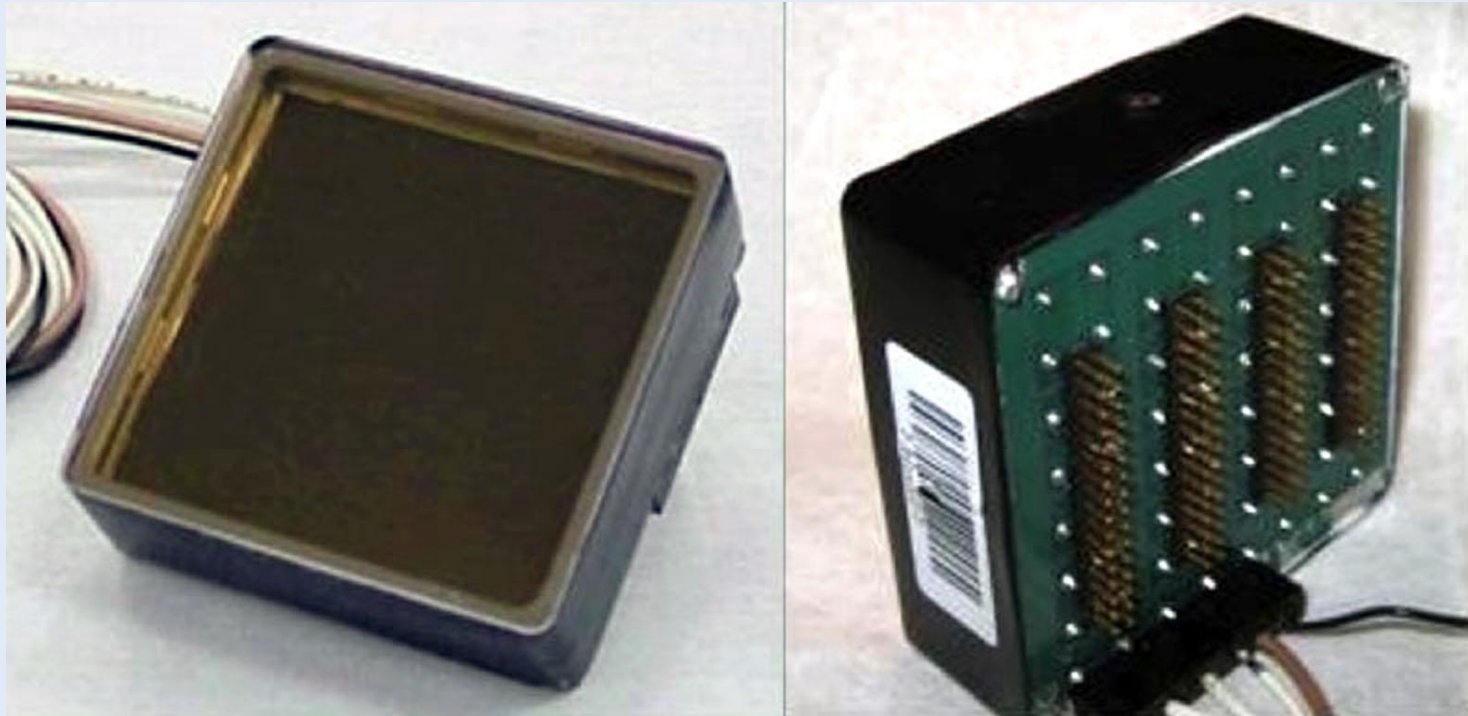
Fast interaction trigger

Fast interaction trigger - FIT



Fast interaction trigger - FIT

Photonis PLANACON[®] XP85012 or XP85112



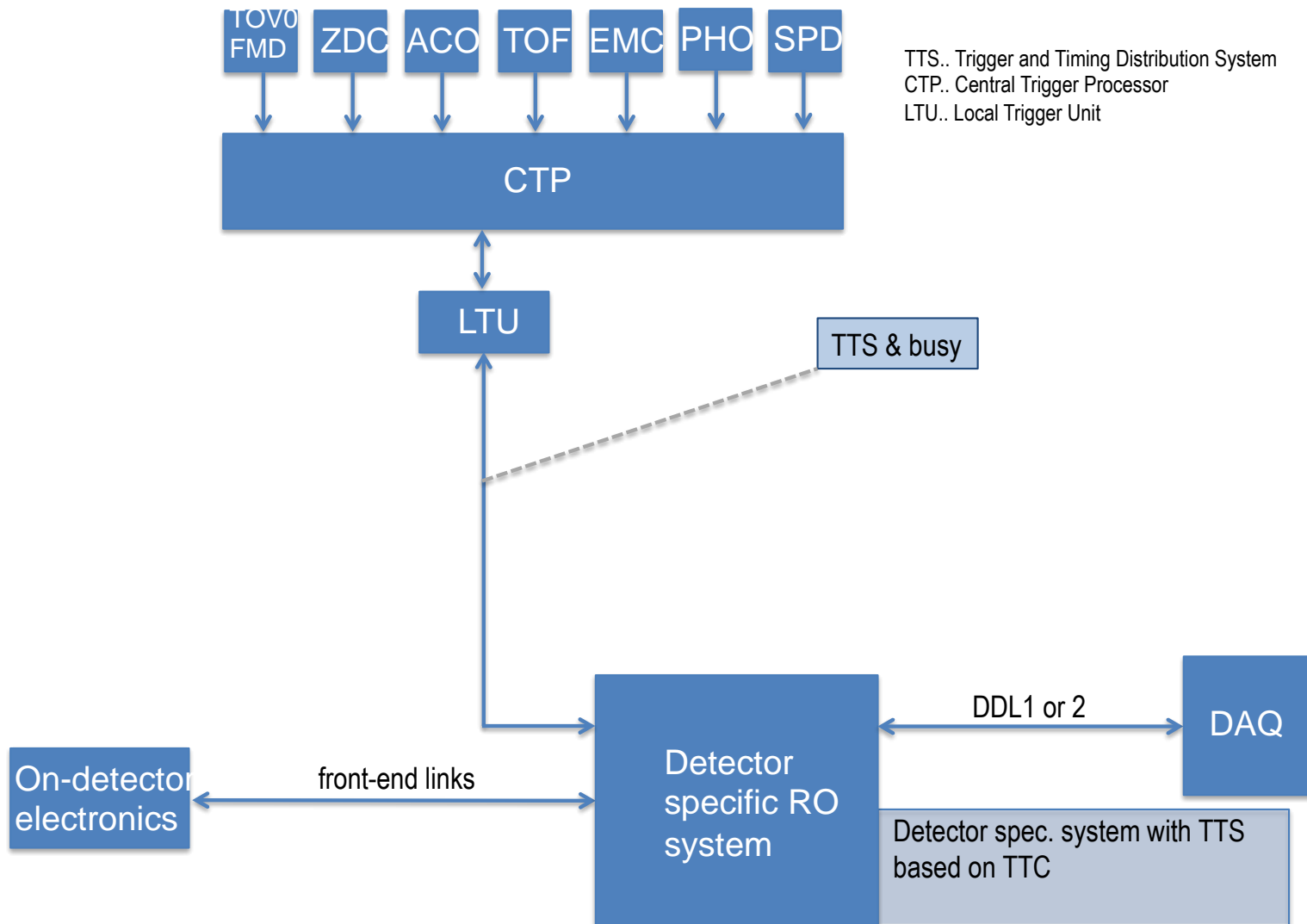
Read-out & Trigger Upgrade architecture

Specifications

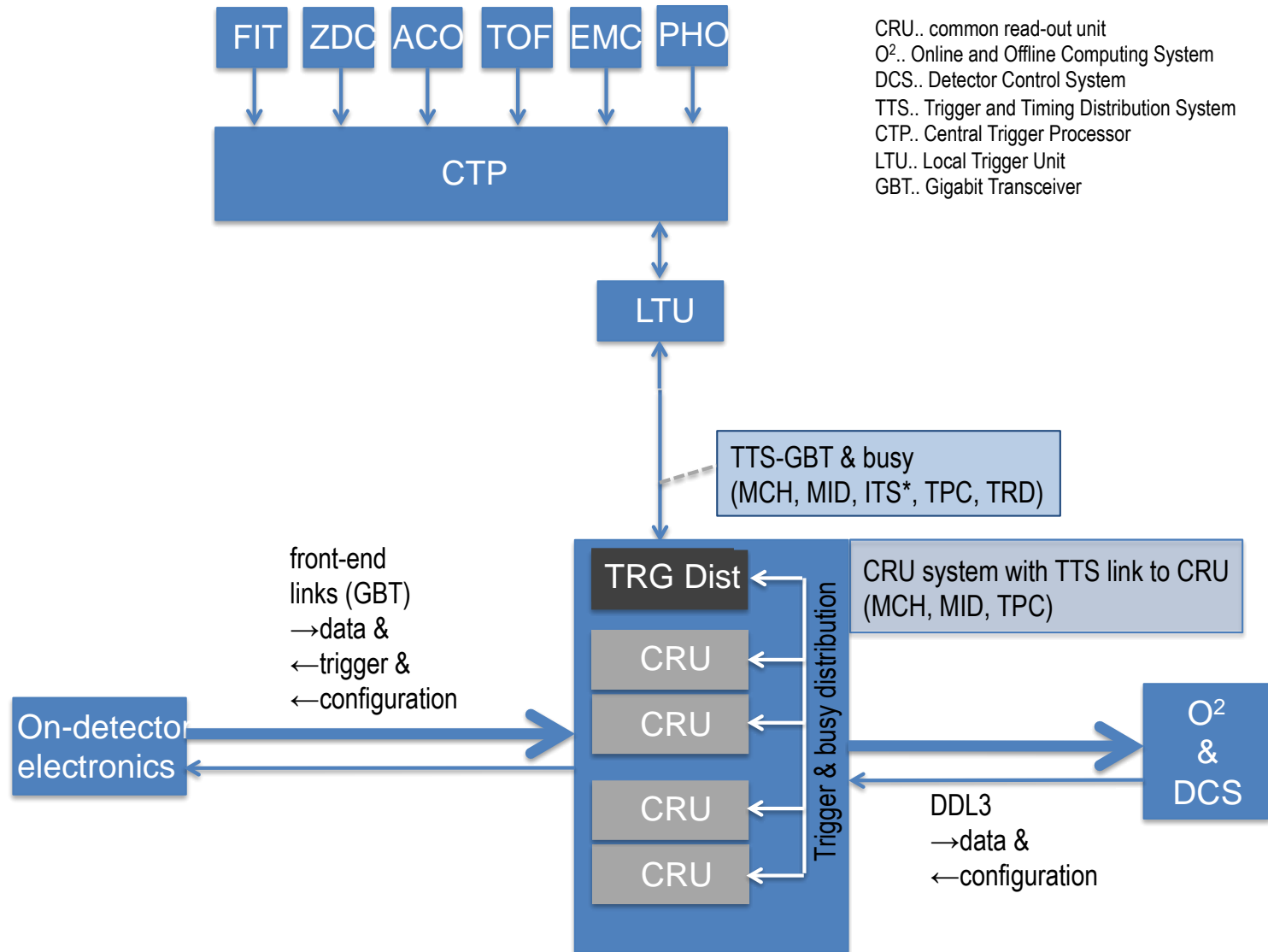


- **Interaction rate Pb-Pb:**
 - from 8 kHz → 50 kHz
- **Trigger rate Pb-Pb:**
 - from ~3.5 kHz → 50 kHz
- **All interactions are read AND recorded**
- **Interaction and trigger rate pp:**
 - → 200 kHz
- **Data rate driven by Pb-Pb**
- **TPC is read continuous & trigger less**

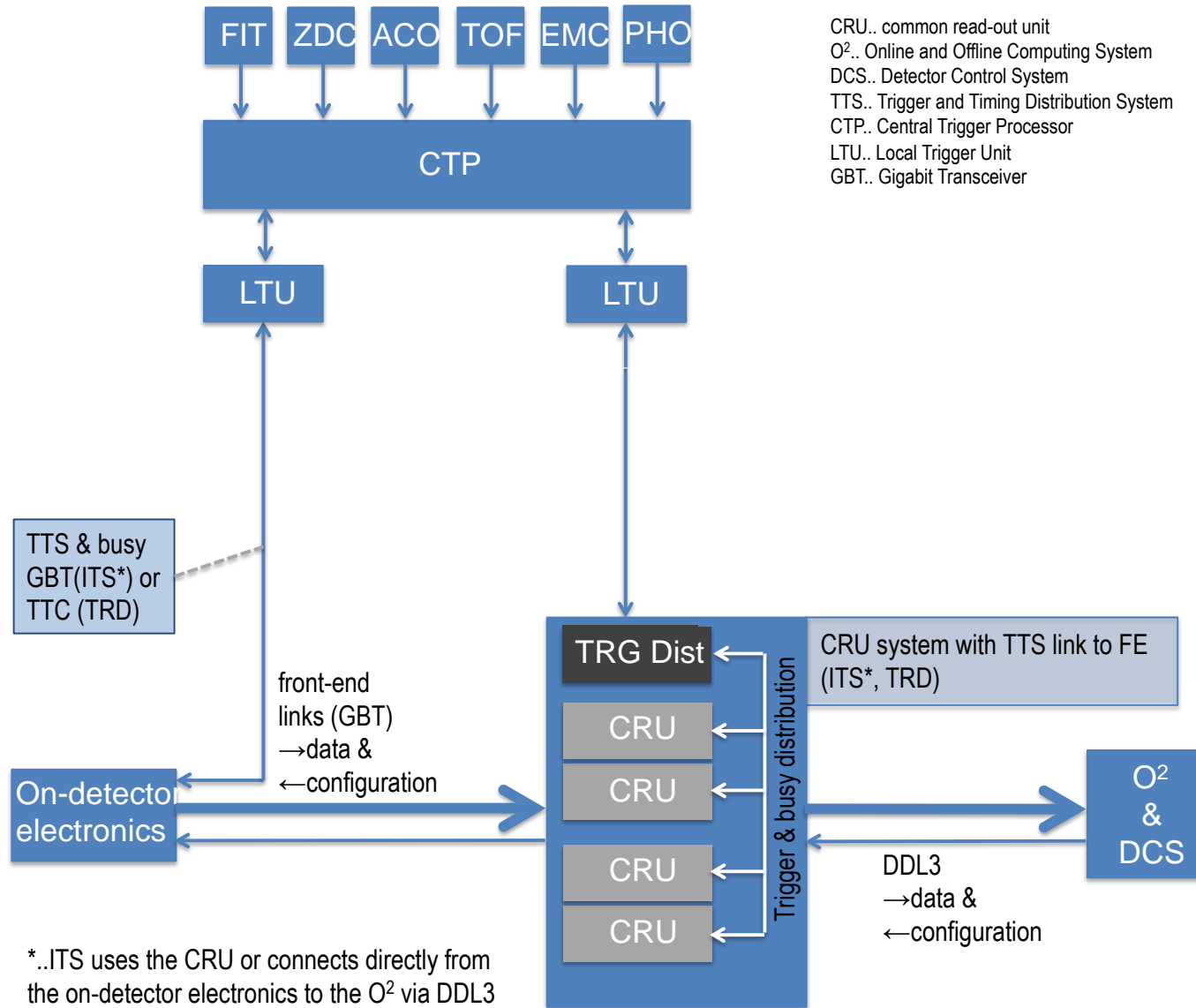
Run1 and Run2 architecture



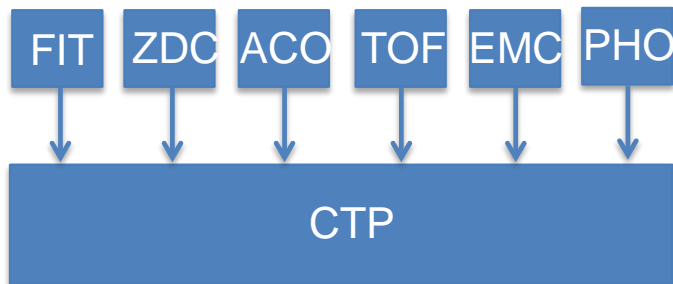
Common read-out unit - CRU & long trigger latency



Common read-out unit - CRU & short trigger latency



Upgrade architecture: det. spec. readout

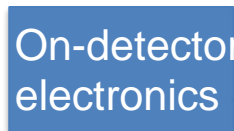


TTS.. Trigger and Timing Distribution System
CTP.. Central Trigger Processor
LTU.. Local Trigger Unit



TTS & busy

front-end links
→ data &
← trigger &
← configuration

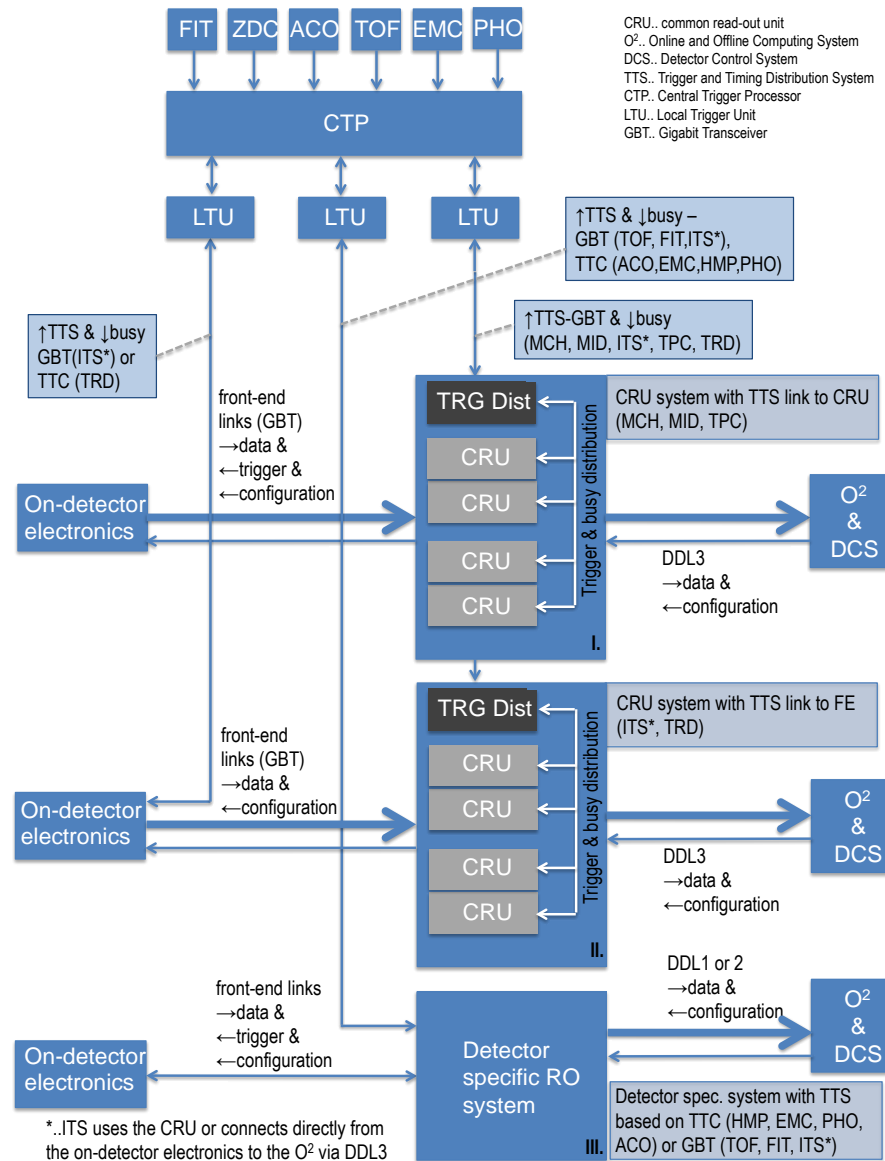


DDL1 or 2
→ data &
← configuration

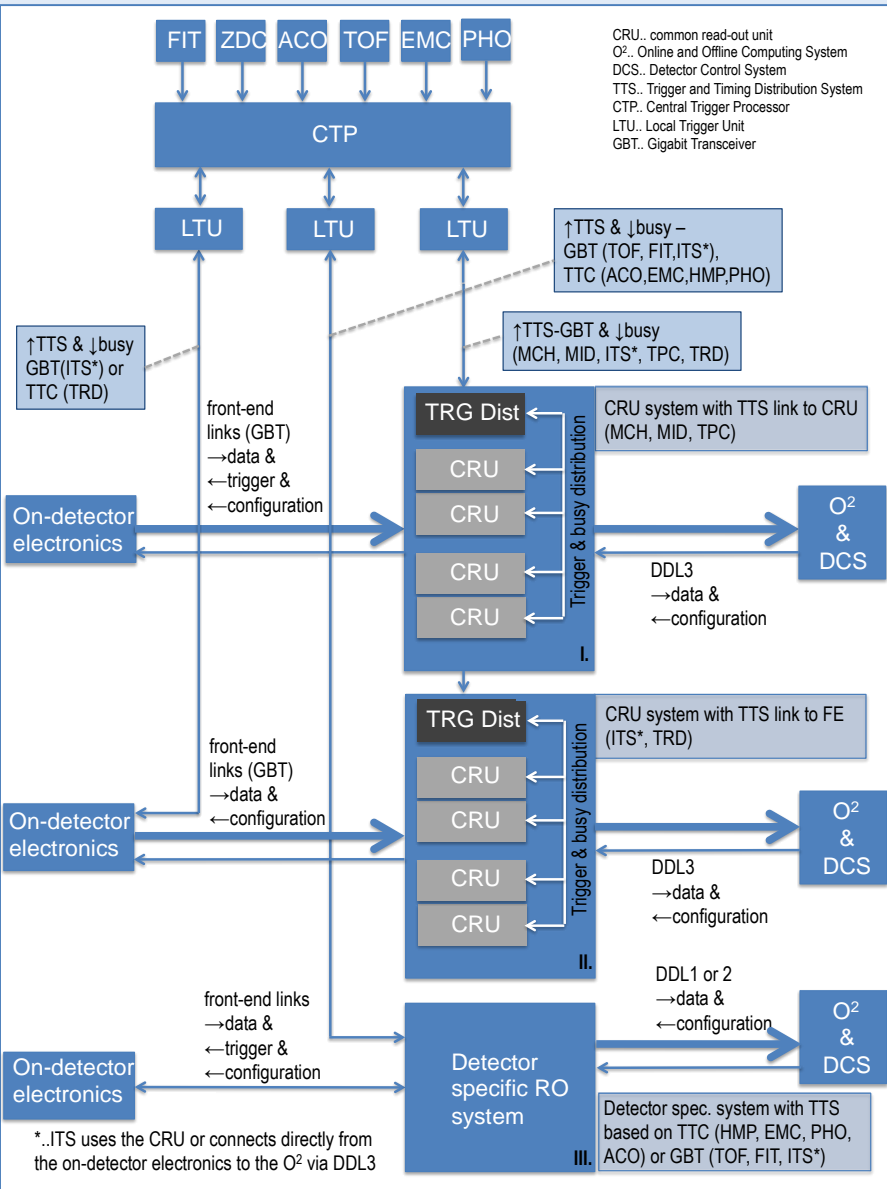


Detector spec. system with TTS based on TTC (HMP, EMC, PHO, ACO) or GBT (TOF, FIT, ITS*)

Upgrade architecture: full read-out system



Upgrade architecture: system components

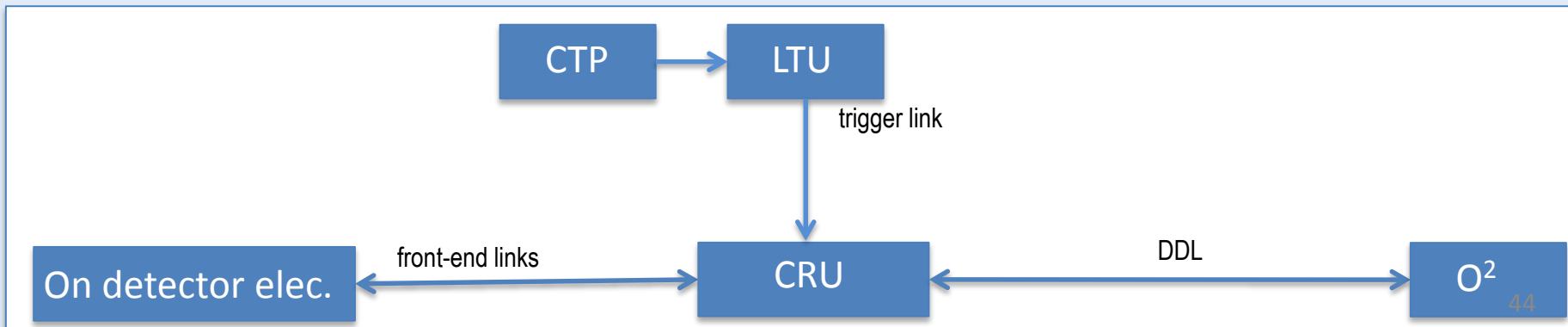


- **DDL**
 - common
- **Off-detector read-out**
 - common readout unit or custom
- **Front-end links**
 - versatile link (GBT) or custom
- **CTP & LTU & TTS**
 - fast serial trigger link (FTL) & TTC
- **On-detector electronics**
 - SAMPA & custom

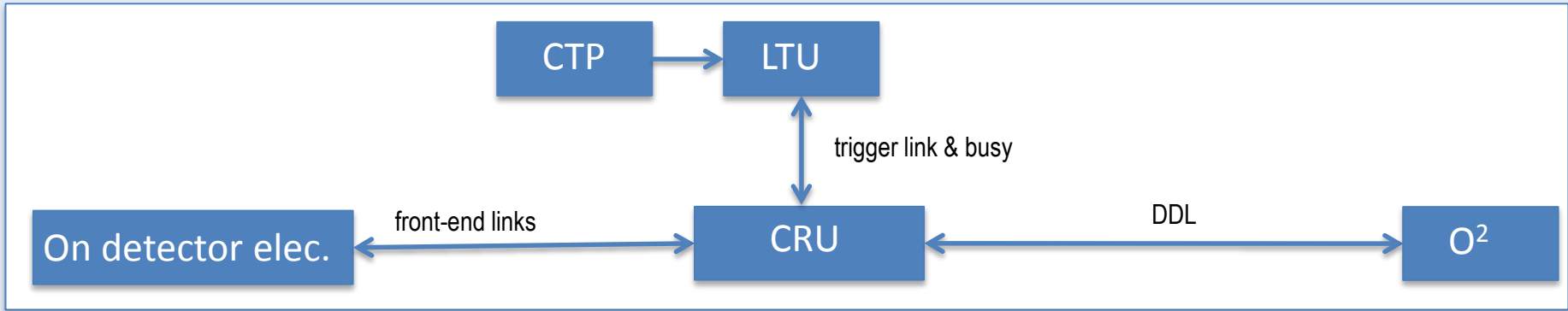
Common Readout Unit – CRU & Detector Data Link - DDL

Read-out architecture

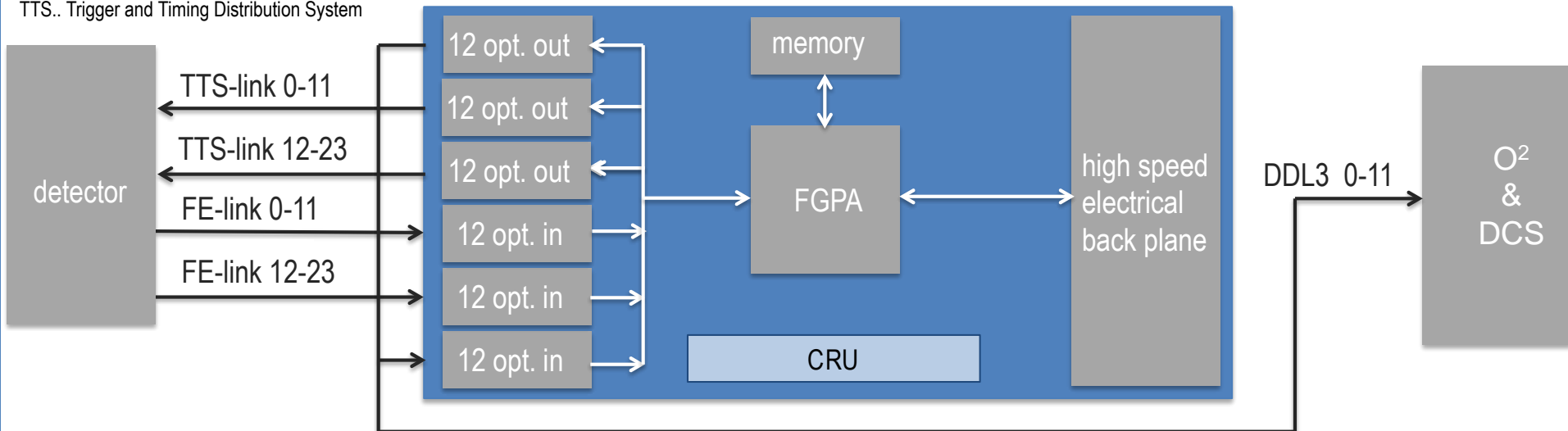
- **Standard interface to DAQ/DCS**
 - **Detector Data Links DDL 1, 2 already developed**
 - 2.125 and 4.25/5.3125 Gb/s
 - **DDL3 based on commercial standard**
 - PCIe plug-in modules
- **Standard interface to Trigger**



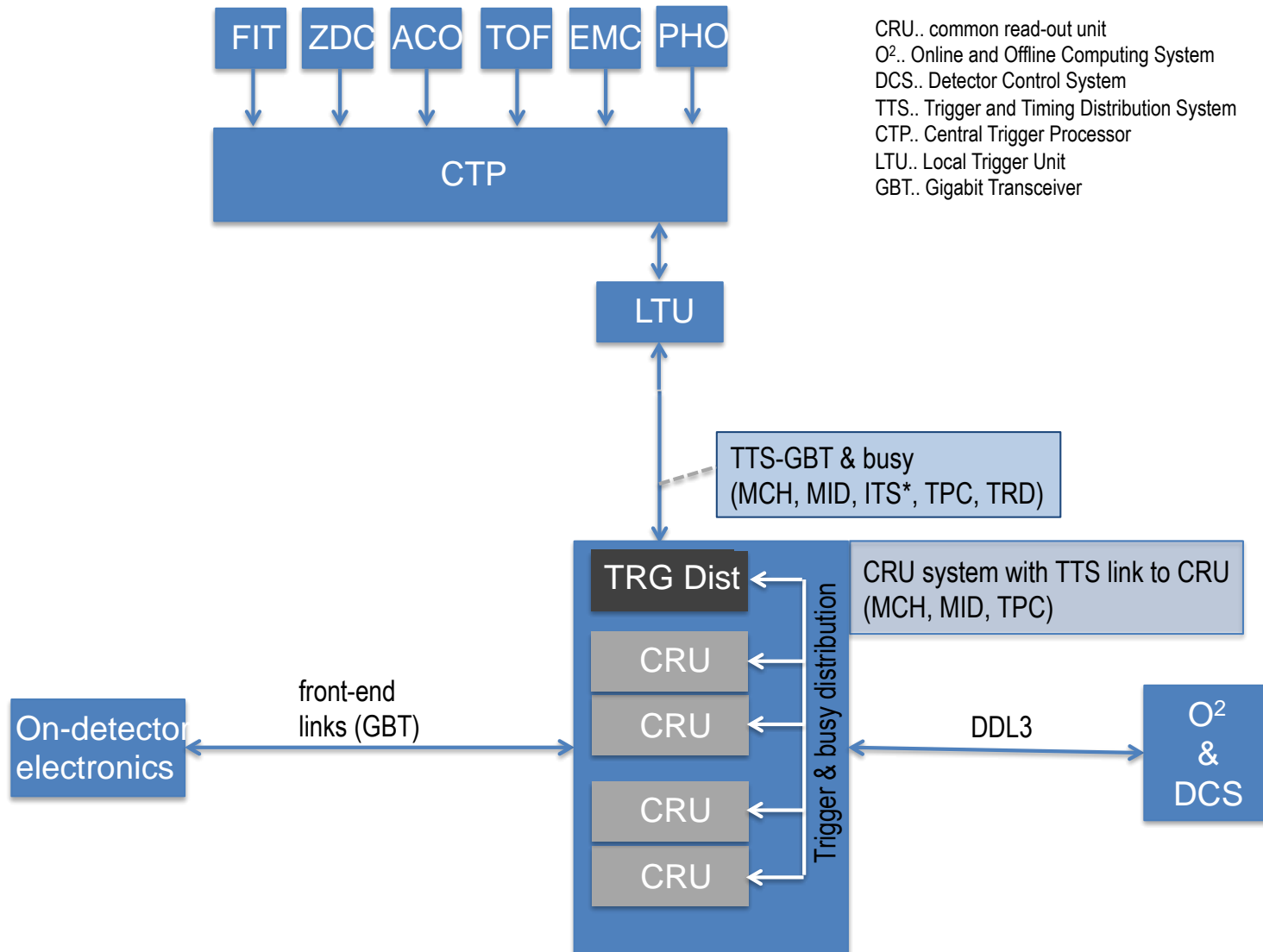
Common readout unit (CRU)



CRU.. common read-out unit
 O².. Online and Offline Computing System
 DCS.. Detector Control System
 TTS.. Trigger and Timing Distribution System



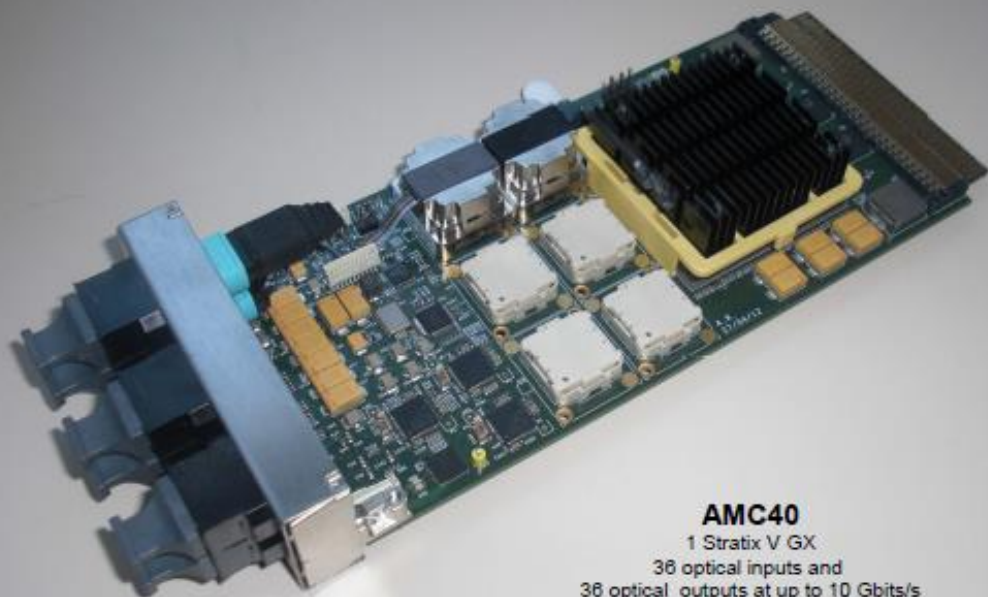
Common readout unit (CRU)



Common readout unit (CRU)

AMC40

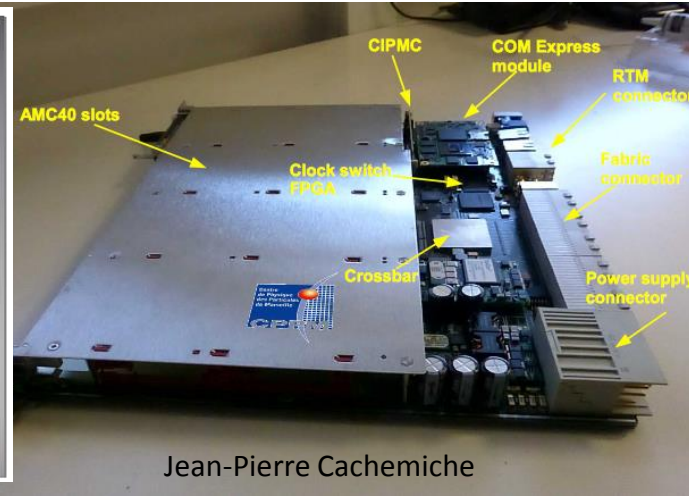
- AMC40 (LHCb)



AMC40
1 Stratix V GX
36 optical inputs and
36 optical outputs at up to 10 Gbits/s
Slow control through PCIe

Jean-Pierre Cachemiche

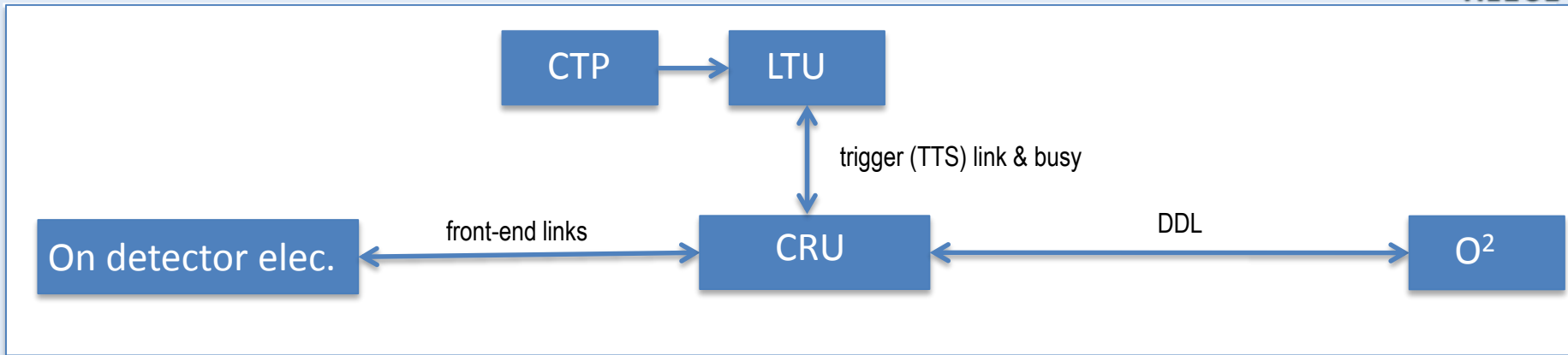
Common readout unit (CRU)



- 4 x AMC40 →
- 1 x motherboard → 14 motherboards →
1 ATCA crate
- Trigger and timing distribution is via
back plane

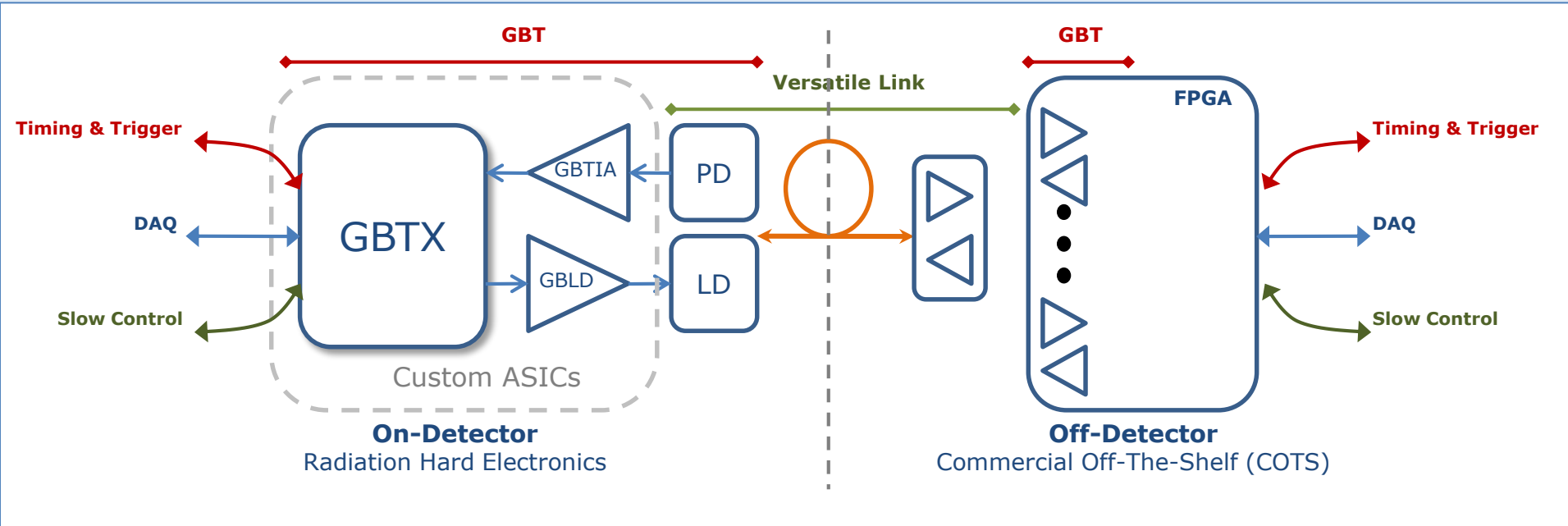
Front-end (FE) links & Trigger and Timing Distribution System (TTS) Links

Common components

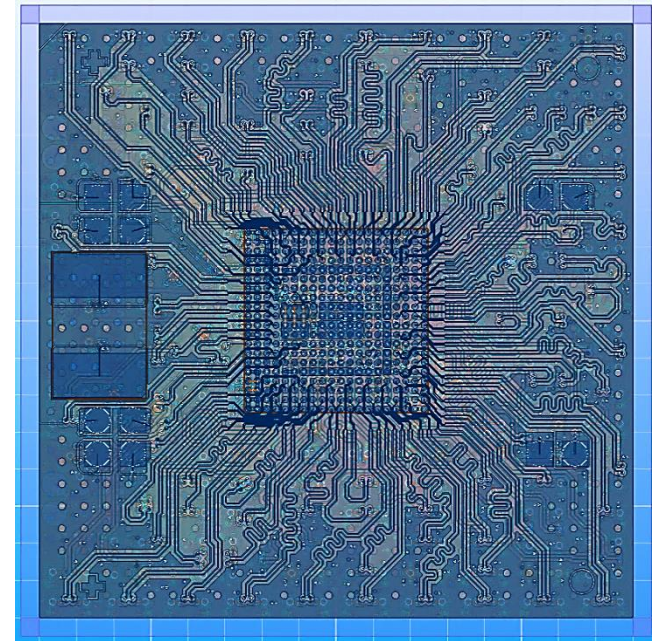
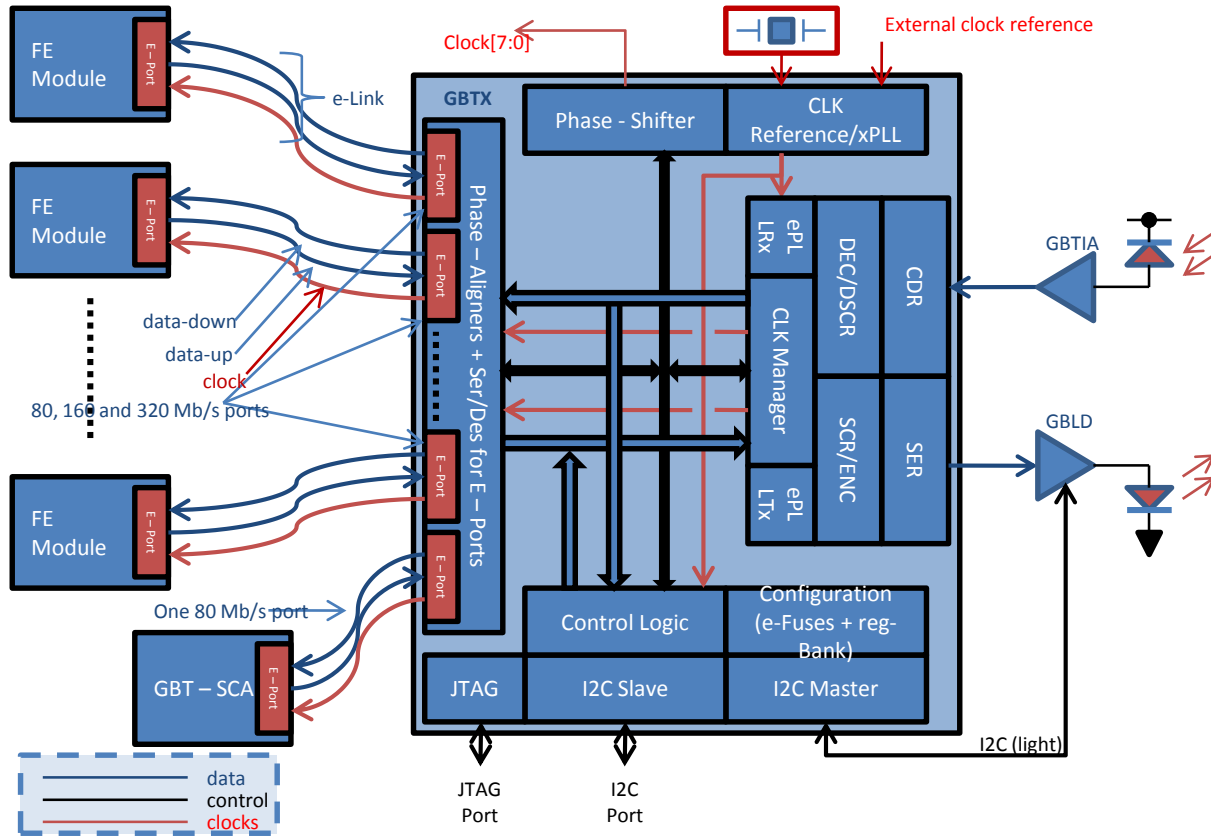


Front-end (FE) links & Trigger and Timing Distribution System (TTS) Links

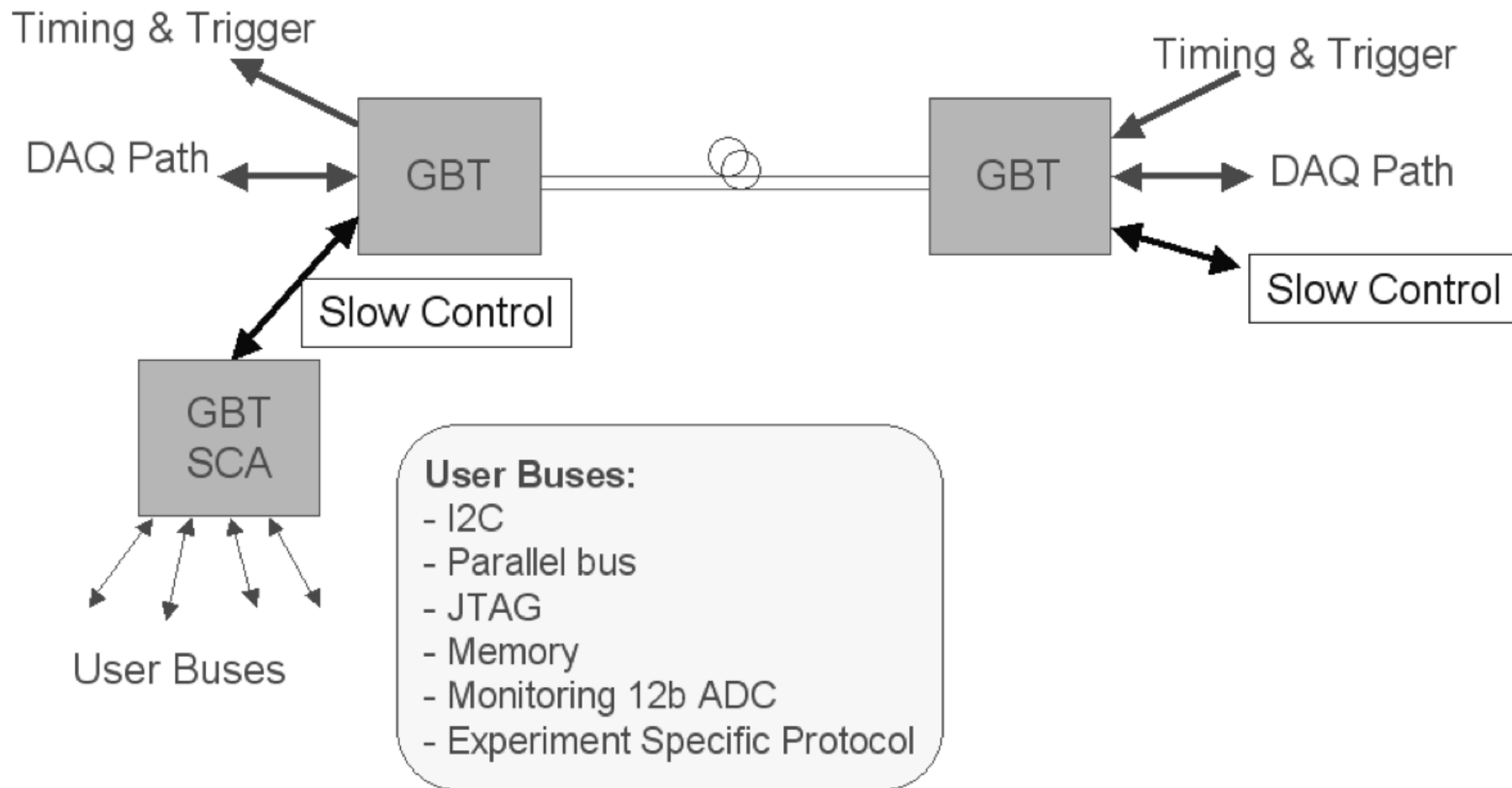
GBT & Versatile link



GBTx



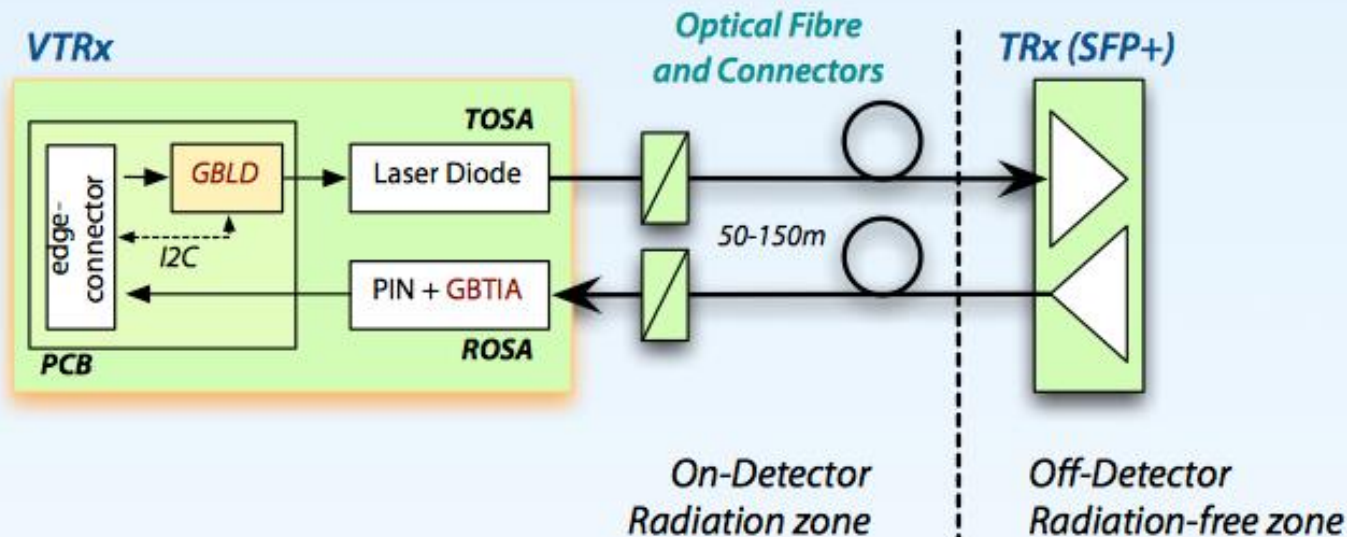
GBT-SCA: slow control adapter



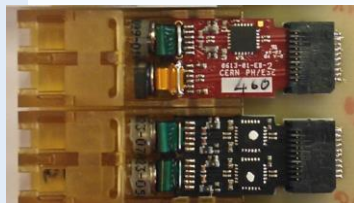
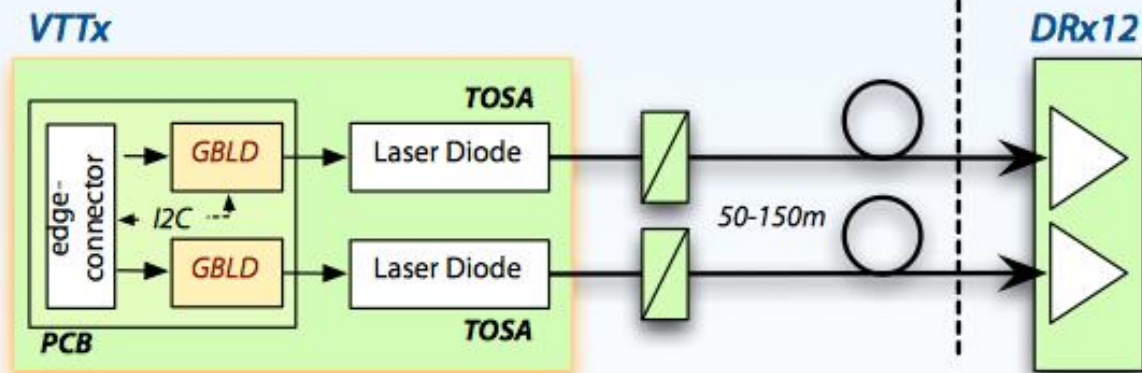
Versatile link components: VTTx & VTRx

Singlemode
EEL/InGaAs

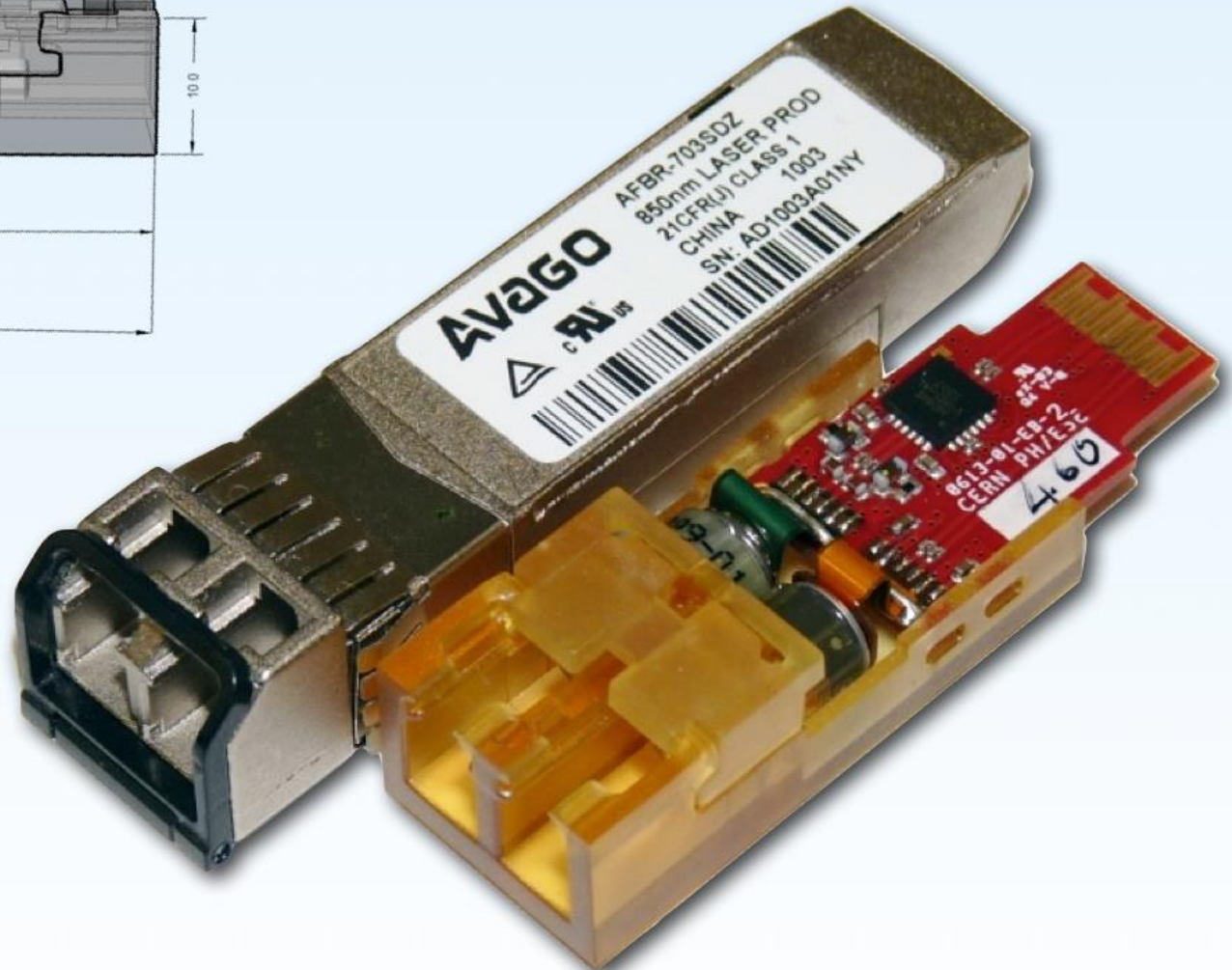
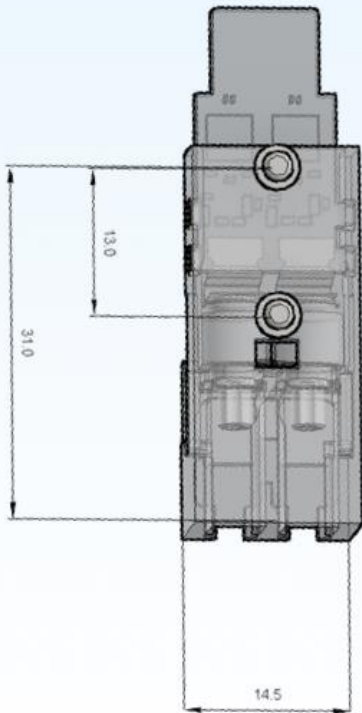
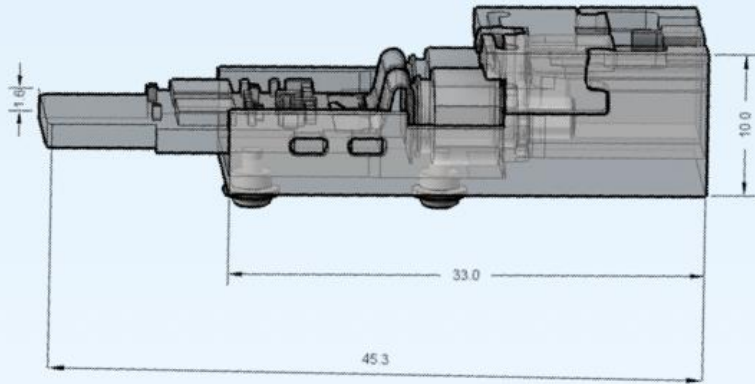
Multimode
VCSEL/GaAs



Multimode
VCSEL

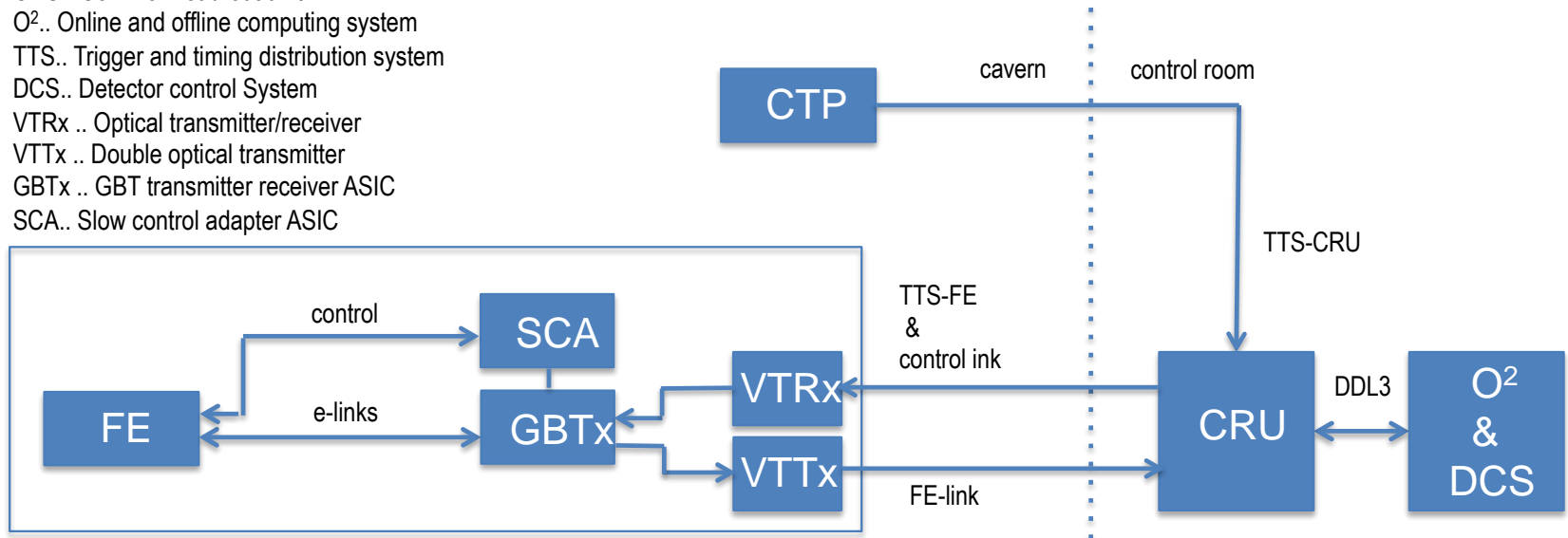


Versatile link components: VTTx & VTRx



CRU & GBT

CTP.. Central trigger processor
CRU.. Common read-out unit
O².. Online and offline computing system
TTS.. Trigger and timing distribution system
DCS.. Detector control System
VTRx .. Optical transmitter/receiver
VTTx .. Double optical transmitter
GBTx .. GBT transmitter receiver ASIC
SCA.. Slow control adapter ASIC



Links

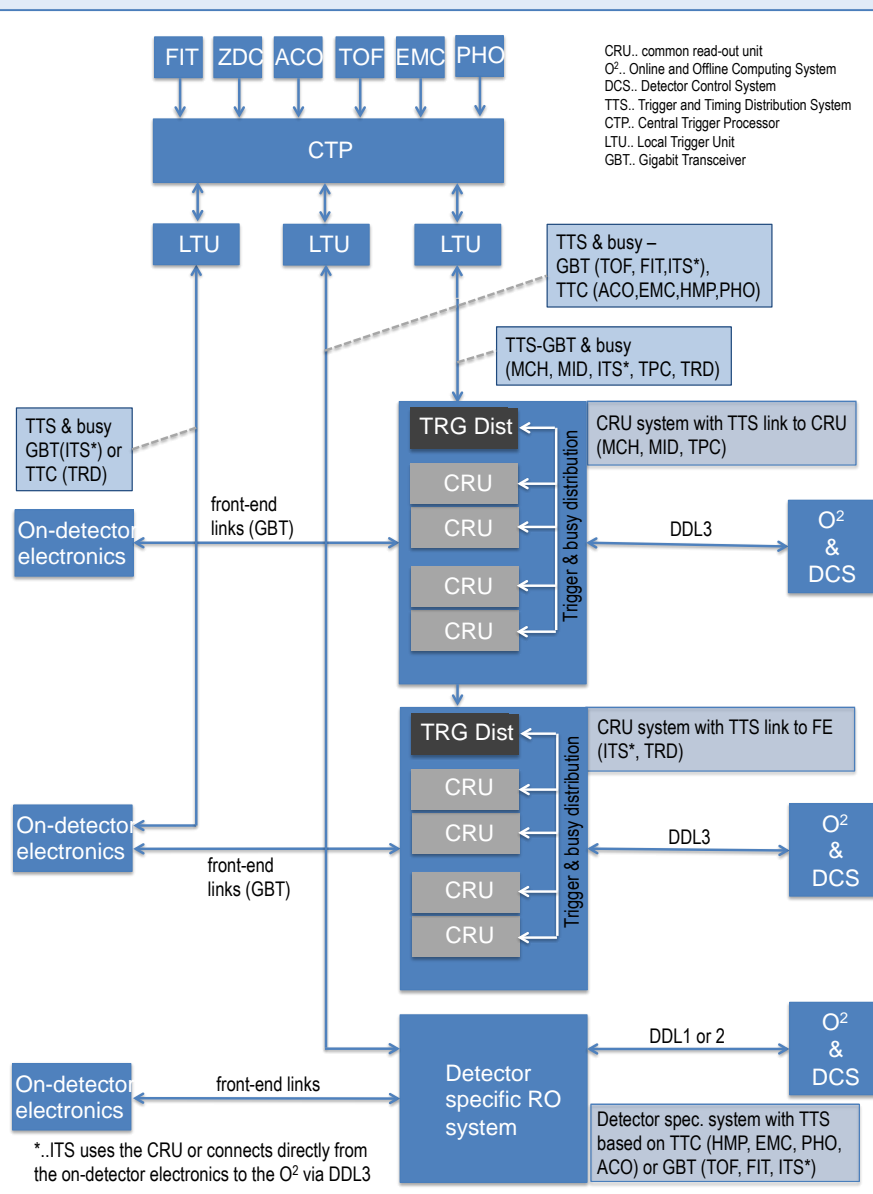


Detector	DDL1	DDL2	DDL3	CRU-FE-links	TTS-FE links
	2.125 Gb/s	4.25-5.3125 Gb/s	10Gb/s	3.2 Gb/s	3.2 Gb/s
TPC			1200	6336	1764
MCH			250	500	500
ITS			*60	*184	0
MID			1	16	16
ZDC			1	1	
TOF		72			
FIT		2			
ACO	1				
TRD			36	1044	0
EMC		20			
PHO		16			
HMP	14				
Total	15	110	1555	8081	2244

Central Trigger Processor (CTP) & Local Trigger Processor (LTU)

CTP & LTU

CTP & LTU: based on high performance FPGA processor
 Logic combinations fully programmable



System description: Trigger signals

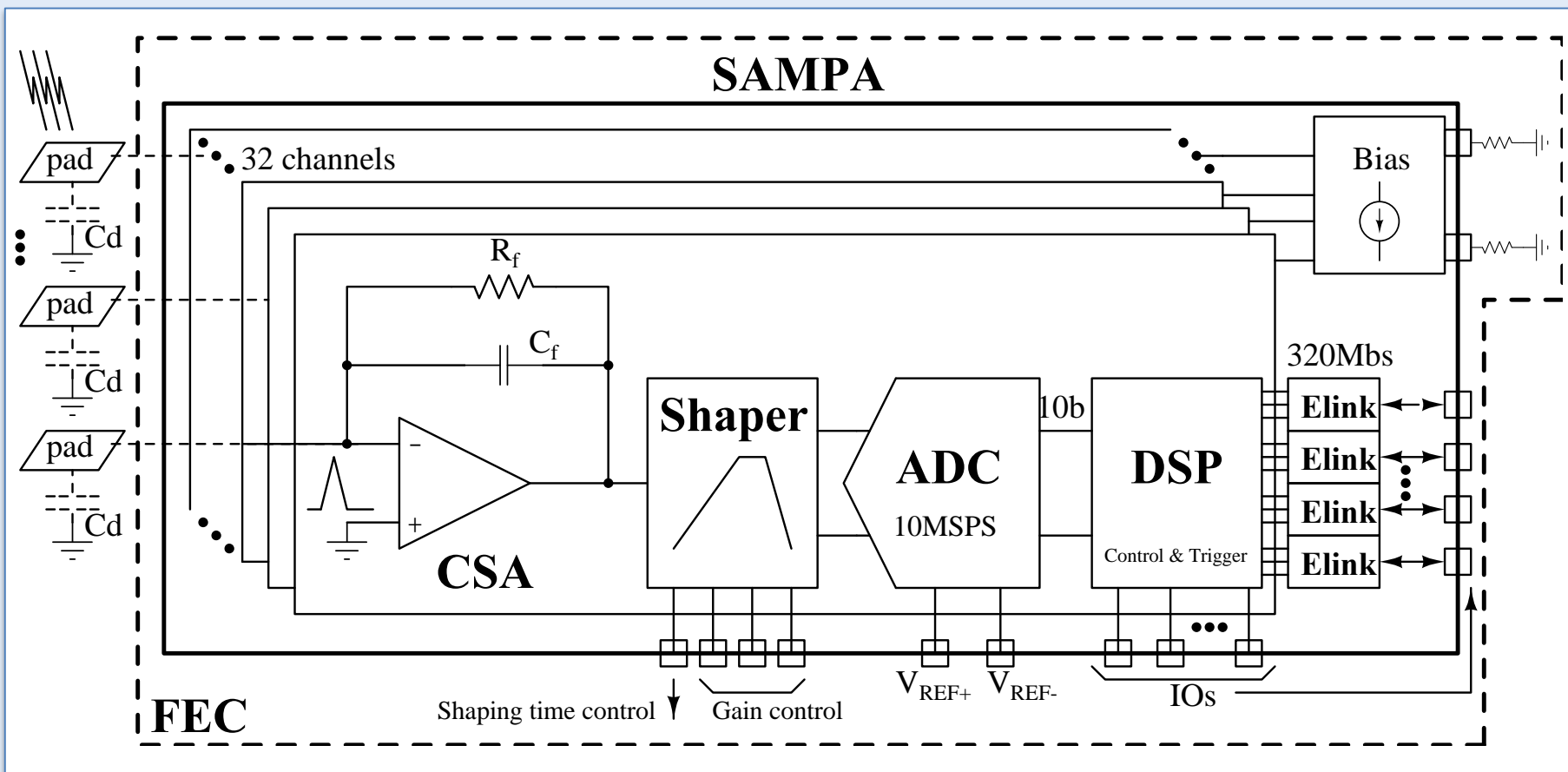


Level	Trigger Input to CTP [ns]	Trigger output at CTP [ns]	Trigger decision at detector * [ns]	contributing detectors
LM	425	525	775	FIT
L0	1200	1300	1500	ACO, EMC, PHO, TOF, ZDC
L1	#6100	#6200	#6400	EMC, ZDC

- LM .. pretrigger wake up signal for TRD: by FIT only
- L0 .. main trigger signal: by FIT & additional trigger inputs
- L1 .. optional EMC-jet and ZDC contribution: long latency

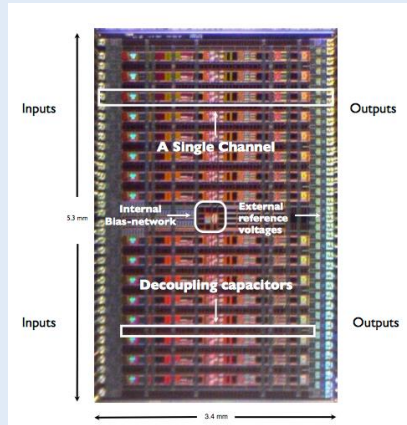
Common TPC/MCH readout ASIC

- common read-out ASIC
- TPC & muon chambers

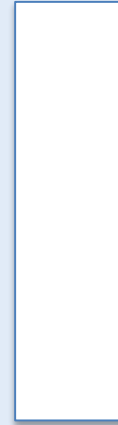
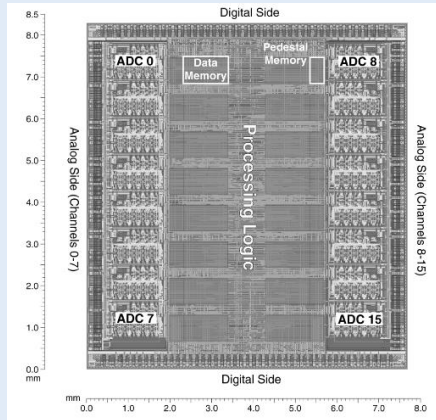


SAMPA

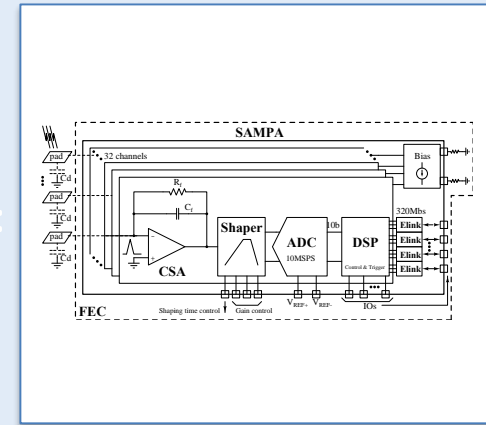
PASA



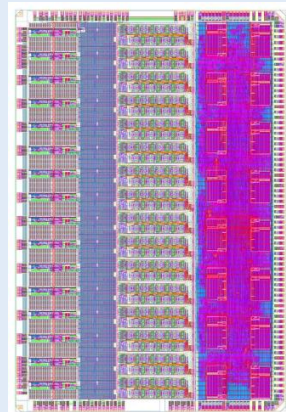
ALTRO Cont. RO



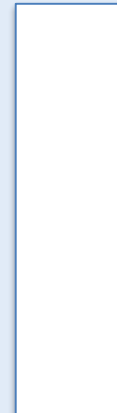
SAMPA



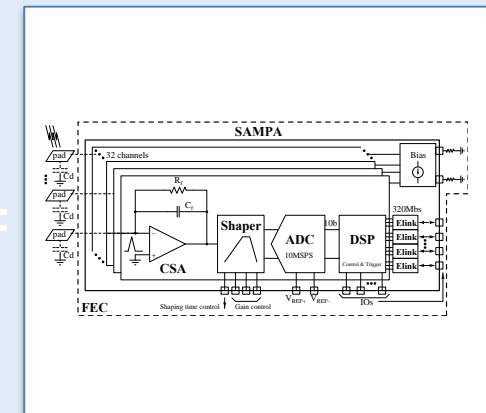
S-ALTRO



Cont. RO



SAMPA



- SAMPA is evolution from PASA / ALTRO & S-ALTRO
- Analog specifications are almost identical

- **TPC & muon chambers (MCH)**
 - 32 channel amplifier-shaper-ADC-DSP
 - triggerless/continuous & triggered readout
 - < 600 e @ 25 pF (TPC), < 950 e @ 40 p (MCH)
 - bi-polarity input
 - 10 bit ADC – 10/20 Msamples/s
 - on ASIC base-line correction and zero suppression
 - 4 x 320 Mbit/s serial outputs
 - 130 nm TSMC CMOS process

Detector Summary

Sub-detector parameter overview



Det	triggered by () = optional	Pb-Pb RO rate [kHz]	TTS FTL/TTC	CRU used
TPC	(L0 or L1)	50	FTL	y
MCH	(L0 or L1)	100	FTL	y
ITS	L0	100	FTL	*y
MID	L0 or L1	>100	FTL	y
ZDC	L0	>100	FTL	y
TOF	L0 or L1	>100	FTL	n
FIT	L0 or L1	100	FTL	n
ACO	L0 or L1	100	TTC	n
TRD	LM&(L0 or L1)	39	FTL&TTC	y
EMC	#L0&L1	46	TTC	n
PHO	#L0&L1	46	TTC	n
HMP	#L0&L1	2.5	TTC	n

Sub-detector upgrade effort



Det	# channels	Run1&2 RO rate [kHz]	upgrade RO rate [kHz]	FE ASIC	FEC	ROC
TPC	5×10^5	3.5	50	17000 SAMPA	3400	CRU
MCH	10^6	1	100	33000 SAMPA	500	CRU
ITS	25×10^9	0.5	100	25000 ASICs	184	CRU
MID	21×10^3	1	100	FEERIC	234	CRU
ZDC	22	8	100	commercial&1	ZRC	CRU
TOF	1.6×10^5	40	100			72 DRM
FIT	160 + 64	80	100		upgrade	DRM(TOF)
ACO	120	100	100			
TRD	1.2×10^6	1	50			CRU
EMC	18×10^3	3.7	46			
PHO	17×10^3	3.7	46			
HMP	1.6×10^5	2.5	2.5			

Summary



- **Rate upgrade: 50 kHz**
- **New ITS & MFT**
- **TPC GEMs & continuous, trigger-less read-out**
- **Muon system electronics upgraded**
- **Common component approach widened**

Backup



Radiation Levels

Radiation levels



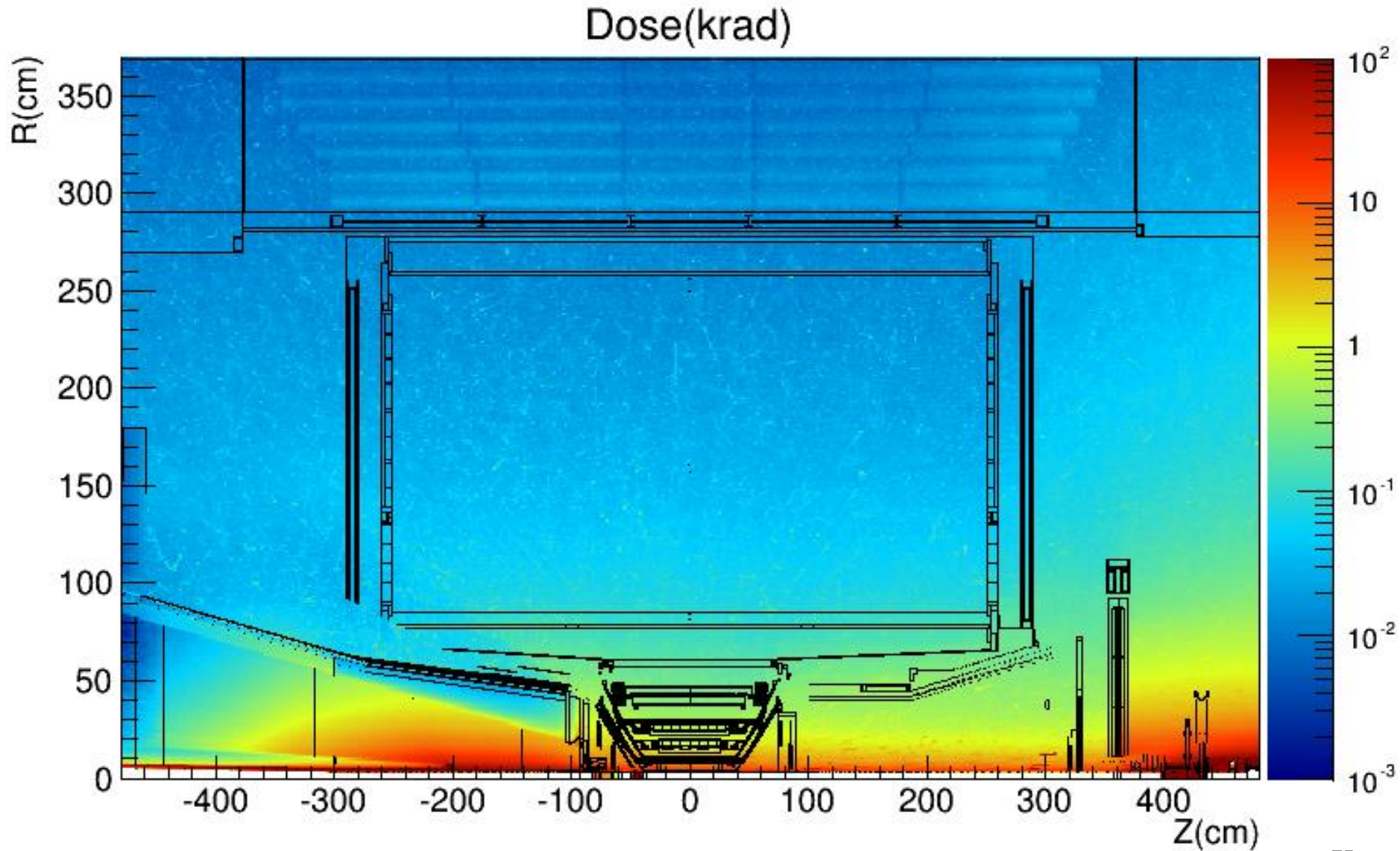
Element	r (cm)	z (cm)	TID (krad)	1 MeV neq (cm ⁻²)	>20 MeV had. (kHz/cm ²)
ITS L0	2.2	[-13.5, 13.5]	646	9.2×10^{12}	1600
ITS L1	2.8	[-13.5, 13.5]	387	6.0×10^{12}	1000
ITS L2	3.6	[-13.5, 13.5]	216	3.8×10^{12}	500
ITS L3	20	[-42.1, 42.1]	13	5.2×10^{11}	28
ITS L4	22	[-42.1, 42.1]	9	5.0×10^{11}	24
ITS L5	41	[-73.7, 73.7]	6	4.6×10^{11}	10
ITS L5	43	[-73.7, 73.7]	4	4.6×10^{11}	9
MFT D0	2.5	-50	395	6.7×10^{12}	1100
MFT D1	2.5	-58	392	6.4×10^{12}	1040
MFT D2	3.0	-66	767	5.9×10^{12}	760
MFT D3	3.5	-72	427	4.3×10^{12}	520
MFT D4	3.5	-76	541	4.8×10^{12}	560
FIT1	5	-80	181	3.0×10^{12}	280
FIT2	5	340	103	1.4×10^{12}	200
TPC In	79	[-260, 260]	2.1	3.4×10^{11}	3.4
TPC Out	258	[-260, 260]	0.3	5.2×10^{10}	0.7
TRD	290	[-390, 390]	0.4	4.8×10^{10}	0.54
TOF	370	[-370, 370]	0.13	2.6×10^{10}	0.26
EMCAL	430	[-340, 340]	0.06	1.5×10^{10}	0.02
MCH S1	19	-536	0.42	4.2×10^{11}	3
MCH S2	24	-686	0.19	1.4×10^{11}	1
MCH S3	34	-983	0.14	1.6×10^{11}	0.9
MCH S4	45	-1292	0.18	3.0×10^{11}	1
MCH S5	50	-1422	0.91	2.5×10^{11}	0.7
CTP Rack	600	-1295	4.8×10^{-3}	7.8×10^9	0.03

Factor 10 safety on
TID & neq:
TID/neq numbers
factor 2 higher than
ALICE-Run1/2
design rates

Factor 2 safety on
>20 MeV hadrons:
factor 3 higher than
ALICE-Run1/2
design rates

Table 3.1: Total Ionizing Dose (TID) and 1 MeV neq hadron fluence for 10nb^{-1} PbPb + $6\text{pb}^{-1}\text{pp}$ + $50\text{nb}^{-1}\text{pPb}$ collisions (including a safety factor 10) as well as high energy hadron fluence for 50 kHz PbPb collisions (including a safety factor 2).

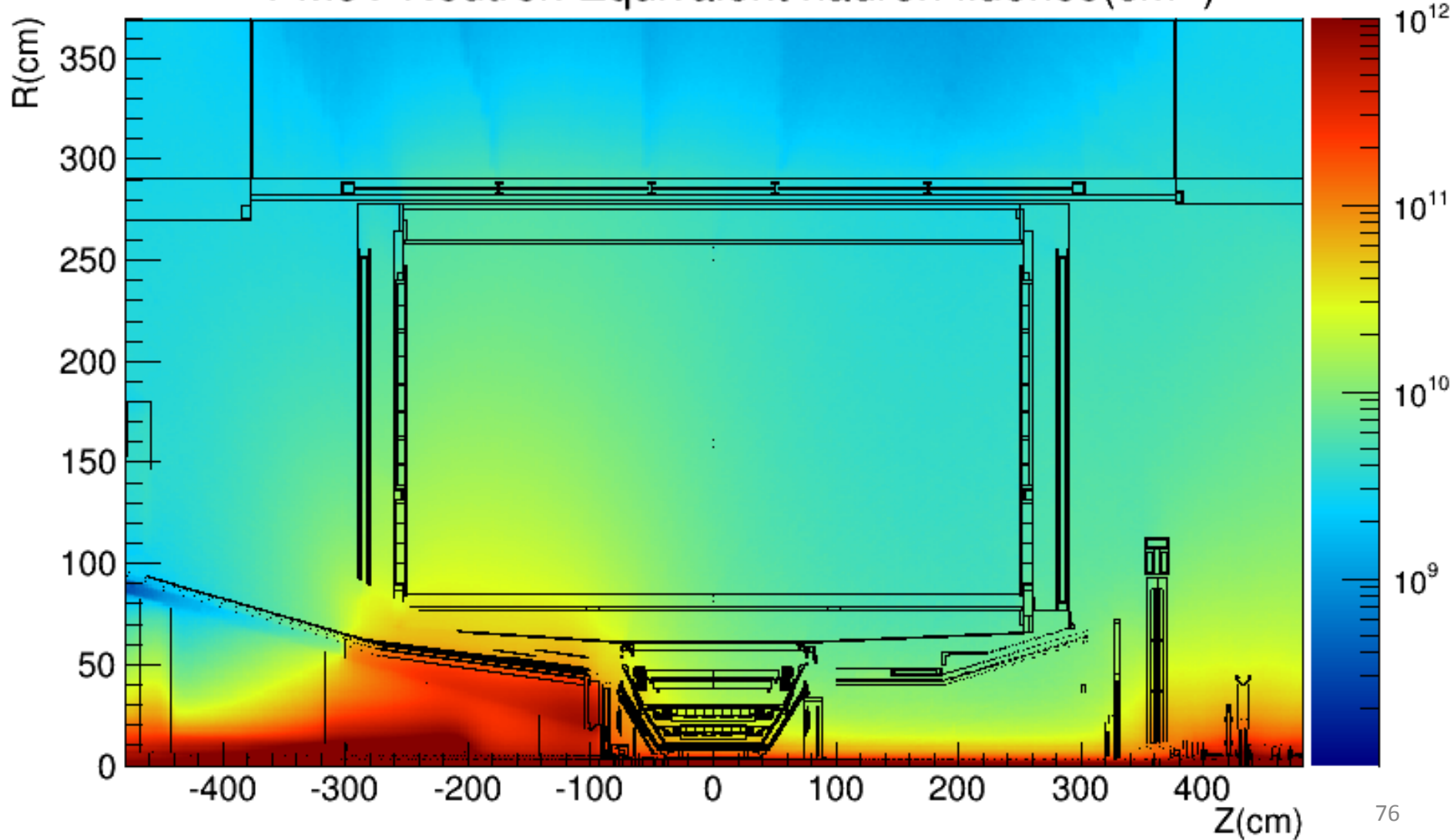
Radiation



Radiation



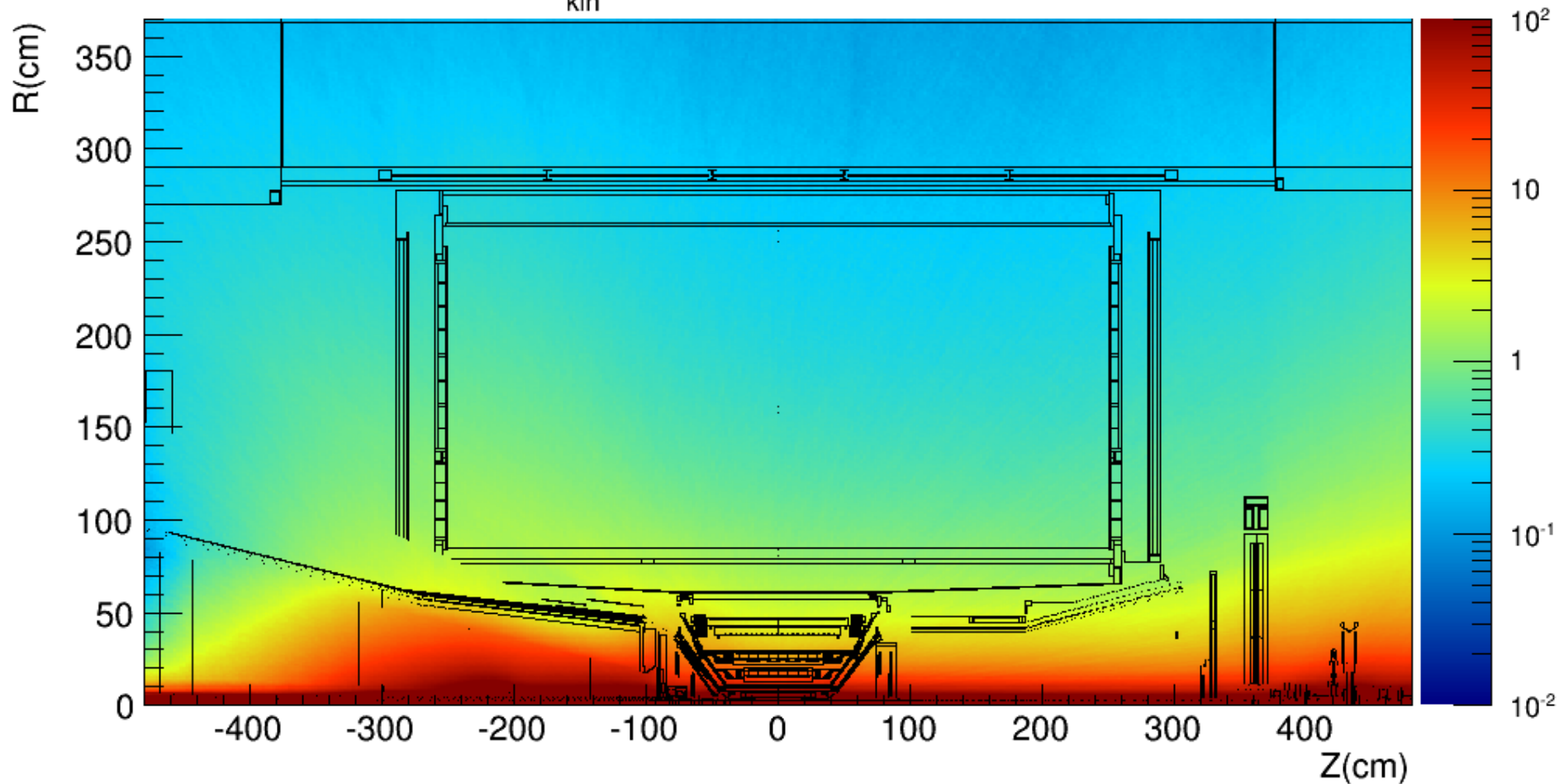
1 MeV Neutron Equivalent hadron fluence(cm^{-2})



Radiation

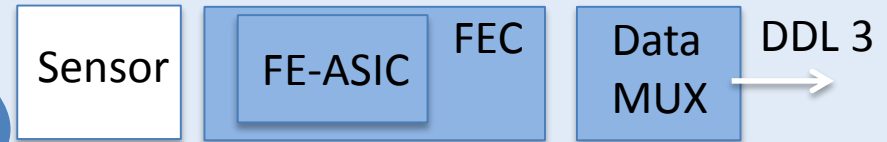


High-energetic ($E_{\text{kin}} > 20 \text{ MeV}$) hadron fluence rate (kHz/cm^2)



Detector Summary

Muon identifier



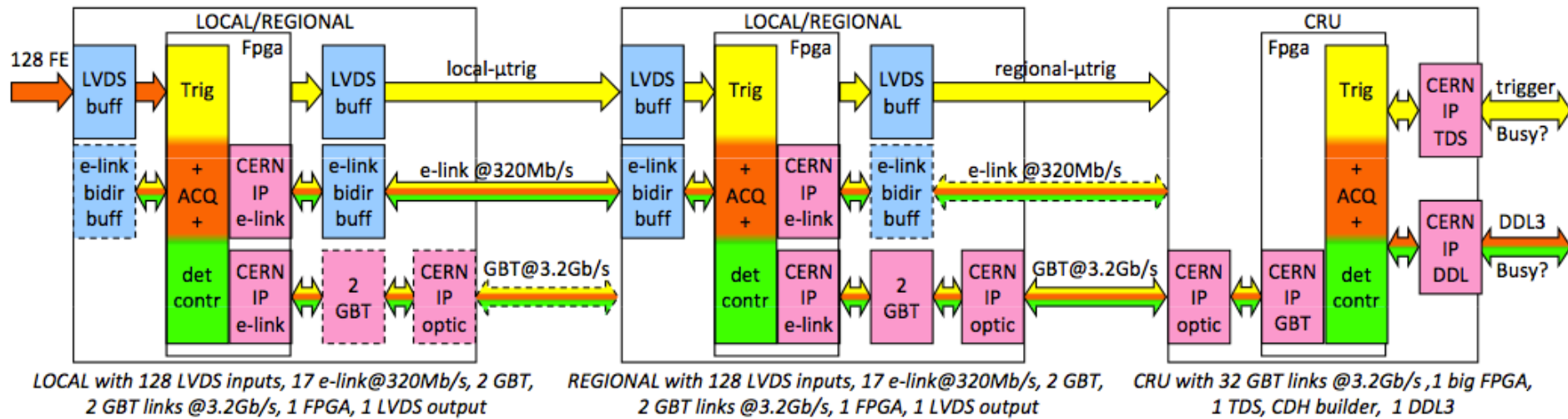
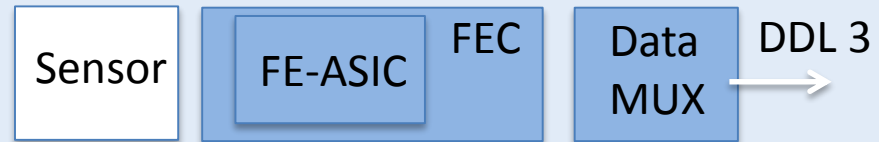
- **21.000 channels (RPC)**
- **replacement of front-end electronics to slow down aging speed of RPCs**
 - by operation in avalanche mode reducing charge produced in the gas
- **Front-end ASIC is replaced by FEERIC ASIC**
 - with amplification
- **Readout out at 100 kHz @ 0 % busy**

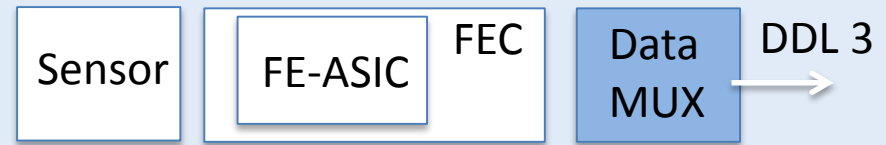
Muon identifier



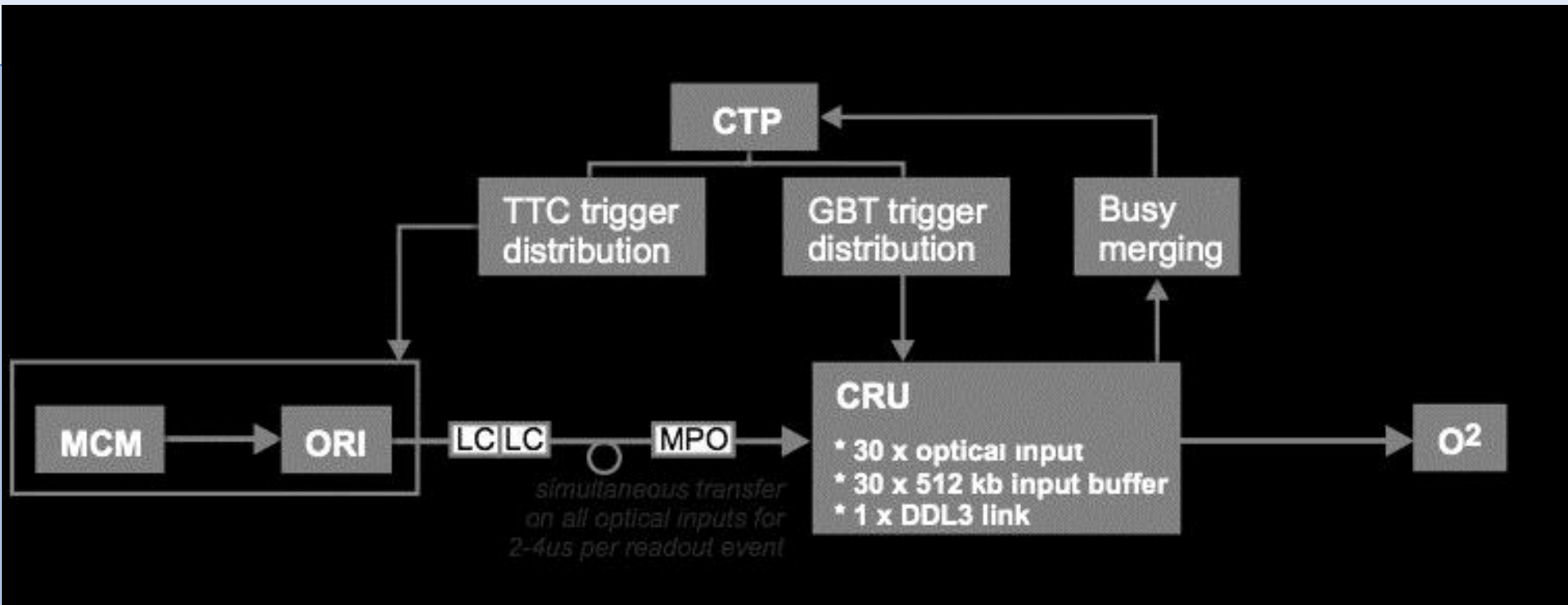
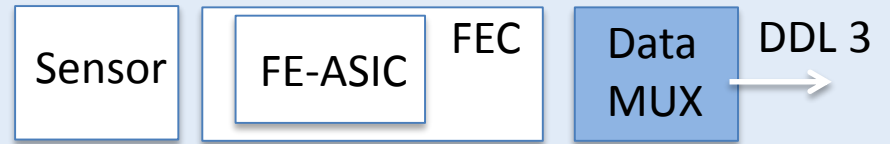
- **Replacement of 2 levels of data concentrators by 234 new front-end cards and CRUs**
- **Small scale system with FEERIC will be tested already in run 2**

Muon identifier

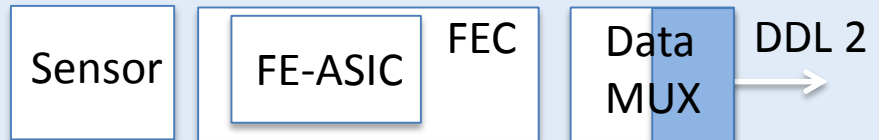




- **1.151.000 channels**
- **rate upgrade from 8 kHz to 50 kHz with 23 % busy**
- **triggered operation (LM & L0)**
- **FE electronics unchanged, but data load reduced with firmware change**
 - **pre-processed data (tracklets) are transferred only or**
 - **partial read-out based on electron region candidates**
- **Data MUX is CRU**

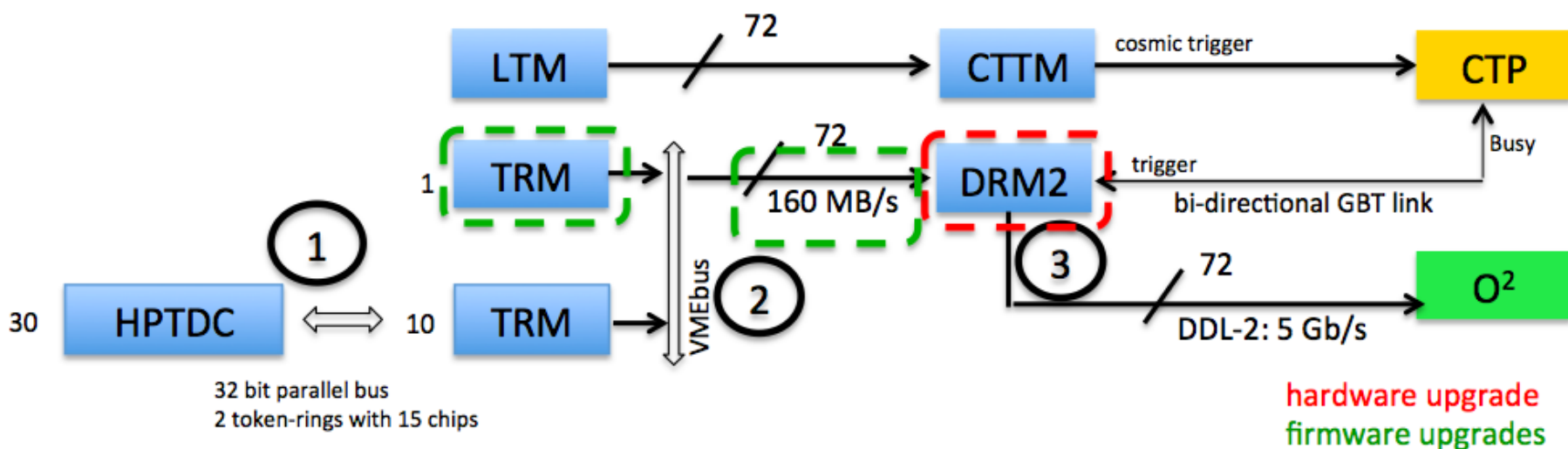
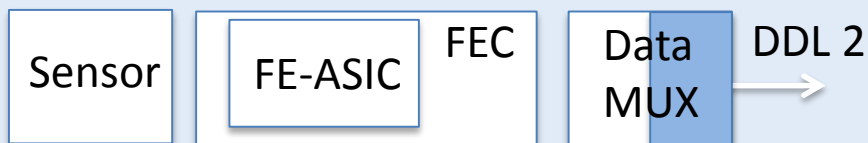


- **~160.000 MRPC pads**

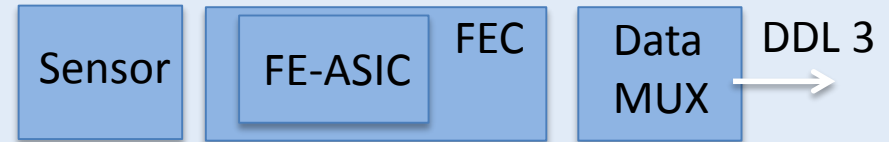


- **rate upgrade from 10s of kHz to 100 kHz PbPb without dead time**
 - max limit by HPTDC in FEC is 265 kHz
 - rate limit comes from VME based read-out and data format
- **upgrade firmware for data format and VME protocol**
- **replace 72 2nd level data concentrator boards (DRM)**

TOF







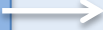
Detector developments: ITS



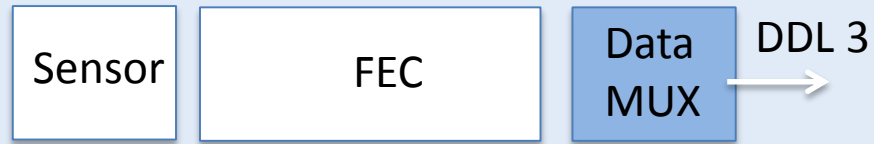
- **25 G pixels**
- **complete new detector**
 - ASIC, sensor, read-out, mechanics cooling
- **triggered @ L0**
- **Detector module sends data 1 Gb/s links**
 - base-line electrical
 - close to detector link interface needed

Detector developments: FIT



- **160 MCP-PMT +**      DDL 2
- **64 Scintillators**
- **Provides interaction trigger**
- **timing reference for TOF**
- **multiplicity measurement**
- **New detector implementation**
 - **new front-end**
 - **RO based on TOF read-out scheme**

Detector developments: ZDC



- **22 channels**
- **outside of radiation zone**
- **use NIM, VME and commercial electronics**
- **provides timing trigger**
- **upgrade from 8 kHz to 16 kHz by introduction of multi-event buffers in firmware (run 2)**
- **to 100 kHz without dead time**
 - **commercial digitizers with on board FPGAs**
 - **TDC model firmware upgrade**
 - **replacement of data concentrator card (ZRC) and**
 - **use CRU**

Detector developments: EMC



- **~ 18.000 channels**



- **provides trigger**

- **L0 input: sum**

- **L1 input: shower and jet**

- **has already been upgraded to 46 kHz @ 15 % busy**

- **front end (ALTRO) limits to 50 kHz**

- **data reduction by on-line data evaluation**

- **replacement of data concentrators by SRU (Scalable Read-out Unit, RD51)**

Detector developments: PHO



- **~ 17.000 channels**



- **provides trigger**

- **L0 input: sum**

- **taking same approach as EMC to 46 kHz @ with busy time**

- **front end (ALTRO) limits to 50 kHz**
- **data reduction sample number reduction**
- **replacement of data concentrators by SRU (Scalable Read-out Unit, RD51)**
- **replacement of trigger region units (TRU)**

Detector developments: HMP



- **~160.000 channels MWPC**
- **RO rate to 2,5 kHz**
- **No detector/electronics change**