ATLAS Phase-2 Upgrade Overview/Status

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- Brief overview of Phase-1 upgrades
- Key features of LoI Phase-2 Upgrade
- Current “Reference Scenario” for Phase-2 Upgrade
  - Options being explored => not a single monolithic design yet
  - Core technologies/strategies largely defined, active R&D program
  - TDRs defined, nominal schedules between Q4 2016 and Q4 2017
- Today: focus on detector – interesting performance results next time !

Brief Overview of Phase-1 Upgrades

- Four major TDRs submitted and endorsed by LHCC in Dec 2013. These upgrades provide improved capabilities for higher luminosities of Run 3, but also form the initial steps towards phase-2 detector (very much a “staged” upgrade program !).
- NSW (New Small Wheel, CERN-LHCC-2013-006):
  - These wheels are the innermost (closest to IP) stations of the “muon endcap”, located between the endcap calorimeter and the endcap toroid. The NSW will provide improved pointing to origin => reject more fake muons and control the rates at high L.
  - Replaces the current Small Wheel with an improved version based on newer chamber technologies (sTGC and Micromegas chambers) which are capable of operation throughout phase-2 (sTGC strips ~3mm pitch, MM strips ~0.5mm pitch). Use both sTGC and MM in L1 trig.
  - The readout and trigger electronics are all designed to be “phase-2 compliant”, so do not anticipate any changes in on-detector electronics during LS-3. Pre-production “late Summer”.
  - Preparing “Module-0” pre-production for sTGC and MM sites in the coming months. Series production should begin in most sites early next year.
  - Installation of NSW represents the first new phase-2 detector system !
- FTK (Fast Tracker Trigger, CERN-LHCC-2013-007):
  - Performs very fast pattern recognition and track fitting on ID data being transmitted to the HLT processor farm. Output is complete list of tracks above PT ~ 1 GeV.
  - Pattern recognition based on associative memories, 8K custom 65nm chips provide one billion patterns to match with IBL, Pixel, and SCT data (8 layers into pattern recognition, 12 layers total for fitting). Production chip submission in next few weeks.
  - First slice based on pre-production AM chips will be operational in ATLAS this year, will phase in complete system during 2016, starting with full barrel coverage for moderate μ values.
  - FTK designs (to be based on still smaller feature size AM chips) will form critical ingredients of L1Track hardware trigger and FTK++ track reconstruction engine for phase-2 HLT.

Brief Overview of Phase-1 Upgrades

- LAr Phase-1 Upgrade (CERN-LHCC-2013-017):
  - Maintain low thresholds and high efficiency for L1 triggers on electrons, photons, and jets at higher luminosities of Run 3 by introducing more segmentation into trigger data.
  - Improved segmentation: trigger tower ($\Delta\phi x\Delta\eta$ = 0.1 x 0.1) -> 10 supercells (4 depth segments, first and last $\Delta\phi x\Delta\eta$ = 0.1 x 0.1, two middle $\Delta\phi x\Delta\eta$ = 0.1 x 0.025)
  - New supercell information is digitized on-detector by new digitizer boards (LTDB), and sent over high-speed optical fibers to the upgraded phase-1 L1 calorimeter trigger.
  - This upgrade to Run 3 L1Calo will allow it to operate as Run 4 L0Calo (see later slide for explanation of two-stage hardware trigger architecture for phase-2).
- TDAQ Phase-1 Upgrade (CERN-LHCC-2013-018):
  - Major ingredients are upgrades of L1Calo (also phase-2) and L1Muon (phase-1 only).
  - The L1Calo upgrade will use improved segmentation supercell data, and implement three “Feature Extractors” (FEX’s) which will process the supercell data. The eFEX will identify electrons and photons, the jFEX will identify standard jets, and the gFEX will perform global calculations such as MET, HT, and large-R jet reconstruction.
  - Some elements of this upgrade package have already been at least partially installed in LS-1 (L1Topo, new CTP, Tile-muon trigger).
  - New phase-1 detectors (L1Calo, NSW) use phase-2 compliant DAQ based on FELIX interface, implementing a heterogenous switching fabric (DAQ, Ctrl/Cfg, TTC, DCS).
- AFP (Forward Proton Detector, CERN-LHCC-2015-009) TDR submitted to LHCC

Accelerator Goals for phase-2/HL-LHC

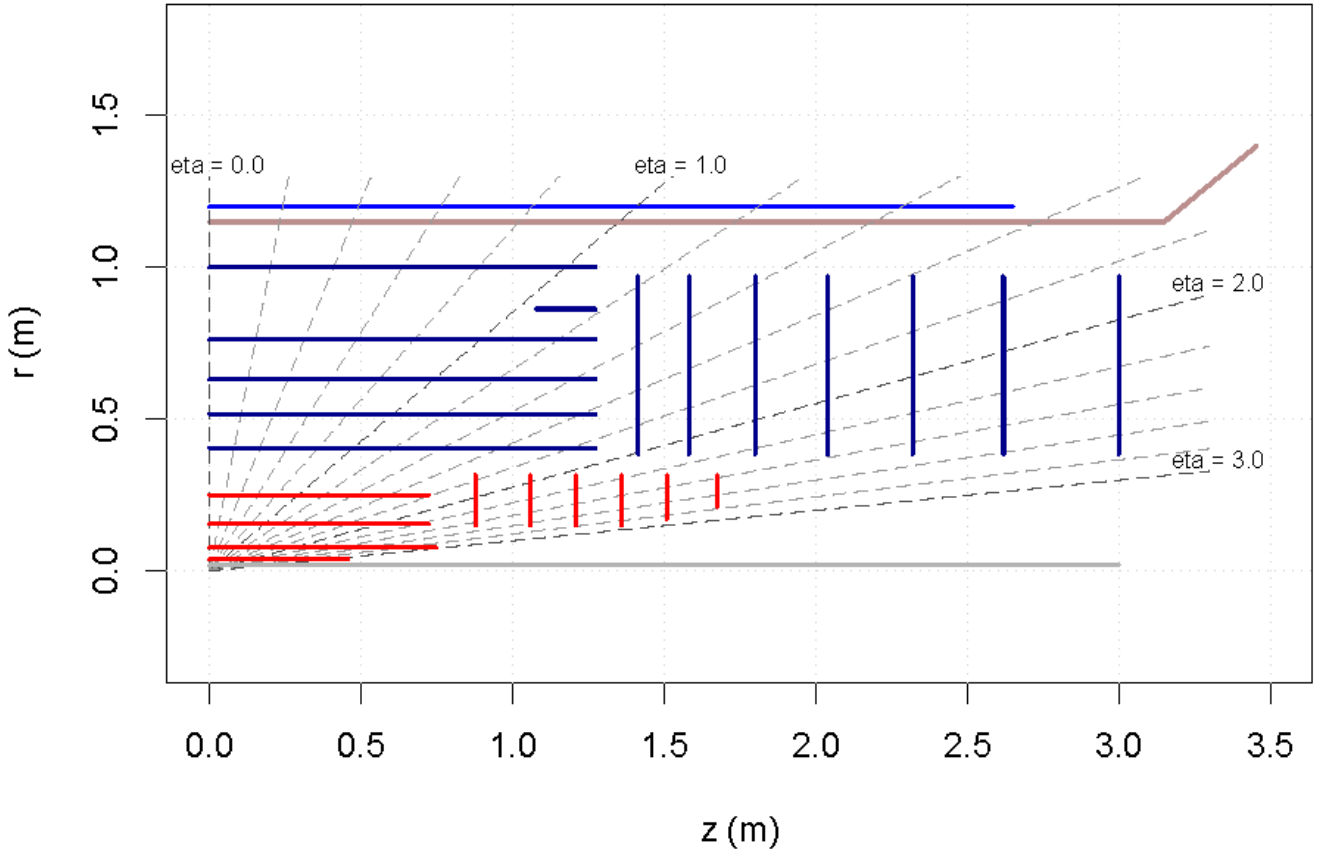
- Nominal goal stated as 250 fb^{-1}/yr delivered lumi, at $5x10^{34}$ luminosity-leveled (nominal operation year gives 160 days of high-intensity pp operation). This served as the basis for the ATLAS Phase-2 LoI design (μ=140). In a 10-year period, with roughly 8 years of operation, this would give delivered luminosity of 2000 fb^{-1} for phase-2, to be added to nominal 300 fb^{-1} up to 2023.
- More recently, ultimate luminosity configuration defined, which provides $7.5x10^{34}$ luminosity-leveled. Due to shorter luminosity lifetime caused by burn-off, would deliver 300 - 350 fb^{-1}/yr, which would bring total delivered in 10 years to roughly 3000 fb^{-1}, with the higher pileup conditions of μ=200.
- Current “reference design” for ATLAS phase-2 upgrade is optimized for ultimate luminosity conditions, in order to take full advantage of whatever the accelerator can produce (so far, LHC has always exceeded our luminosity expectations !)

Brief Summary of LoI Phase-2 Detector

- Defined in official (CERN-LHCC-2012-022) document from Dec 2012. Design was optimized for luminosity-leveled $5x10^{34}$ or μ=140 (some results at μ=200).
- Nominal cost was 230 MCHF, with an improved version (including a fifth pixel layer and a new FCal, plus other modest improvements) costed at 275 MCHF.
- Dominant cost item was new tracker, ITk, with nominal cost of 131.5 MCHF. Major upgrades to TDAQ (23.3 MCHF), major upgrades of LAr electronics based on streaming of all data off-detector with 40/80 MHz digitization rate (32.1 MCHF), major upgrades of TileCal electronics (7.5 MCHF), and major upgrades of muon electronics (19.6 MCHF). A common fund of 16.3 MCHF also included.
- Trigger architecture implements two hardware trigger levels (L0, L1), where the L0Calo is essentially the phase-1 L1Calo, and the L0Muon is an improved version of phase-1 L1Muon. L0 rate was > 500 kHz, and L1 rate into HLT was 200 kHz. At L1, one critical element is an FTK-like trigger L1Track, which in combination with the L0 triggers feeds into L1Global (L1Muon and L1Calo).
- Replace all LAr FE and BE electronics, replace all TileCal on-detector and off-detector electronics, replace “most” on-chamber muon electronics and provide support for MDT in L0Muon trigger, move muon trigger electronics off-detector.

LoI ITk Layout

- Pixel system in ITk layout has 4 barrel layers and 6 disks (~8 m^2). Strip system has 5 barrel layers (and 1 stub layer) plus 7 disks (~190 m^2). Provides at least 14 hits over full eta range, counting strip layer as 2 hits, pixel layer as 1 hit.

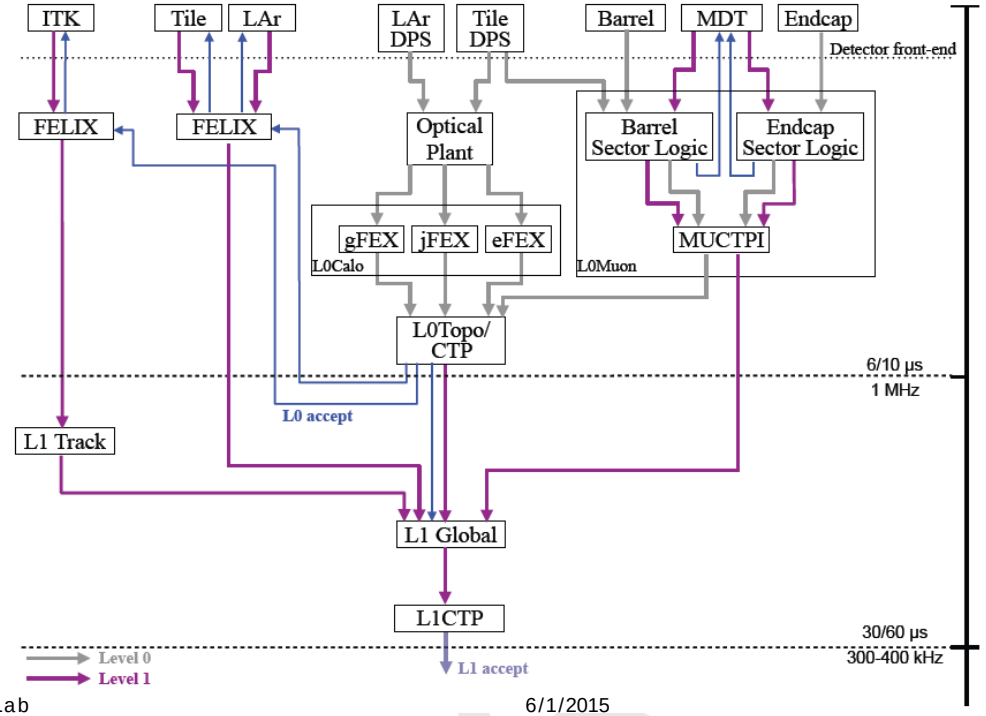


Developed List of Post-LoI Options for Evaluation

- Start from LoI ITk layout for reference design, constrained by need to be able to carry out performance simulations without long development. New Layout TF now working.
- Add large-η extensions to ITk, Pixels only, extending to η=3.2 or η=4.0 (maximum).
- Add sFCal with improved high-lumi performance and finer segmentation (improve both ϕ and η segmentation by factor 2 by reduced ganging of readout electrodes).
- Consider adding finely segmented W/Si thin calorimeter with precision timing to cover region $2.4 < \eta < 4.0$ for improved vertexing and e/γ performance (MBTS region).
- Add BI RPC+sMDT upgrade (cf. BIS78) plus updated MDT electronics for hardware triggering (replace existing on-chamber electronics where possible – everywhere ?).
- Add segment-tagging muon station in front of NSW ($2.6 < \eta < 4.0$) to match extended ITk η coverage – extension of NSW at smaller radius in same shielding structure.
- Add more powerful L1Track (uses ITk data in L0 ROI) and FTK++ (event filter track processor) AM track processors to handle more patterns per second (higher μ, lower track PT, more input layers, larger η coverage, higher rates to match new L0/L1 rates).
- Consider adding Forward detector upgrades if compelling concepts emerge (current forward detectors are ALFA/AFP, LUCID, ZDC – consider accelerator issues too).
- Some of these options are well-defined with clear advantages, some of them are at a more conceptual stage with less developed performance/physics cases. Converge as rapidly as possible, generally in 6-12 months maximum.

Trigger and DAQ Architecture

- Based on split L0/L1 architecture. L0 latency similar (6μs) to that of current L1 latency => similar approaches. L0 trigger based on phase-1 L1Calo with FEX architecture, and new L0Muon trigger (see muon system slides).
- L1 latency significantly longer (30μs) => introduce L1Track AM-based track finder (PT~2-4 GeV), driven by L0 ROIs (no L0 tracking trigger), and L1Calo based on L0 ROIs and full calorimeter data. Allows track/calo matches for e/μ/τ/jets, keep thresholds low, include modest pileup suppression.



Note: L1 Global needs to provide capability for processing roughly 40 events in parallel.

Trigger and DAQ Architecture

- FTK++ AM track reconstruction engine => target 100 kHz reconstruction of all tracks with PT > 1 GeV (mostly focused on hadronic triggers).
- **Note:** both L1Track and FTK++ plan to use next-generation AM chip using 28nm TSMC process => lower power, factor 4 in density (512K patterns/chip). Activity ramps up once AM06 for phase-1 in production. Most components in common.
- HLT processing farm specified for max output rate of 10 kHz.
- Updated readout architecture for phase-2:
  - Transition started in phase-1 TDAQ upgrade, with introduction of FELIX => move away from point-to-point architecture used in Run 1/Run 2 towards network-based dynamically-configured approach which provides greater scalability and reduced need for custom solutions in the DAQ system.
  - Many details to be worked out in definition of FE/TDAQ interface, including full protocol for L0/L1 trigger architecture, efficient implementation of calibration procedures, interactions between ITk and L1 trigger processors, etc. Task force now working on these issues.
  - Significant prototyping effort underway in 2015 in the context of phase-1 DAQ. Will naturally lead towards more mature starting designs for phase-2.
- Generally speaking: phase-1 activities in TDAQ (FELIX), LAr (L1Calo FEX), and Muons (NSW, BIS78) are already implementing phase-1 as a “prototype” of phase-2, or in some cases, are implementing “phase-2 compliant” designs.

Development of Prototype Phase-2 Trigger Menus

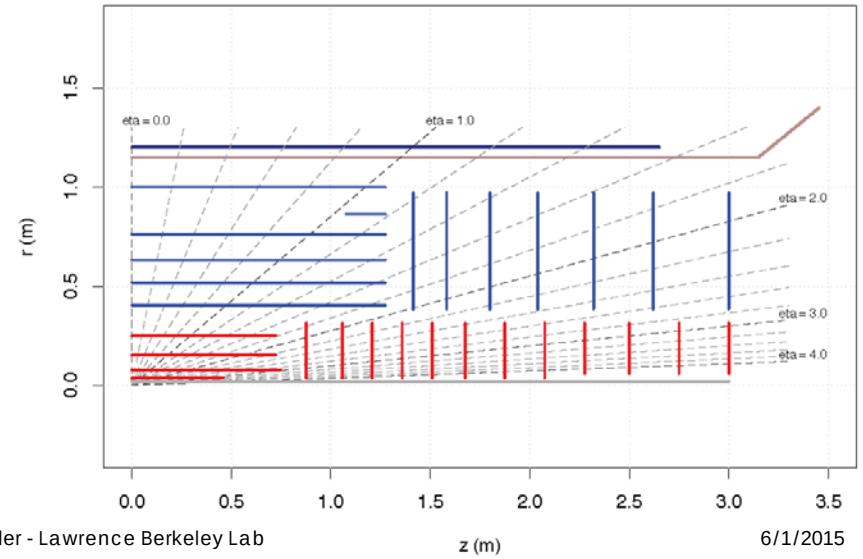
- Now have relatively detailed models for basic ingredients of phase-2 triggers at L0 and L1, just put this together into prototype trigger menus (collection of specific triggers, with thresholds and requirements), and predict rates.
- Provides a powerful metric of the performance of the TDAQ system, and is an important component of the Scoping process.
- Expectations for L1 rejection achievable: factor of 5 for single electrons and di-leptons including di-tau (L1Track and L1Calo), factor of 2 for photons, di-photons (L1Calo), and factor of 2 for jets (L1Track and L1Calo).

Trigger	L0 Rate	L1 Rate
Single Lepton	330 kHz	110 kHz
Multi-lepton	175 kHz	30k Hz
Taus	250 kHz	50 kHz
Hadronic triggers	190kHz	100 kHz
Others (exotics, VBF, etc.)	50 kHz	50 kHz
Total	**995 kHz**	**340 kHz**

Results of initial $7x10^{34}$ menu prepared for ECFA 2014, with approx. rates expected.

ITk Layout

- Substantial work on different layout structures at mechanics level => minimize material, and explore different approaches to layout for endcap/forward regions.
- Layout TF set up to revisit requirements for tracker, survey available layouts, converge towards a final layout early 2016.
- New fast-simulation packages and streamlined geometry creation allow more rapid evaluations and comparative studies => fairly rapid progress.
- Particular challenge is finding effective ways to extend pixel tracker out to η=4.0 (maximum possible in ATLAS tracker volume) for evaluation - material and services are critical to avoid increases in neutron fluences and degradation of calorimeter performance. Need realistic geometry !

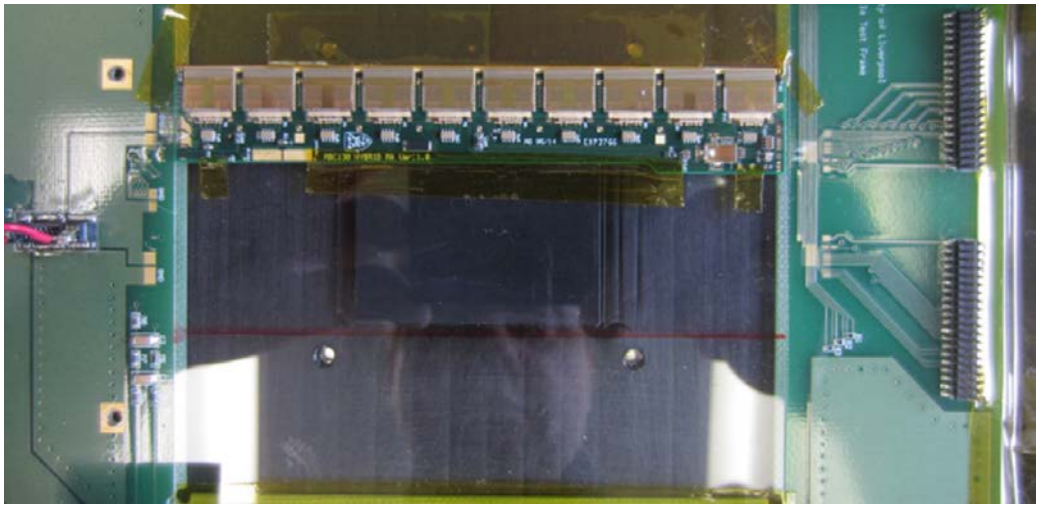


Initial simulation studies based on idealized layout in very forward region using pixel disks extending to η=4.0

More realistic layouts now being optimized – large-η tracking not ideal in "short" solenoid. At η=4, field ~1T, track length ~10cm, potential for large material build-up, very different from η<2.5 tracking of ATLAS today…

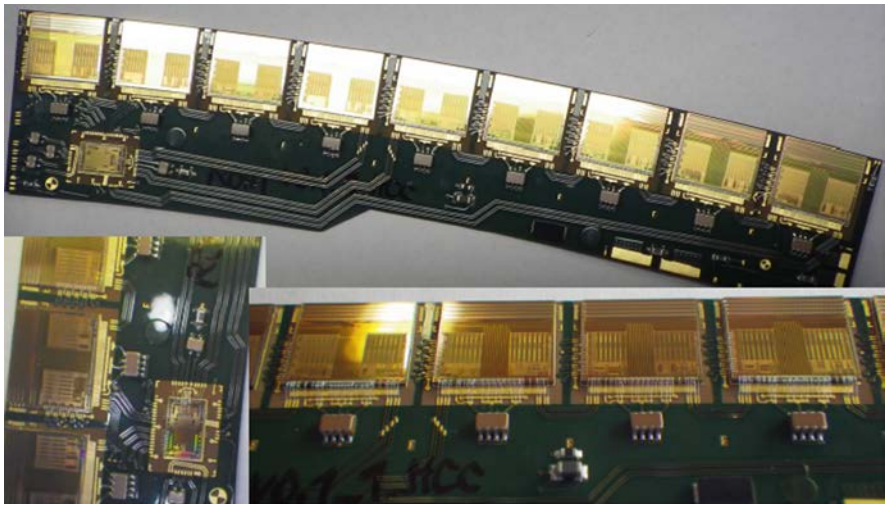
ITk Strips Recent Progress: Electronics and Modules

- Strip activities at high level of maturity: after investment in ABC130 FE chip (256 channels in IBM 130nm process) and realistic prototype sensors => modules !



Complete module with 10 ABC130 chips on hybrid (2560 ch), with HCC controller chip, and short-strip (24mm) sensor.

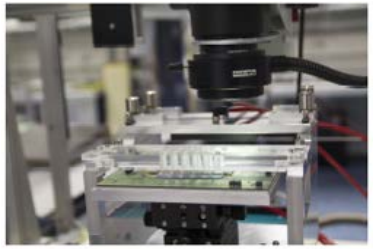
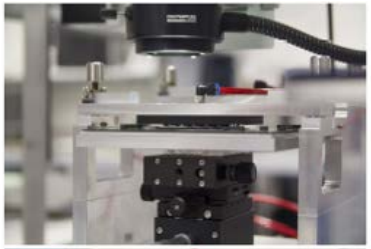
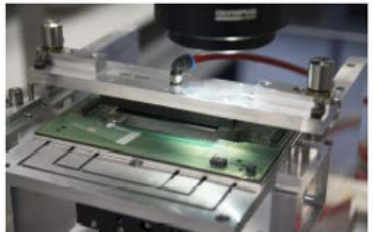
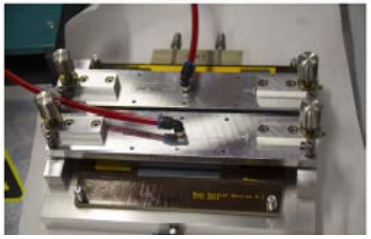
Expect to carry out chip and module irradiations later this year at SPS.



Complete endcap hybrid with ABC130 FE chips and HCC controller chip.

ITk Strips Recent Progress: Modules and Structures

- Sophisticated tooling already being developed for module construction, and local support loading.


Module assembly tooling developed on dummy modules, being used now for prototype modules.

Module placement setup developed for loading barrel half-staves (13 modules).

Sophisticated stave prototypes already include co-cured electrical bus and integrated cooling.

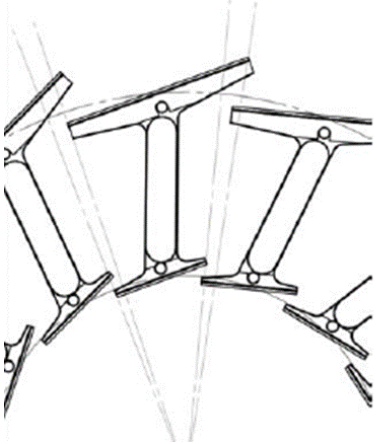
ITk Pixels Recent Progress: Electronics and Modules

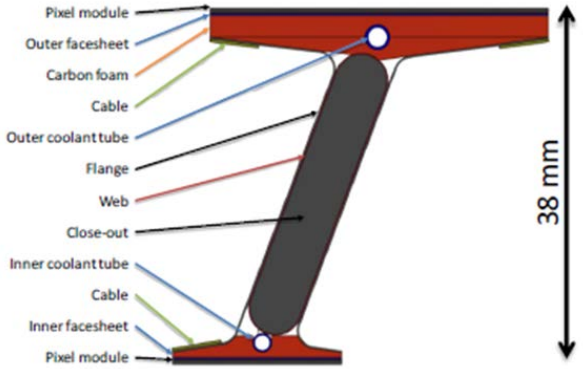
- Starting point for evaluation of modules uses FE-I4 chip produced for IBL:
  - Chip implemented in IBM 130nm, qualified to 250 Mrad for IBL application.
  - Contains 80 columns of 250μ long pixels, with 336 rows of 50μ width pixels (total of 26880 pixels) in a die of size of roughly 19mm x 20mm. It includes internal regulators to power the circuitry, and uses a regional readout logic architecture with a 4-bit TOT measurement.
  - Specifications are close enough to allow realistic prototyping and operation of modules and larger assemblies, while FE-65 chip, to be built in TSMC 65nm process with 50x50μ pixels, is under development. Substantial software and hardware development available for lab and testbeam studies, etc.
- Expect initial demonstrator prototype from RD53 (so-called RD53A chip) to be submitted in 2016 – multiple analog FE designs, minimal overall integration - many details and features remain to be worked out…

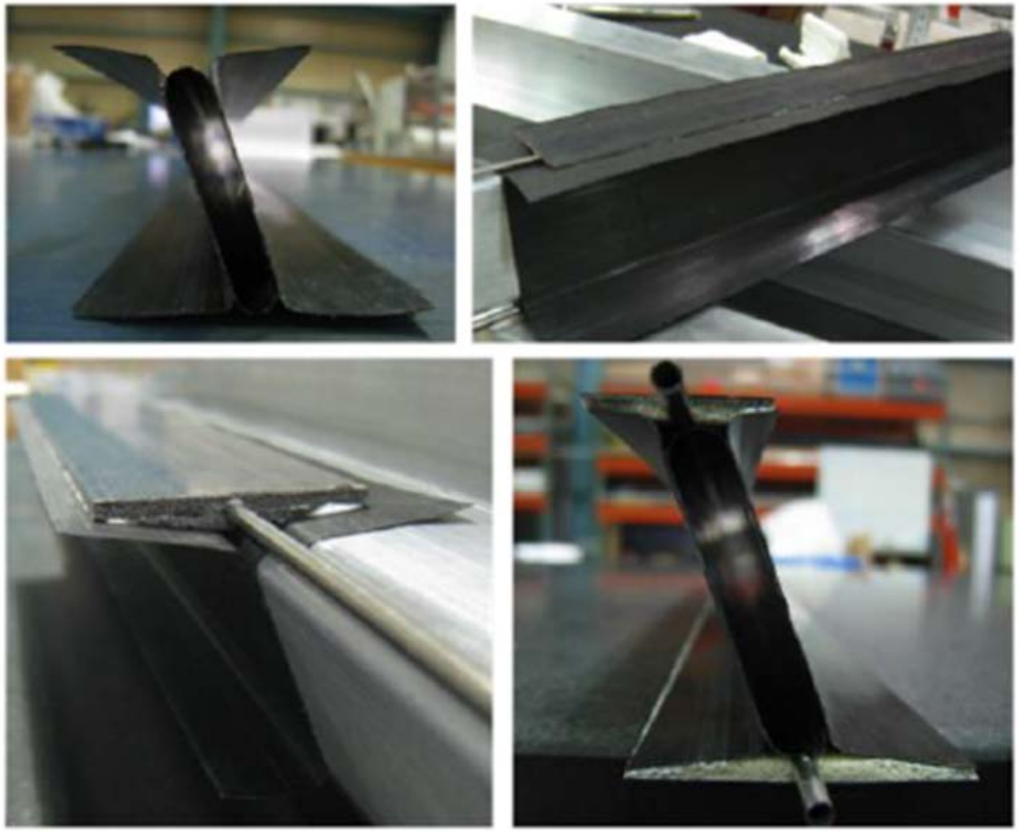
Prototype Quad Modules (basic building block of phase-2 Pixel layout) using FE-I4 chips and prototype CIS n-in-p sensors.

ITk Pixels Recent Progress: Local Supports

- Significant development taking place on several different local support concepts for the barrel and for the forward/endcap region.
- One example of extremely low-mass structure for the two innermost layers ($R_2 = 2R_1$ => 1 quad inside, 2 quads outside) is I-beam structure with thin CF skin bonded to thermal foam with embedded cooling pipes, integrated services:







ITk HV/HR-CMOS R&D Program

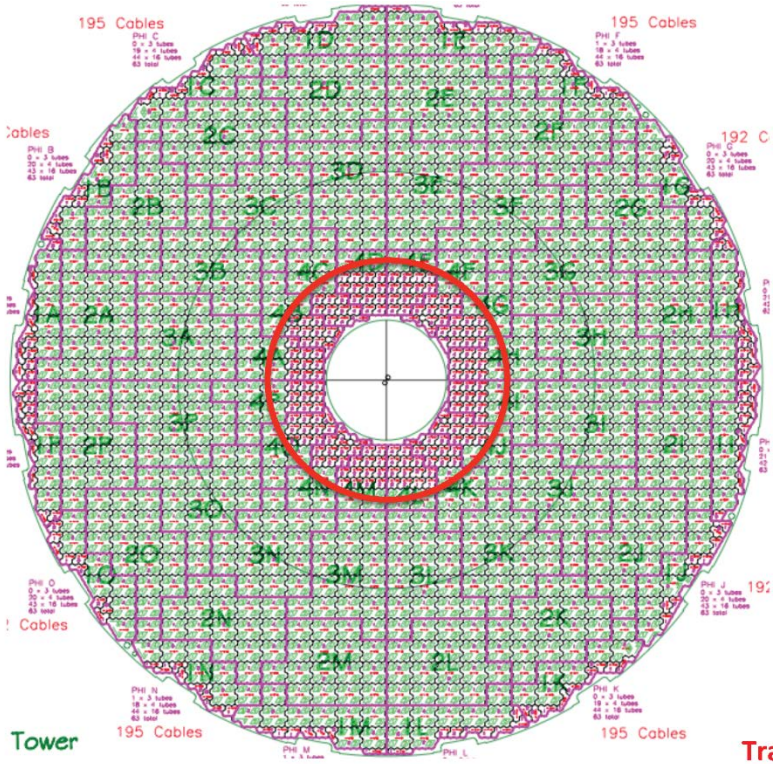
- Commercial processes offer potential of cheaper “smart” sensors with some (or almost all) FE functionality embedded. Volume production on large wafer sizes.
- Sensors with embedded gain could reduce interconnect requirements (AC ok – low Ω DC not needed) for Pixels. Can provide thinner sensors to reduce cluster size and/or pitch. Need to demonstrate required radiation tolerance.
- Strips:
  - Little time for development left, must instrument ~100-200 m^2 => must be low risk replacement on early timescale, otherwise conventional procurements need to start.
  - Large potential savings from single sensor for 2D information – fewer bonds, less material. Need to demonstrate module functionality by end 2015.
- Pixels:
  - Ideal candidate for larger radius layers (lower doses, large areas to cover).
  - For initial R&D, should be compatible with readout by current FE chips (e.g. FE-I4), bumped or glued, have low power/pixel and high efficiency after irradiation to O(10^{15}) NIEL or 50 MRad TID.
  - Build single-chip modules with FE-I4 by end 2015, evaluate in testbeam.
  - Multiple samples in hand, encouraging results, working with several vendors. Expect to review results by early 2016, define remaining R&D program.

LAr Phase-2 Upgrades

- Need to replace:
  - LAr front-end electronics (on-detector) and related on-detector powering
  - LAr back-end electronics (off-detector)
- LAr front-end electronics:
  - Move to a digital 40/80 MHz streaming output which also provides ROI-based finely segmented data to L1Calo in phase-2 (supercell trigger data from phase-1 will be used for L0Calo in phase-2). Allows higher performance transforms to be used off-detector to extract maximum information for each event.
  - ASIC development underway for pre-amp/shaper, and digitization. Optimize read-out for high pile-up conditions in phase-2, with multiple designs. Prototype unipolar shaper and multi-gain digitization system in 65-180 nm – submission planned for late 2015. Several ADC schemes being investigated in 65nm as well. Aim to complete prototyping and evaluation by end-2016.
  - Plan to use lpGBT for data transmission
  - New on-detector powering concepts, most likely rad-tolerant DC/DC convertors, under investigation.
- Back-end electronics design will follow front-end design. Expect to arrive at a unique proposal for both for TDR in mid-2017.

Proposed sFCal Upgrade

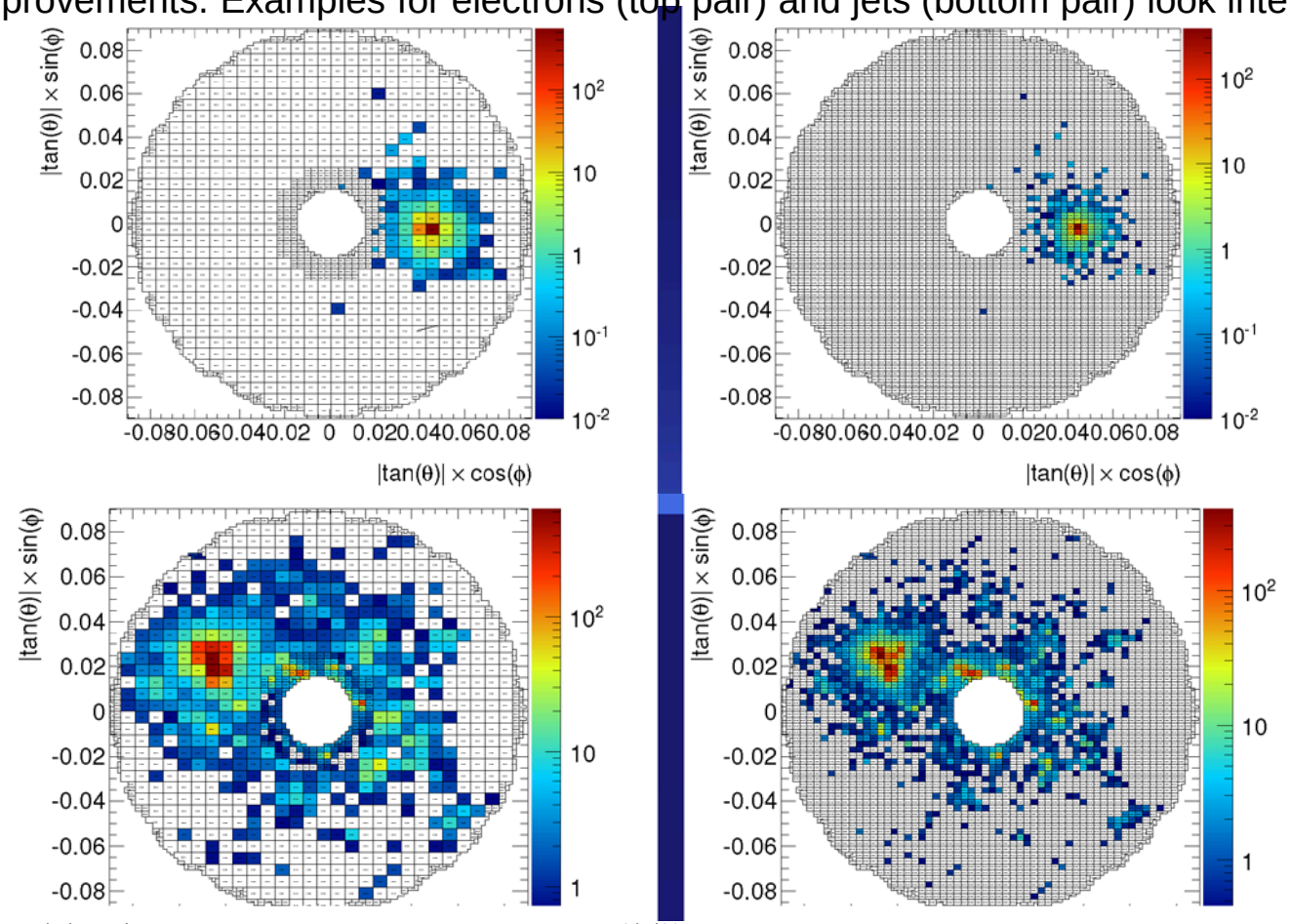
- Present FCal based on Cartesian array of electrodes (e.g. 12260 in FCal1 layer), parallel to beam, with ~250μ drift gap. Phase-2 issues for instantaneous luminosity include ion build-up, HV distribution with present series resistor values, and LAr cooling – currently large R only - heat transfer from FCal may not be high enough
- Propose reduced LAr gap of ~100μ, improved HV distribution, local cooling loops to eliminate concerns with instantaneous luminosity (studies still underway to assess impact if these improvements not done – LAr boiling is principal risk…)



Improved sFCal Segmentation

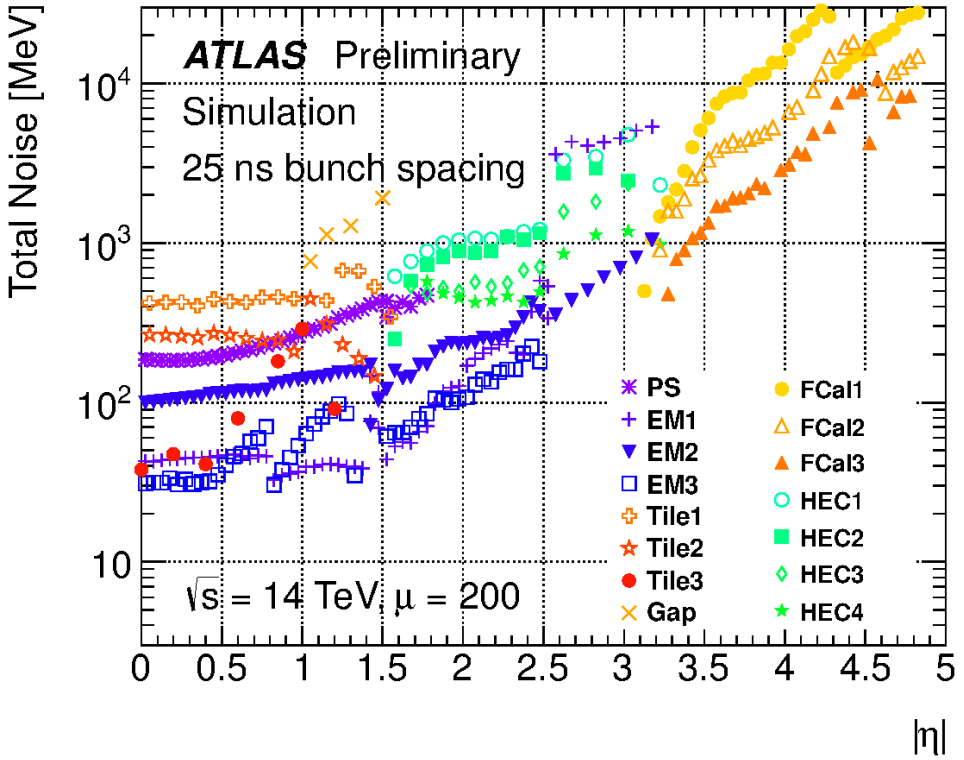
- Presently 2x2 summing done inside each FCal module and additional 2x2 summing done on back of HEC. Explore impact of removing one layer of summing => segmentation finer by factor 2 in both directions.

- Full simulation geometry model now working, simulations underway to assess impact of improvements. Examples for electrons (top pair) and jets (bottom pair) look interesting !



Noise (Electronics + Pileup) in Forward Region

- Simulated noise in the LAr calorimeters has been calculated, adding electronic and pileup noise in quadrature. The pileup simulation takes into account the sensitive time of the LAr readout and the bunch-train structure. The results below are for 25ns bunch spacing and the ultimate HL-LHC luminosity μ = 200.
- Results are shown here for each layer, as a function of η, with the noise in GeV (to be compared to deposited energy NOT ET).



Note the dramatic rise in the region above η=2.5 (the region between 2.5 and 3.2 is driven by coarse segmentation). Relevant for 4D detector in following slides.

In the FCal region, note the significant reduction above η=4.3, which is where the summing reduces to 2x2 electrodes in FCal1 instead of 4x4 electrodes.

The rapid increase for η>3.2 will be reduced by a factor 4 with previous FCal segmentation change.

sFCal Decision Process

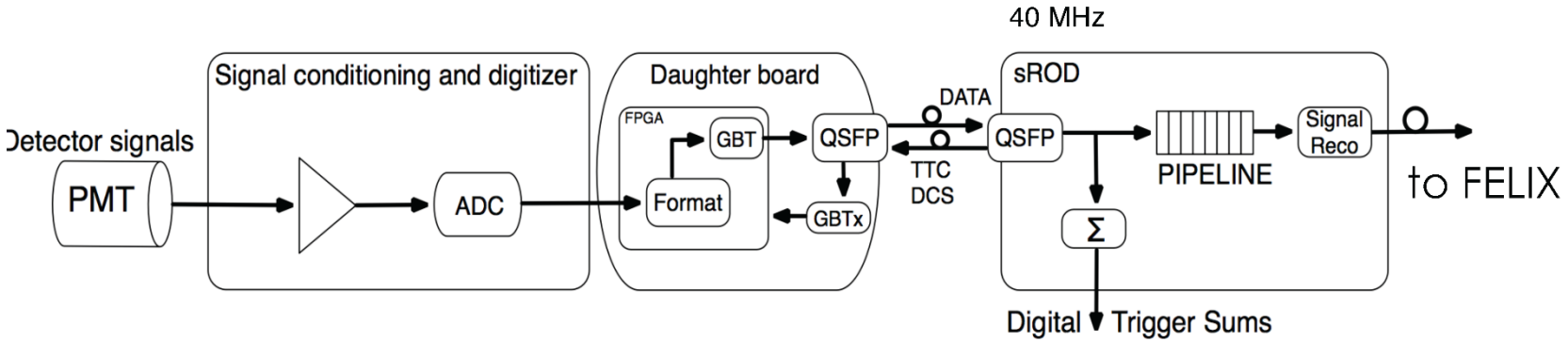
- Replacement of sFCal is a very complex process. Need to open both warm and cold walls of Endcap Cryostat at small radius. Very comprehensive risk analysis, since cryostat is shared with EMEC and HEC endcap calorimeters, area will be intensely activated (therefore, concluded that replacement FCal needed even if only the segmentation change would be made). Done in UX15 cavern => significant impact on LS-3 logistics for major activities foreseen in ID/ITk system and Muon system => beginning planning process for LS-3 activities to assess.
- Risk analysis underway – combination of challenges needs careful consideration !
- If we do not control the material in the ITk, particularly for a very-forward extension, the impact of sFCal improvements might be substantially reduced !
- Expect to reach a decision roughly mid-2016, as an extended prototyping program will be required to assure the performance of the sFCal.
- The region covered by the current FCal ($3.2 < \eta < 4.9$) is extremely important given the role of VBF processes in SM VBF/VBS studies, Higgs coupling studies (VBF production has lowest theory uncertainties !), and also for “natural” SUSY models where VBF production can be important for EWKino production. Also critical for lepton reconstruction in this region (very challenging in phase-2 !)

Consider “4D” Segmented Timing Detector

- Extension of tracking coverage to beyond η=2.5 exposes scoping decisions made for initial detector, where calorimeter segmentation in EMEC, HEC, and FCal was reduced to save cost in regions where no precision reconstruction of most physics objects was considered useful…
- Forward region suffers from very high pileup in phase-2, and is the only region where timing information could be used to associate (somewhat probabilistically) energy depositions with vertex positions.
- In ATLAS, there is a thin region on front of the ECC which has been occupied by a thin layer of scintillators (so-called MBTS = MinBias Trigger Scintillators), recently refurbished during LS-1 for use in Soft QCD and related HI measurements. Easily accessible during YETS => flexible installation scenarios even after LS-3.
- Consider option of a “thin” (O(5cm)) layer in the region $2.4 < \eta < 4.0$ to provide additional information in this complex region. Consider W/Si (or Cu/Si to reduce neutrons) to provide maximum information. Recover some missing segmentation for electron/photon/jet reconstruction, add high-precision timing (O(50ps)) to also provide vertex-tagging capability.
- Note standard Gaussian beam collision scheme (even with crab-crossing) results in poor correlation between z and t (Run 1 at given z position, have σ(t)~200ps). However, crab-kissing scheme offers opportunity to stretch z distribution of collisions while compressing t distribution, since bunch head collides with bunch tail. This makes a “4D” detector potentially interesting => investigate.
- Interesting work underway on LGAD (low-gain avalanche detectors) => evaluate !

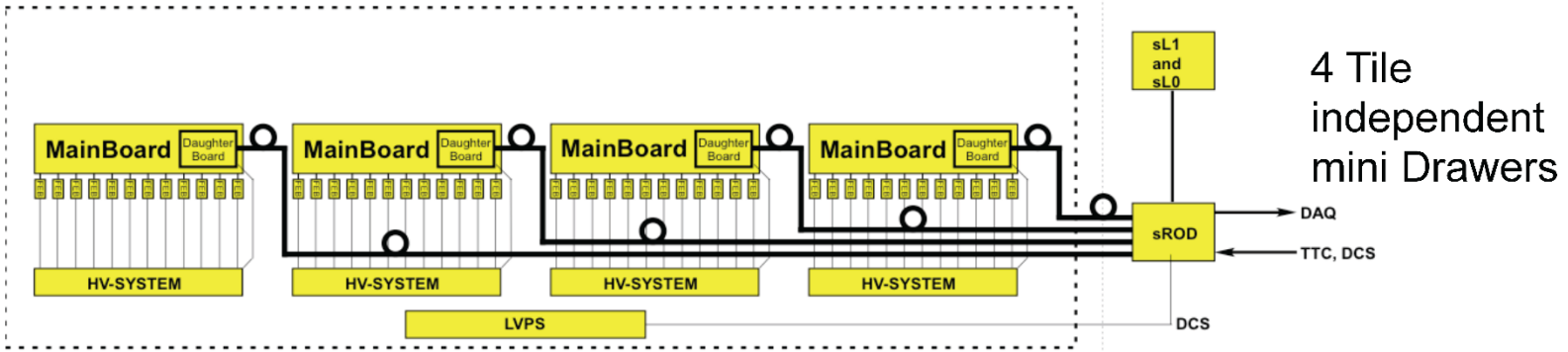
TileCal Phase-2 Upgrades

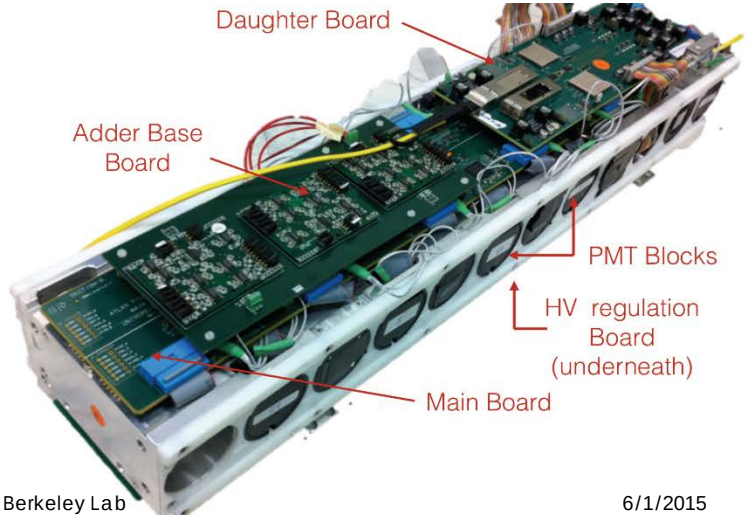
- Need to replace current front-end electronics with new signal conditioning and digitization capable of continuous operation at 40 MHz to provide low-latency inputs to L0Calo trigger and DAQ system. Stream data at 40 MHz off-detector, as for new LAr front-end electronics.
- Transmit all of this information off-detector using GBT links, and new back-end electronics contains pipelines, derandomizers, and initial summing for trigger.
- Presently three different approaches to front-end implementation being prototyped and assessed in detail – choice will be made before TDR in 2017.
- Also two approaches to HV distribution being evaluated, one with internal regulation as in current system, and one with remote regulation (supplies are always remote).



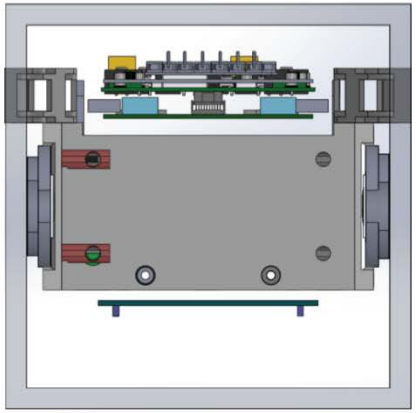
TileCal Phase-2 Upgrades

- Update system modularity at both electrical and mechanical level, improve reliability and simplify handling and installation. Based on new “mini-drawer”, four of which replace previous super-drawer. Each mini-drawer reads out 12 PMTs, with internal redundant powering and readout.



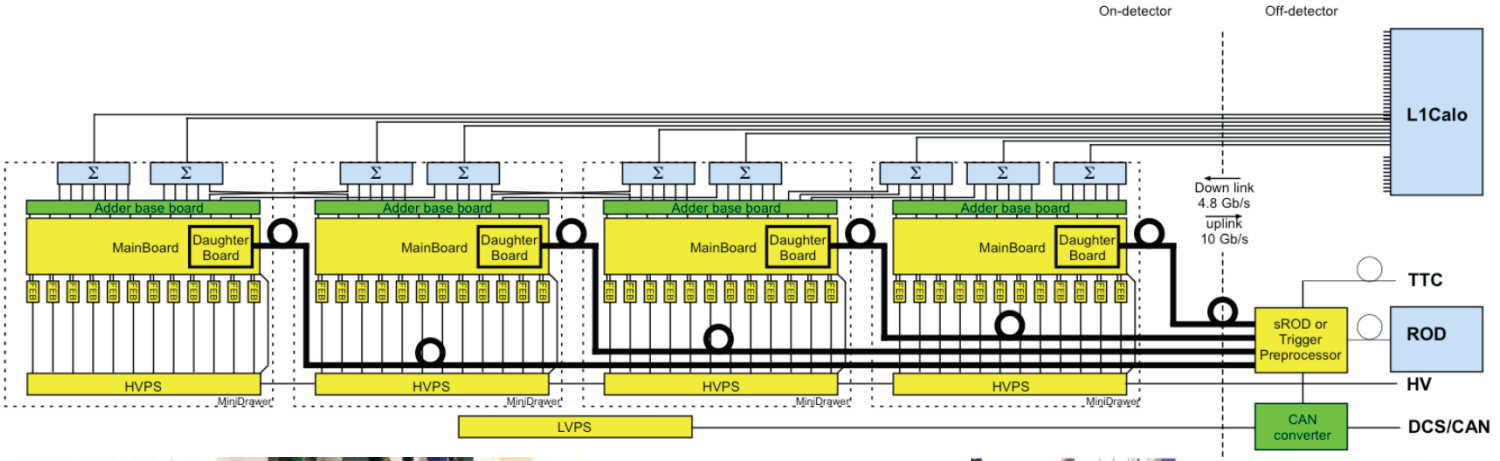


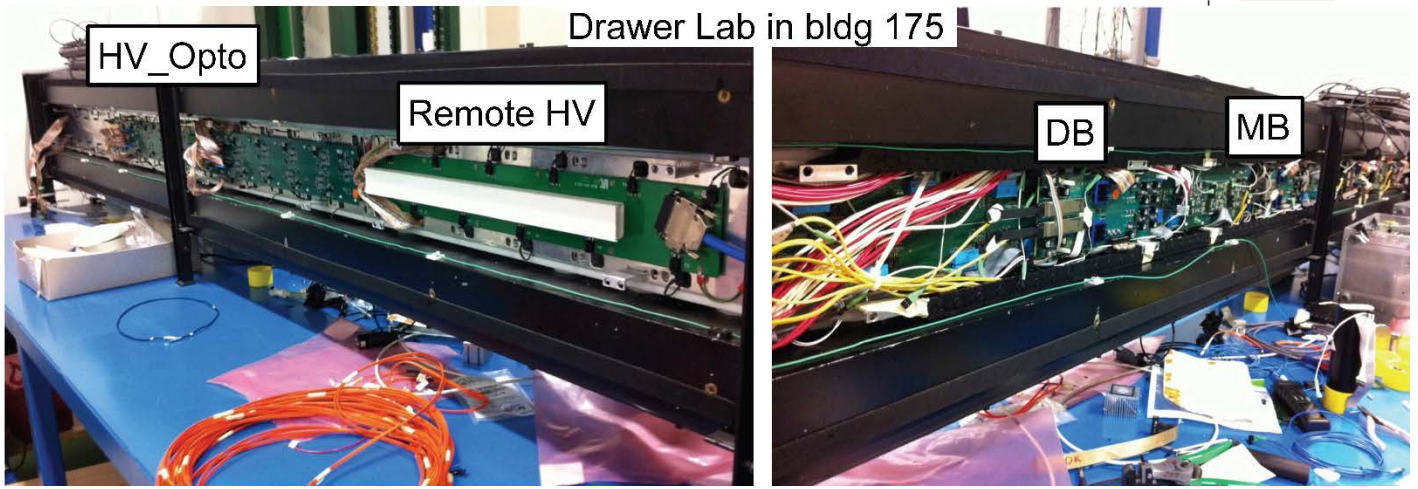
Cross section of a mini-drawer



TileCal Phase-2 Upgrades

- Community has built a Demonstrator prototype using 4 prototype mini-drawers, and with “hybrid” interfaces to allow it to be operated within the present TileCal system (should be installed in ATLAS during a YETS). Used for “system test” and “reliability test” of mini-drawers and all of their components:





Muon Phase-2 Upgrades

- Upgrade of MDT readout electronics:
  - Space charge limits for MDT tubes (30mm diam) not reached once NSW is installed.
  - Longer latency implies higher buffer occupancies, but main challenge is higher data transfer rate arising from higher L1 rate and higher buffer occupancy (assuming they are only read out each L1 trigger, so they could not provide L0 trigger input). Potential for data loss beyond L1 of 200 kHz.
  - Ideally, would change all legacy on-chamber electronics for MDTs, but for innermost barrel chambers (BI chambers), this is very challenging.
  - ATLAS TC has prepared a plan for this, but would require 18-24 months, assuming for BI layer that it would be necessary to remove and re-install MDT chambers.
- Upgrade of RPC readout electronics:
  - Possible to replace first digital component of RPC readout electronics, which is accessible on chambers, with new Data Collector and Transmitter box.
  - Then transmit all data in digital form (using GBT links) off-detector to allow performing all trigger processing off-detector using FPGAs rather than the present on-detector rad-tolerant ASICs.
  - Note current chambers will still require reduction of HV in order to remain within safe charge/rate limit for 3000 fb^{-1} lifetime. This will imply that these chambers will operate at a reduced efficiency. Worst locations will have efficiencies as low as 65%.
  - Note that current RPC implementation in the barrel, with 2 BM layers and 1 BL layer, requires a 3/3 coincidence => 71% Run 1 acceptance*efficiency due to “OR of holes”.

Muon Phase-2 Upgrades

- Upgrade of TGC readout electronics:
  - The TGC chambers in the present SW will be replaced by sTGC and MM chambers in the NSW phase-1 upgrade. Also propose to replace TGC's in BW at smallest radius with sTGC as in NSW. Remaining BW TGCs will need new readout electronics. This will also allow displacing all of the trigger electronics off-detector to allow use of FPGAs instead of custom ASICs for this logic.
- Use of MDT information in L0Muon trigger:
  - Maintaining 20 GeV offline muon trigger threshold requires sharpening the trigger turn-on curve, beyond what is available in the current L1 muon trigger.
  - Proposal is to use ROIs defined by trigger chambers (RPC and TGC), in combination with MDT information, to sharpen the trigger thresholds. This is possible if the MDT on-chamber electronics is replaced – MDT data needs to be transmitted in time for L0 decision. It benefits from the displacement of all muon trigger logic off-detector => sophisticated FPGA or FPGA/CPU algorithms possible in L0 latency available for phase-2. Potential for factor 2-4 reduction in L0 rates.

Muon Phase-2 Upgrades

Reference proposal for phase-2 muon upgrade:

- Assume that it is possible to change all of the MDT electronics on the innermost barrel layer of the muon system. This eliminates any artificial limits on the L1 trigger rate and L1 latency arising from the legacy electronics.
- Replacing MDT electronics on all BI chambers, which requires removing the chambers from ATLAS, replacing the electronics, and re-installing them, allows making more significant changes.
- Proposal is to replace the BIS (small, inner) chambers with new chambers built using sMDT (15mm diam tubes), which leaves space to add a triplet of RPCs on the outside of these new chambers. In addition, a triplet of RPCs would be added on the outside of the present BIL chambers (large, outer) => can implement 3/4 coincidence using all three barrel layers and reach acceptance*efficiency in the range 90-95% for barrel muons (+ reduced sensitivity to lower effic of old RPCs). The phase-1 BIS78 project applies this approach to highest-η chambers.
- In addition, consider addition of a muon tagger (for segment-tagged muons, meaning an ITk track linked to a track segment behind the calorimetry in ATLAS) in the region $2.6 < \eta < 4.0$. This would effectively extend the current NSW acceptance to cover the new phase space covered by the very-forward ITk. Have already agreed to provide a region in the JD shielding/support for NSW to allow installing such a layer. Note the ECT field is essentially gone by η=2.7, so unlike NSW/BW, this tagger would not bring any momentum information.

Summary

- ATLAS presented first concept for phase-2 detector upgrade in LoI document dating from 2012.
- In the intervening time, ATLAS has continued to develop and evaluate these initial ideas. In addition, a recent TF has reviewed the very forward region and injected some further ideas into the evolving design.
- The design presented here represents the best snapshot today of the detector upgrades we hope to build for phase-2, and is the reference design for our Scoping Document.
- This design is being evaluated extensively in the context of the Scoping Document exercise – expect more information for the Sept LHCC, including a range of relevant performance and physics studies in the context of this exercise.

Backup Material…

Scoping Scenario Variations

- Variations in ITk configuration:
  - Vary the number of hits available in barrel and disks at large radius (Strips).
  - Vary the very-forward Pixel coverage beyond η=2.7.
- Variations in LAr Upgrade configuration:
  - Build and install sFCal replacement for present FCal.
  - Build and install 4D W/Si finely segmented precision timing detector.
- Variations in Muon Barrel Upgrade configuration:
  - Upgrade full BI layer, including replacing MDT electronics, implementing L0 MDT trigger capability, and implementing BI sMDT+RPC upgrade. Alternatively, implement BI sMDT+RPC on only 50% of the BI layer which is at larger η (easier access), or do not implement any of these changes on BI layer.
- Variations in Muon Endcap Upgrade configuration:
  - Replace MDT electronics and implement MDT L0 trigger on EO (outermost) chambers.
  - Build and install very-forward muon tagger covering $2.7 < \eta < 4.0$ region.
- Variations in TDAQ Upgrade configuration:
  - L1 trigger rate is reduced to 200 kHz from 400 kHz, EF rate is reduced to 5 kHz from 10 kHz.
  - L1Track and FTK++ PT thresholds and η coverage are varied. Rates track the first item.
  - L0Calo, L0Muon, and L1Global (Calo and Muon) track available η coverage.