The Front End Readout Electronics for the Hybrid Avalanche Photo Detector of the Belle II ARICH

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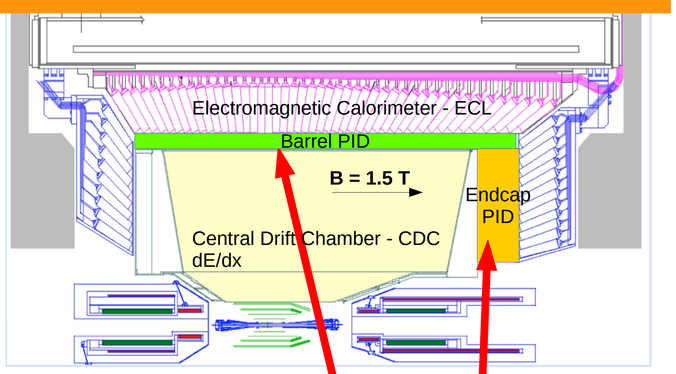
RICH 2016

Particle identification in Belle II



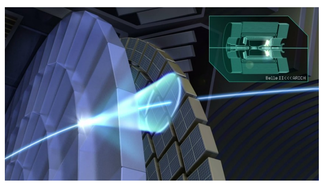
Two dedicated particle ID devices:
both RICHes → designed to fit into available space
- Barrel: **Time-Of-Propagation (TOP)**
- End-cap: **Proximity focusing Aerogel RICH (ARICH)**

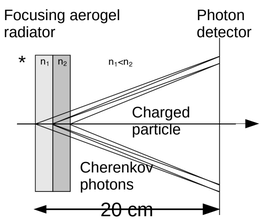
Photo detectors should operate in magnetic field of 1.5T

Proximity focusing Aerogel RICH

Goals and constraints:
- > 4 σ K/π separation @ 1-3.5 GeV/c
- limited available space ~280 mm
- radiation tolerance (n,γ)

Selected type:
proximity focusing aerogel RICH



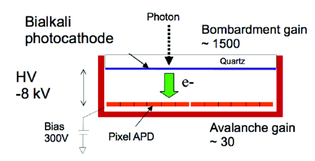


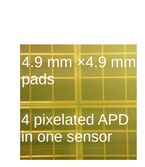
- <n> ~ 1.05
- $\theta_c(\pi) \approx 307$ mrad @ 3.5 GeV/c
- $\theta_c(\pi) - \theta_c(K) = 30$ mrad @ 3.5 GeV/c
  - pion threshold 0.44 GeV/c,
  - kaon threshold 1.54 GeV/c
- neutron fluence: up to ~10^{12} n/cm2
- radiation dose: up to ~1000 Gy

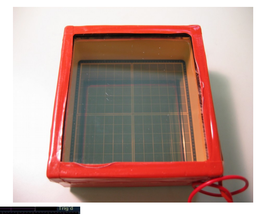
* to increase the number of photons without degrading the resolution

limited space (~5cm) behind the HAPD

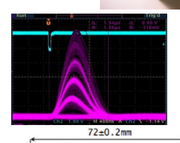
HAPD -Hybrid Avalanche Photo Detector



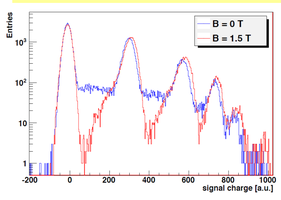




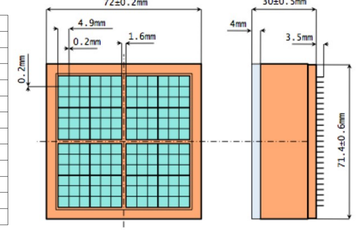
- HAPD developed with Hamamatsu Photonics
- Works in a magnetic field of 1.5T
- Excellent separation of single photoelectrons



Pulse height distribution

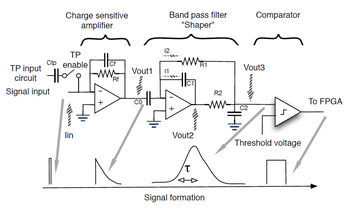


Package size	72 x 72 mm^2
No. of pixels	12 x 12 (6x6/APD chip)
APD bias	about 400V
Avalanche gain	about 50
Pixel size	4.9 x 4.9 mm^2
Effective area	67%
Typical QE	25%
HV	-7kV
Bombardment gain	about 1700
Total gain	about 10^5
Pixel capacitance	80pF
S/N	15
Weight	220g



ASIC chip

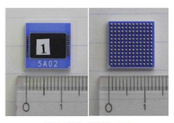
36 channel ASIC developed by KEK :
Consists of preamplifier, shaper and comparator
→ provides hit information
- settings: 4 step gain, 4 step shaping time, offset level
- shaping time >100 ns



SA02 ASIC	
Chip size	6.5 × 3 mm^2
Package size	13 ×13 mm^2
No. of channels:	36
Technology	TMSC 0.35 μm process
Standard input	60000 e$^-$
Gain	20-70 mV/fC
Shaping time	250 - 1000 ns
ADC	1 bit leading edge discriminator
Power supply	± 1.65 V
Power consumption	3.7 mW/ch

ASIC channel and global registers

Register	Name	Function
D[2:0]	DECAY TIME	Decay time of the preamplifier (not-used)
D[6:3]	OFFSET	Coarse offset adjustment
D[10:7]	FINEADJ UNIPOL	Offset adjustment for unipolar comparator
D[14:11]	FINEADJ DIFF	Offset fine adjustment for differential comparator
D[15]	–	reserved
D[16]	TP ENABLE	Test pulse enable (1 = disable, 0 = enable)
D[17]	KILL	Disable channel (1 = disable, 0 = enable)

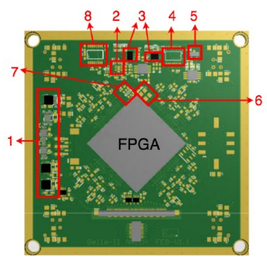


SA02 (36ch)

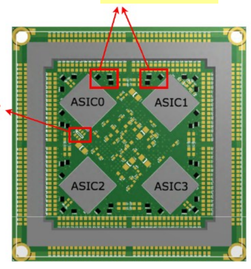
Register	Name	Function
D[1:0]	PHASECMPS	Reverse transfer capacitance for phase compensation
D[3:2]	GAIN	Gain (3=min, 0 = max)
D[5:4]	SHAPINGTIME	Time constant of the shaper (0 = min, 3 = max)
D[6]	COMPARATOR	Selection of the comparator (0 = unipol, 1 = diff)
D[14:7]	VRDRIVE	Output drive
D[16:15]	MONITOR	Select position monitor for analog signal‡
D[25:17]	ID	9 bit chip ID ; read only

Front end board

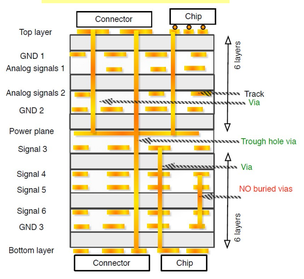
Top side



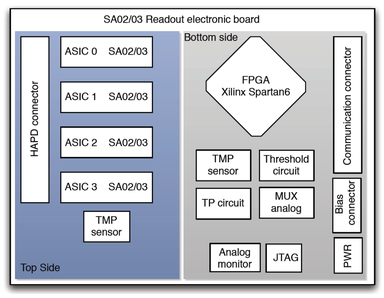
Bottom side



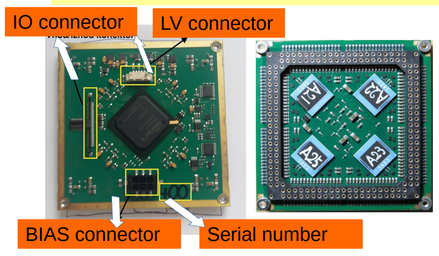
12 layer FR-4 board



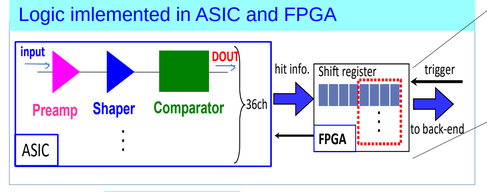
1. LDO-low dropout regulators
2. ADC
3. Analog multiplexer
4. Digital resistor
5. Reference diode
6. Oscillator
7. Temperature sensors
8. Test Pulse generator
9. ESD- electrostatic discharge protection



Front end board with 4 ASICs and Spartan6 FPGA



Logic imlemented in ASIC and FPGA



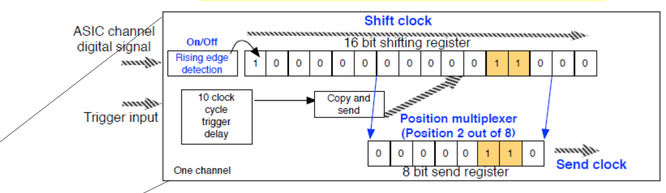
SPI instruction | SPI response | SPI data | trigger | JTAG
IO connector

Spartan-6 XC6SLX45 FPGA

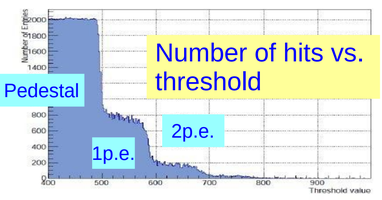
Responsible for
- Hit detection,
- Coarse time-over-threshold measurement to discriminate between single Cherenkov photons from aerogel and the Cherenkov photons produced in the HAPD window
- Communication with the back end
- Monitoring of supply voltages and temperature
- Also implemented in the firmware: SEU controller

Spartan-6 XC6SLX45 FPGA specifications:
Size: 23 mm 23 mm
Number of I/Os: 358
Number of banks: 4
Number of logic cells: 43.661
Max RAM: 401 Kb
Bank power supplies: +1.2 V, +1.5 V, + 2.5 V, +3.3 V

Signal detection and propagation in FPGA

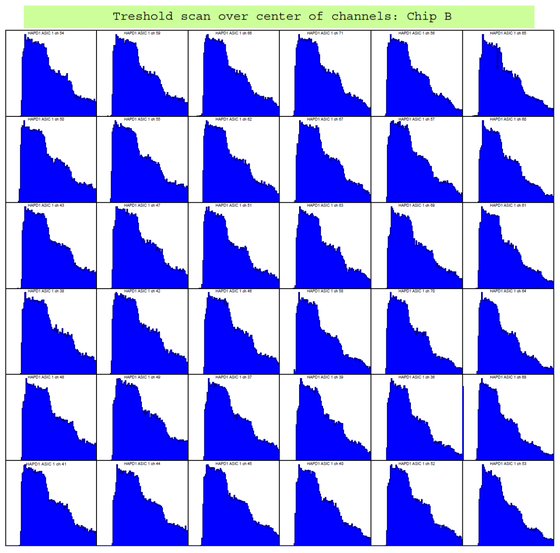


Response to low intensity light



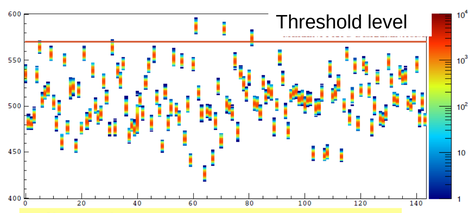
Number of hits vs. threshold

Threshold scan for channel of one of the ASICs:
Response to short laser pulses

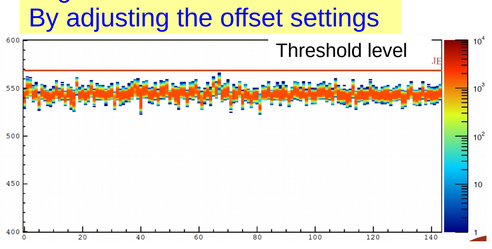


Threshold scan for all channels – non illuminated

Non aligned –
channels have different offsets

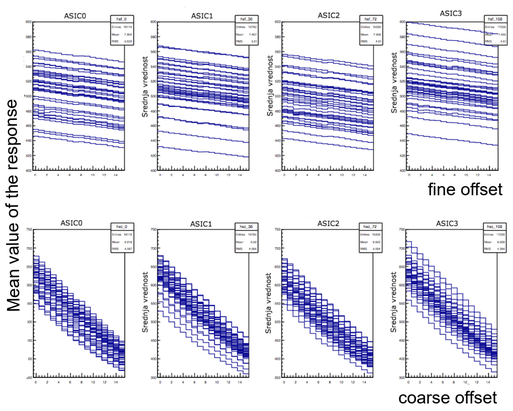


Aligned -
By adjusting the offset settings

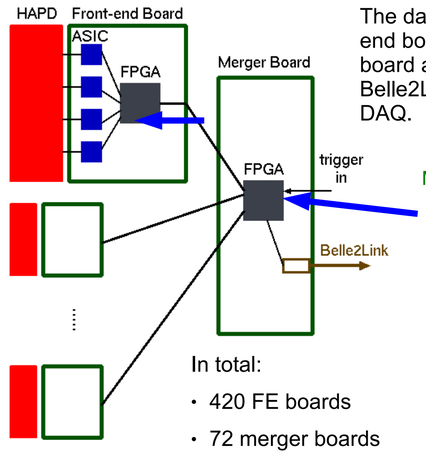


Offset linearity

The offset can be calculated by using a pre measured curve.



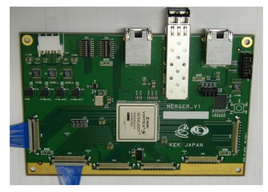
ARICH readout chain



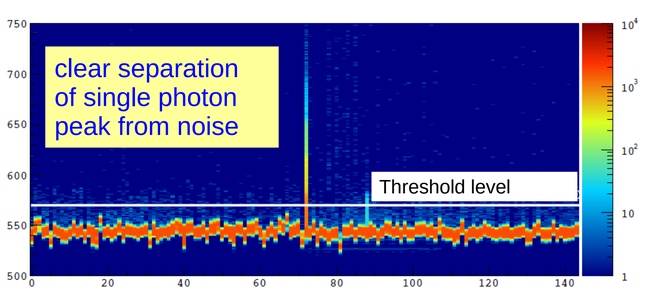
The data coming from up to 6 front end boards are collected by a merger board and send through the optical Belle2Link to the common experiment DAQ.

In total:
- 420 FE boards
- 72 merger boards

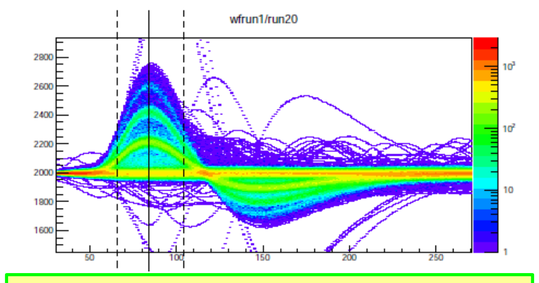
Merger board with Virtex5 FPGA



Threshold scan for all channels
Response to single photons from laser –
one channel is illuminated



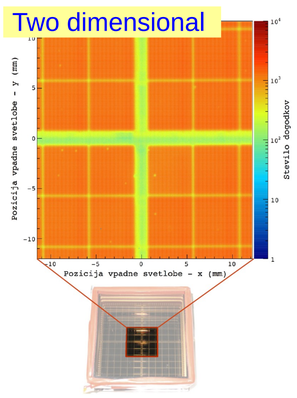
Monitor output of a single selected channel



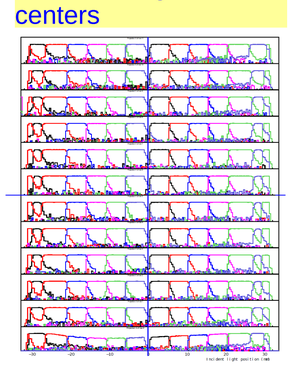
Neutron Irradiation tests

Scan with a laser beam across the HAPD

Two dimensional



Linear through channel centers



The readout board is being tested in the TRIGA nuclear reactor

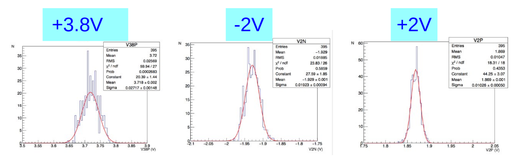
No degradation in operation after 5 Belle II years (5x10^{11} n_{eq}/cm^2)

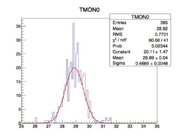
Single events upsets have been observed during the operation in the reactor. The expected rate in the Belle2 environment is manageble:
- Software error mitigation controller will be synthesized in the Xilinx Spartan6 firmware
- In the case of SEU the firmware will be reloaded

Quality check : Tests of the 420 boards after production

- Check the supply voltages
- Check the temperature sensor
- Upload of the ASIC Parameters
- Check connections to the FPGA
- FPGA firmware upload
- Threshold scan
- Calibration

The distribution of main supply voltages measured by the on-board ADC.





Temperature distribution

Cosmic test data with partially equipped detector – clear Cherenkov rings are observed