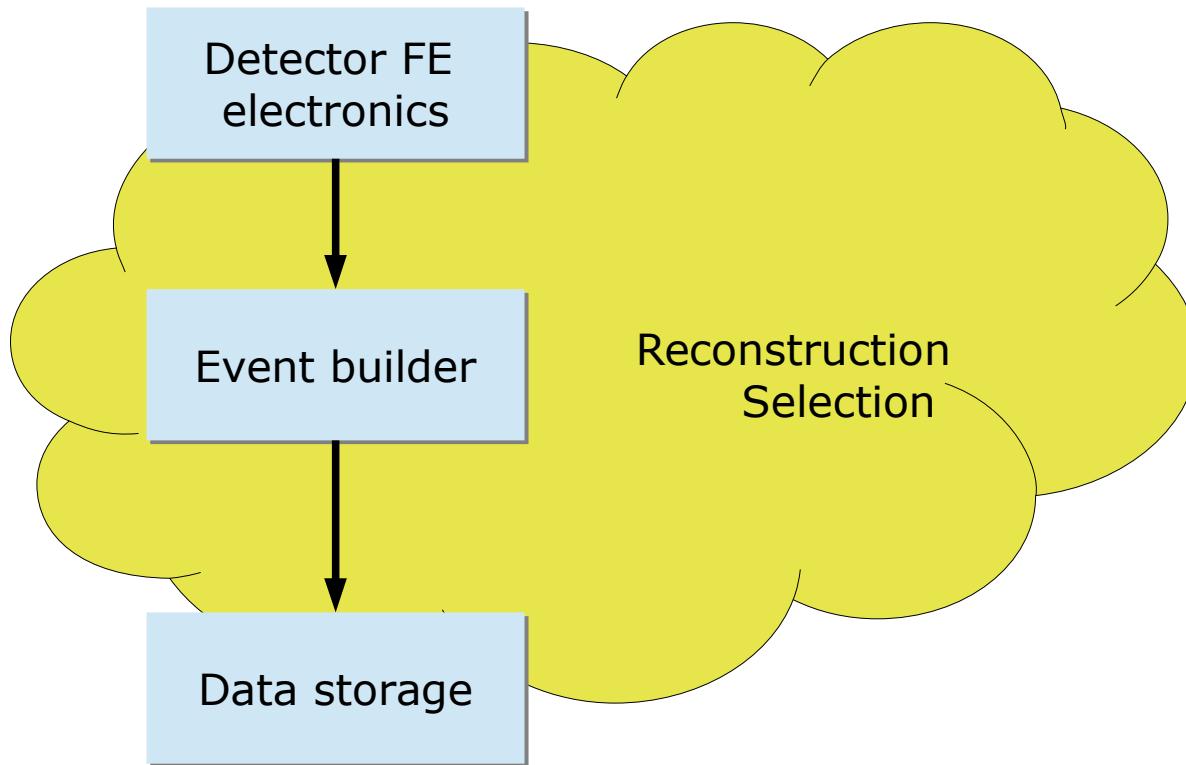


1st FCC-ee mini-workshop on Detector Requirements
17-18 June 2015
CERN

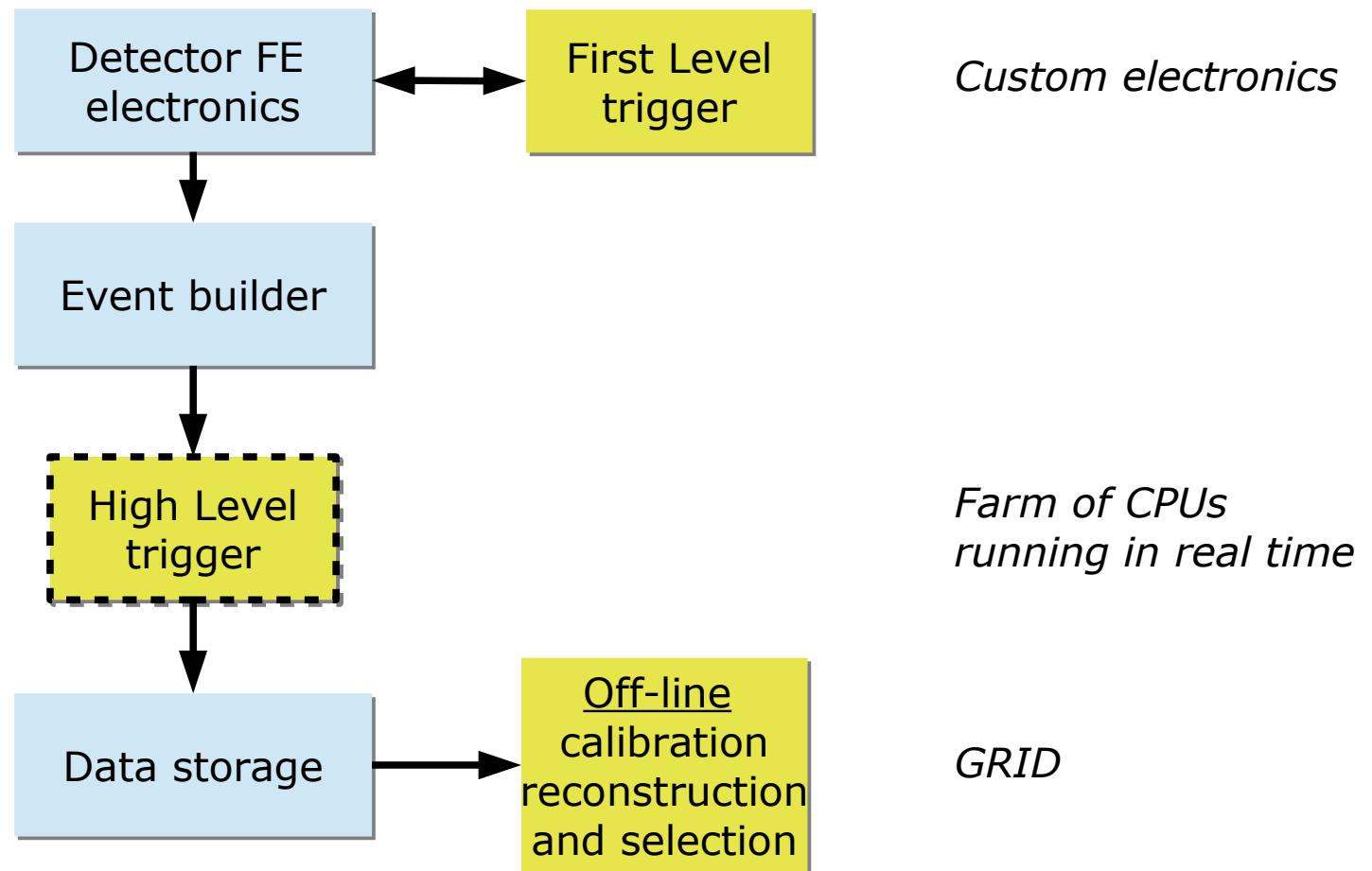
LHCb upgrade (hardware-less) trigger

R. Le Gac
CPPM, CNRS/IN2P3

Corner stones for readout systems



Readout system with trigger



Pro and Cons

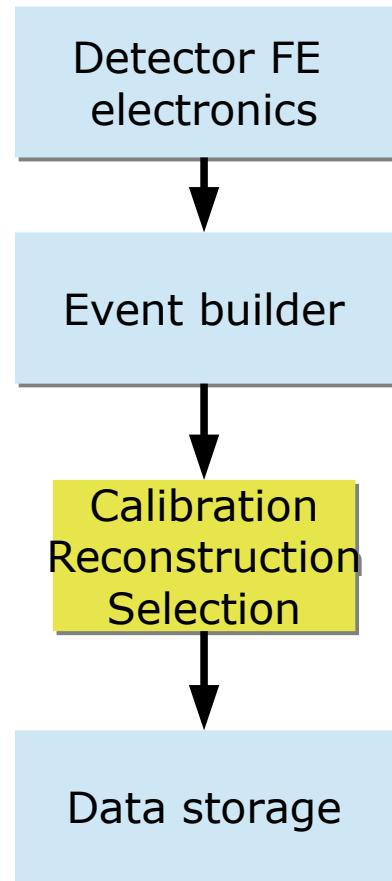
▶ Pro

- Reduce the bandwidth a soon as possible
- Minimize the size of the event builder
- Calibrations and final reconstruction are ran off-line and can be repeated several times

▶ Cons

- Complex integration of the first level trigger with the FE electronics
- Bias and inefficiencies introduced by the first level trigger
- Coherence between *on-line* and *off-line* reconstruction
- Require large computer resource on the GRID

Readout system trigger-less “*b* and *c* -factory”: full reconstruction and selection in real time



*Farm of CPUs
running in real time*

Pro and Cons

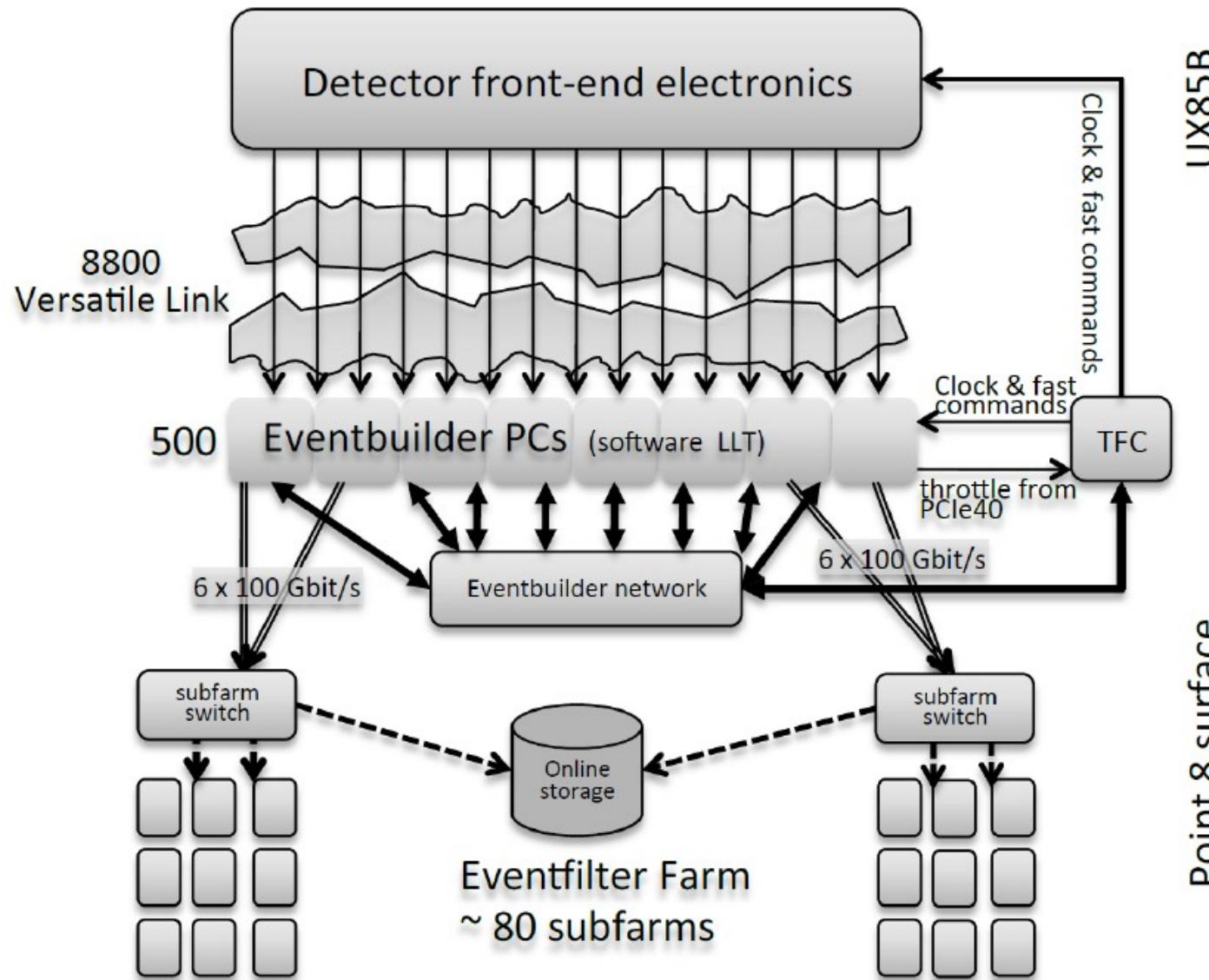
▶ Pro

- **Maximize the efficiencies to collect many particles ($D, D_s, B, B_s, \Lambda_b \dots$) with very different production rates and kinematic phase spaces.**
- Data are ready to be analysed as soon as they are collected
- Only one reconstruction and selection process
- Storage might be reduced (no RAW keep only micro-DST)
- GRID resource might be reduced

▶ Cons

- Large bandwidth requires between the FE and the event builder
- Large scale event builder
- Large scale event filter farm
- Calibration has to be determined in real time
- Reconstruction is only run once

LHCb readout system for the upgrade



Front-end electronics

- ▶ One of the most difficult part
 - Custom electronic which is specific to each detector
 - Running in a harsh environment
(space, radiation, power dissipation, cooling, ...)
 - Many channels distributed over either small or large volume
 - Zero suppression and data compression

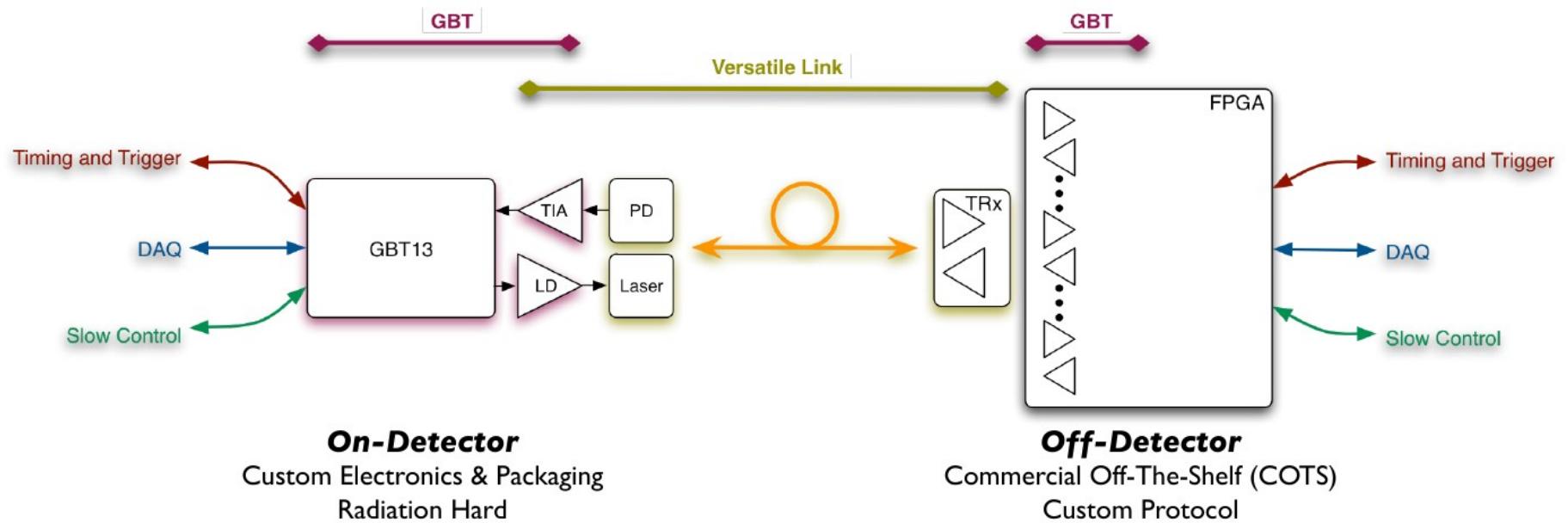
- ▶ Challenge
 - Would it be possible to concentrate data as much as possible and to push them on very large bandwidth links using a well established network protocol (100 Gb Ethernet, 400 Gb) ?

Serial high speed optical links

- ▶ ~9000 data links in LHCb upgrade
- ▶ Very nice:
 - Large bandwidth, cable with small diameter and light weight material
 - No electromagnetic coupling between FE and the event builder
- ▶ But expensive
 - Cost increases with the bandwidth and the distance
 - Cost decreases when links are merged into ribbon: 12 / 24 / 48 fibres
- ▶ Emitter
 - No commercial rad-hard emitter
CERN developed the GBT chip and the Versatil link (4.5 Gb/s)
 - Current bandwidth for commercial off-the shelf component, 10 -25 Gb/s on a single fibre, 100 Gb/s by aggregating several fibres, ...)

Bi-directional versatil link

<https://espace.cern.ch/project-versatile-link/public>



IN LHCb, the DAQ and the ECS (timing + fast command + slow control) flows are separated since it simplifies the architecture and ease the maintenance.

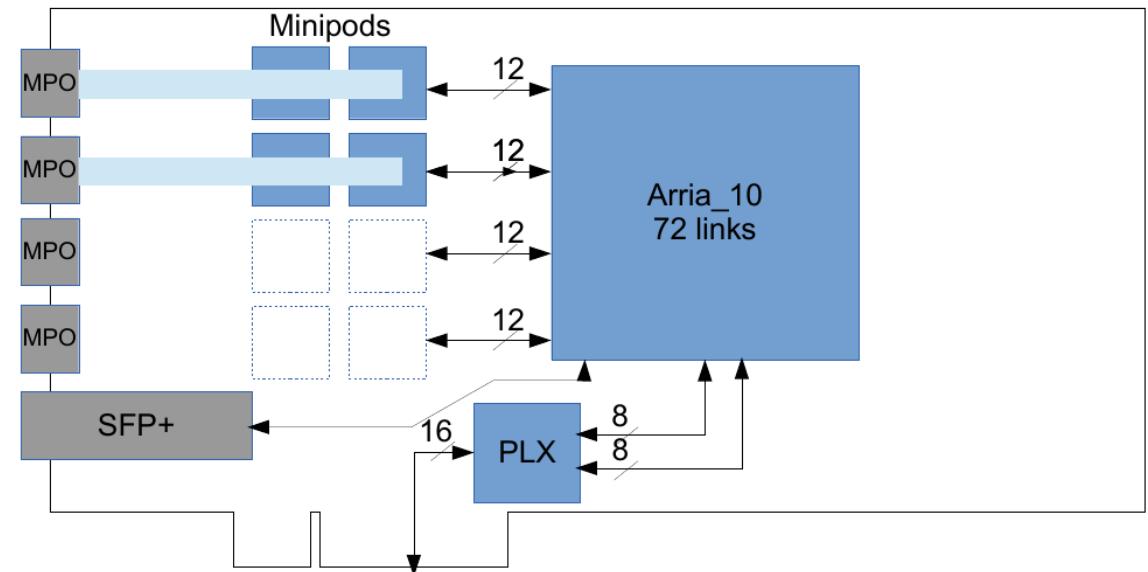
Interface the FE to the event builder

- ▶ PCI Express board.
Complex interface based on custom electronics:

Up to 48 optical inputs
Serial signal up to 10 Gb/s

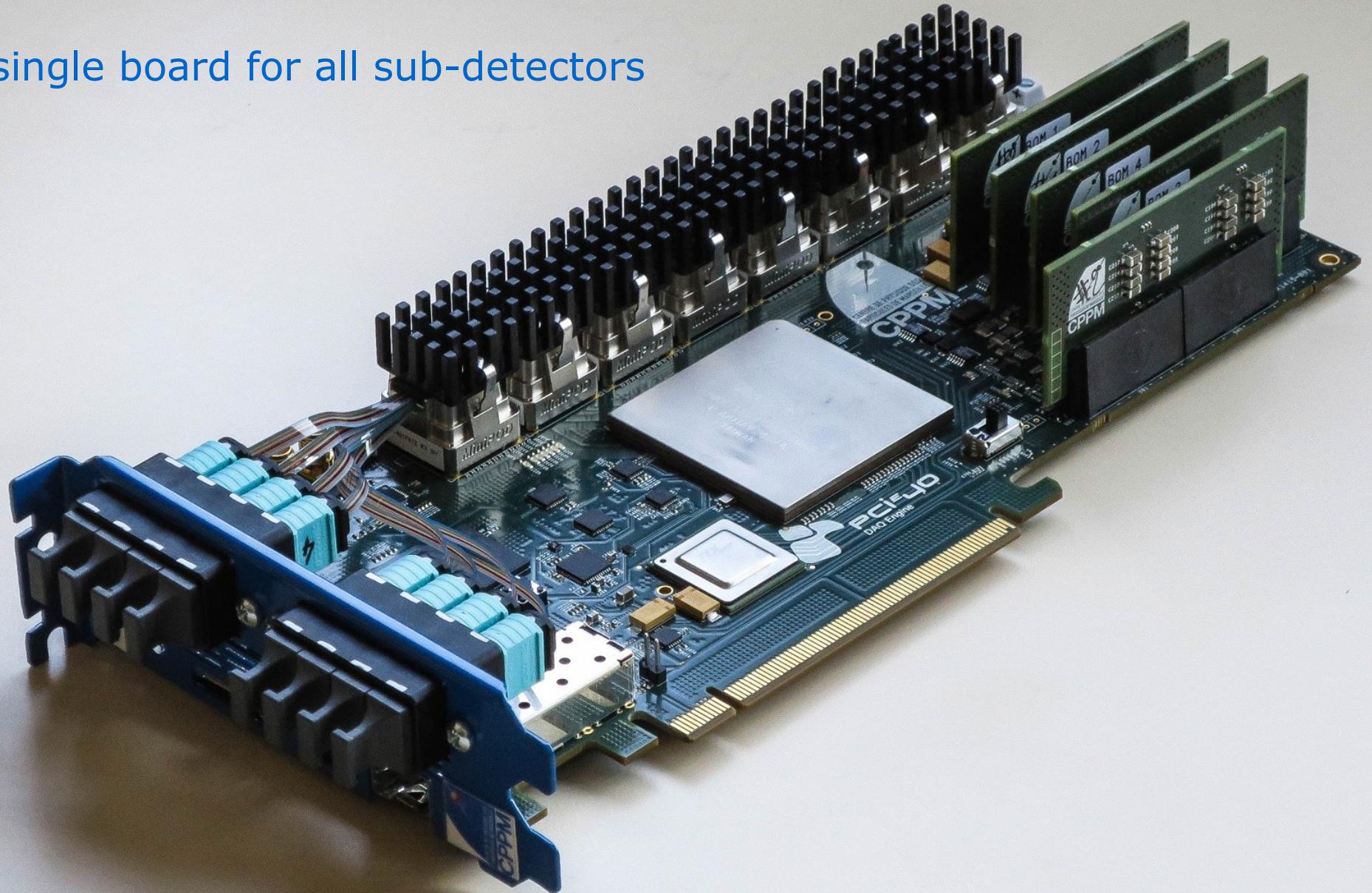
Up to 48 optical output
Serial signal up to 10 Gb/s

Bidirectional serial
links for the TFC



- ▶ The readout board is connected to the FE electronics via 24 optical links running the GBT protocol ($24 \times 4.5 \approx 100$ Gb/s)

A single board for all sub-detectors



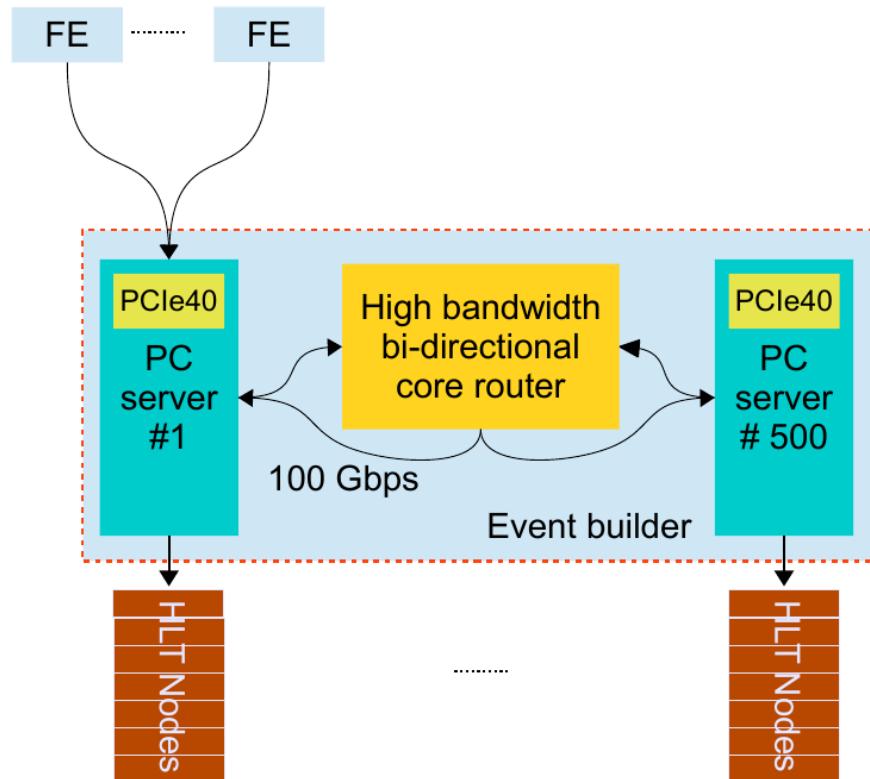
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Firmwares development

- ▶ The readout board relies on the last generation of FPGA from the Altera company (Arria10):
 - 1.15 million of logic cells
 - 72 High speed links
 - ...
- ▶ Developing the firmware for such complex component is an issue:
 - Experience electronics engineers
 - In most of the case the firmware depends on the sub-detector.
 - Select generic approach as far as possible
 - Set-up a teams of developers
 - Use framework and well defined interface to isolate the user code form the hardware specificities

The event builder (IT domain)

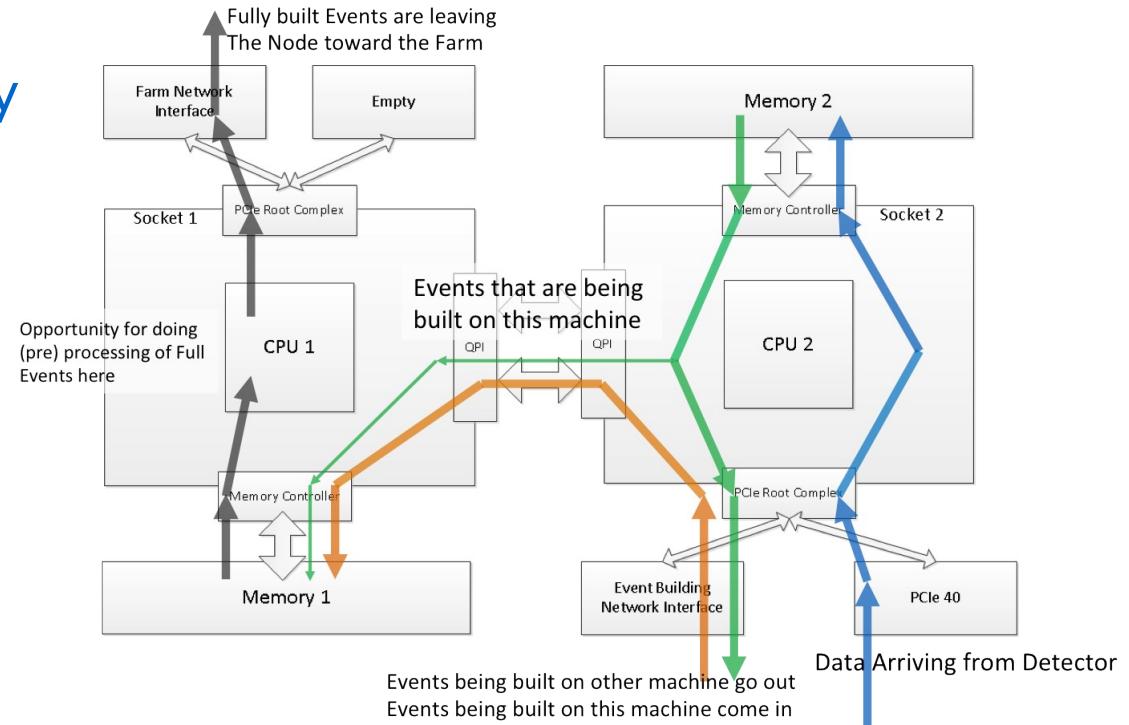
- ▶ 32 Tbits/s
- ▶ The challenge has been to find a cost effective solution:
 - Use component / technology widely use in Data Centre
 - Reduce the distance between readout boards, PC servers and switches
- ▶ 500 PC-servers connected to one switch through high bandwidth bi-directional links at 100 Gbps (Ethernet, infiniband, ...)



Event builder PC-server data flow

- ▶ 4 DMA transfers running in parallel and continuously

Total flow of 400 Gb/s



- ▶ Difficult to experience a large scale system in the lab (High Performance Computing sites)
- ▶ Scalability of the event builder is under study.

Calibration in real time

- ▶ Difficult to achieve day 1 since you have to understand your detector.
- ▶ In LHCb Run2, the calibration is performed by run and by fill. A complex sequence of processes have been deployed to run simultaneously the calibration and the event selection:

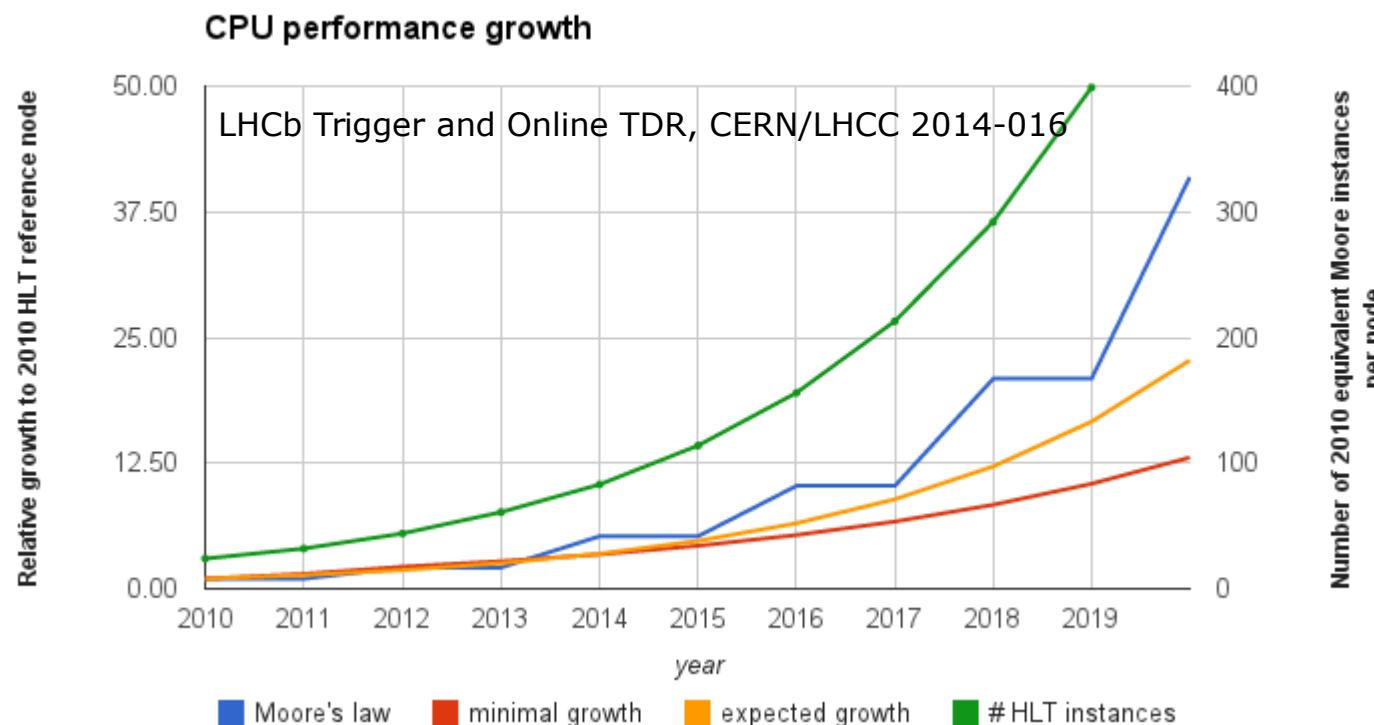
- When VertexLocator (VELO) subdetector is closed:
 - Accumulate data for tracking detector alignment O(5 min)
 - Perform tracking detector alignment on these data O(6 min)
 - Change run in HLT1 partition and load tracking alignment
 - Take data for the rest of the fill using offline quality alignment
 - Change run every ~60 minutes
- At end of each run taken with the DAQ / HLT1
 - Perform RICH calibrations
 - Start HLT2 processing
 - Start HLT2 monitoring
- At end of each run processed by HLT2
 - Start data quality monitoring



Reconstruction, selection in real time

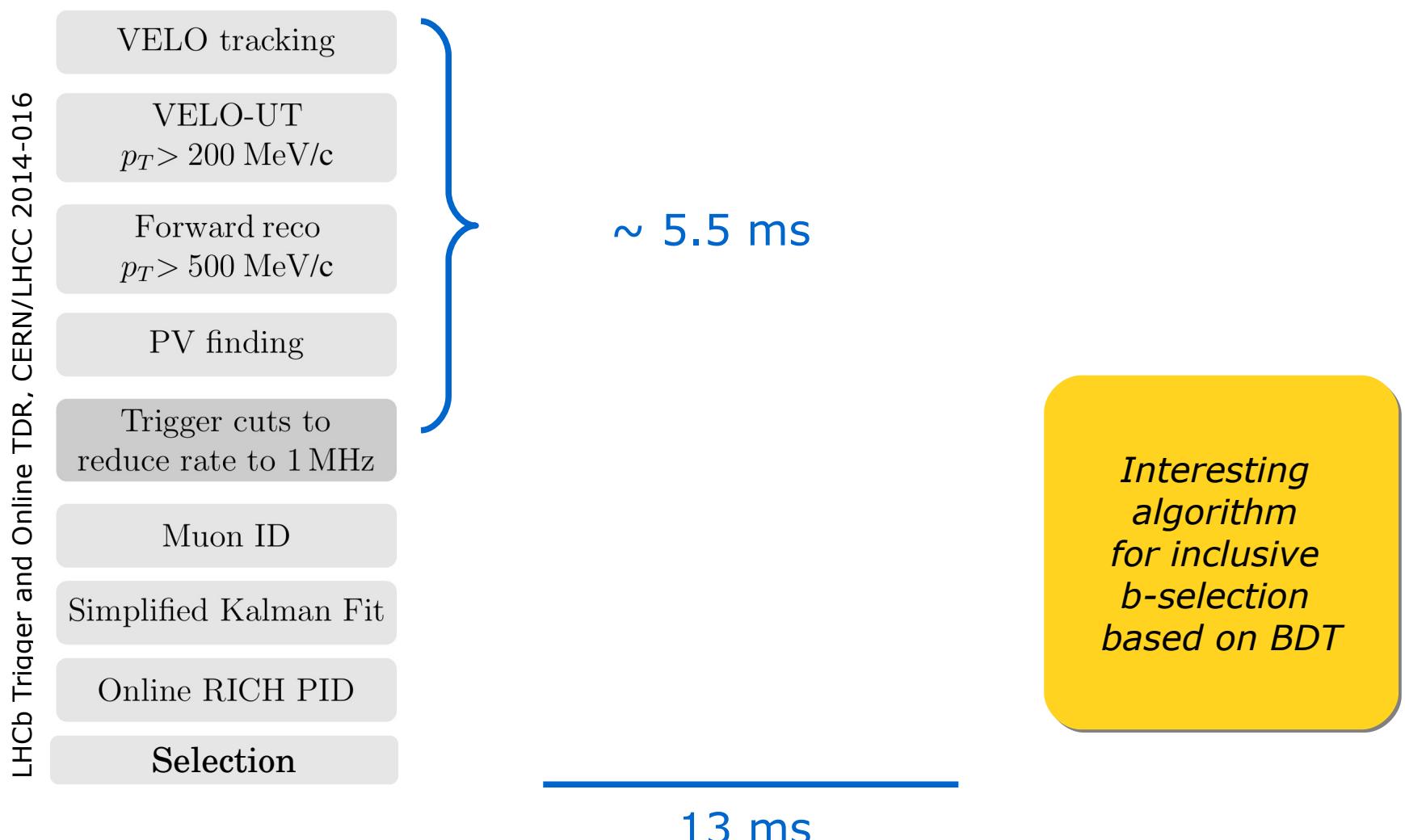
- ▶ Not an easy to extrapolate the CPU resource in 2020:

Server (2019)	1000
Tasks/ server	400
Time per collision	13 ms



Event filter algorithms for the upgrade

The design of the detector has been optimized to minimize the time of the tracking algorithm



Output stream

- ▶ The size of the output event has to be minimized. This is mandatory to maximize the statistics of interesting events.

The Grail is to keep only micro-DST containing reconstruct object.

LHCb Run 2:



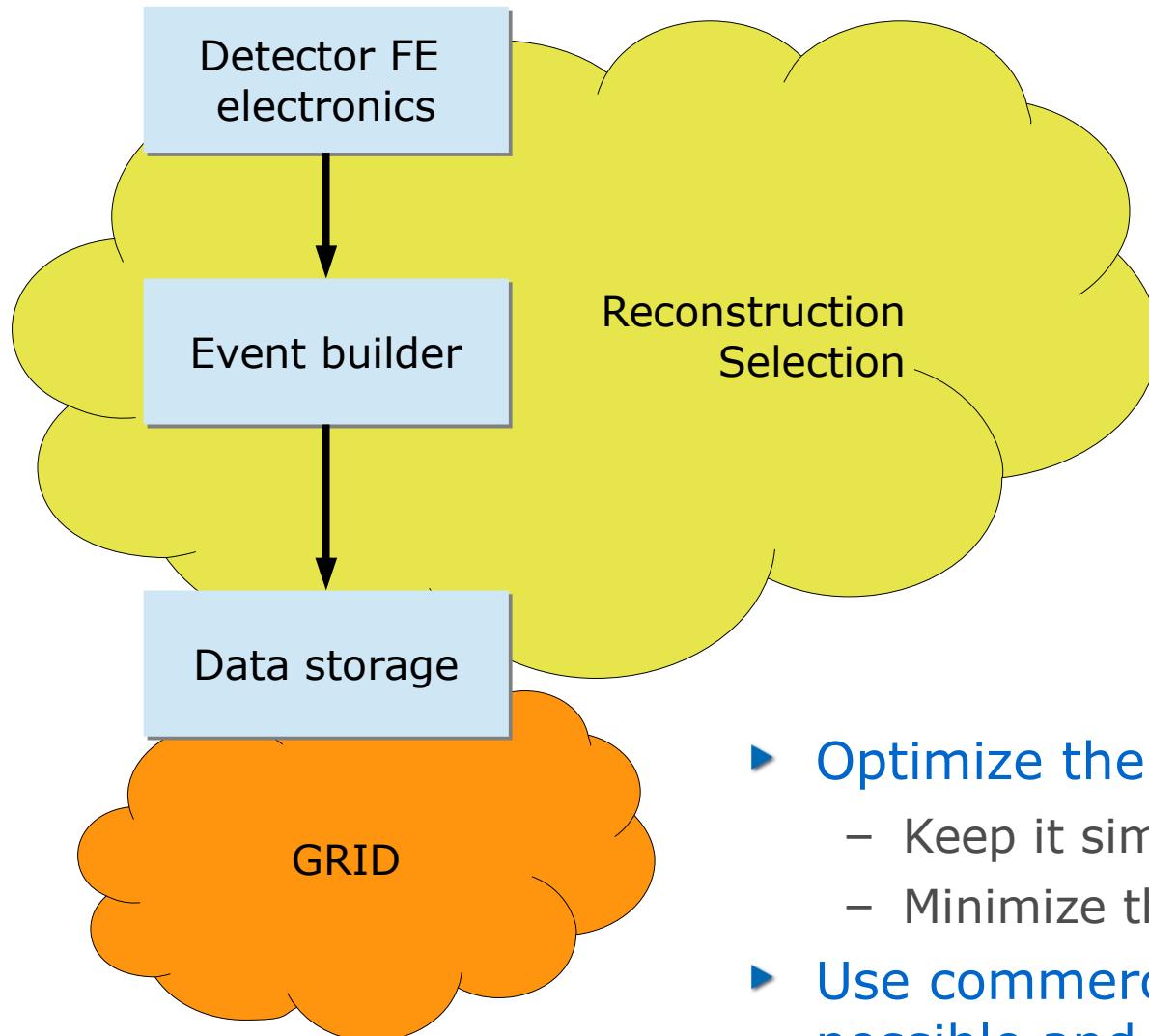
A fraction of the full stream will be parked and reconstructed during the next Long Shut down (2019-2020)

- ▶ How do you distribute the physics among the different stream ?

Software

- ▶ Nowadays, software require high level expertise:
 - The framework has to take benefit of multi-core CPU
 - Deal with multi-threading, vectorization,
 - Convergence off-line / on-line
 - Run on several CPU architectures (X86, GPU, XEON PHI, ARM, ...)
- ▶ Code optimisation is mandatory to reduce the CPU resources.

Conclusions: data processing



- ▶ Optimize the data processing globally:
 - Keep it simple, efficient and flexible
 - Minimize the cost and human resources
- ▶ Use commercial components as far as possible and deal with human aspect related to skill, contribution,